CYM8210BPM

2M x 16 Static RAM Module

Features

- **High-density 32-megabit SRAM module**
- **Low active power**
  - **5.3W (max.) at 25 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.725 in.**
- **Available in 80 pin SIMM Package**

Functional Description

The CYM8210 is a high-performance 8-megabit static RAM module organized as 2M words by 16 bits. This module is constructed using eight 512K x 8 SRAMs (CY62148) in SOJ packages mounted on an epoxy laminate board with pins.

Writing to each byte is accomplished by enabling the appropriate Chip Select (E0, E1, E2, E3) and write enable (WH or WL).

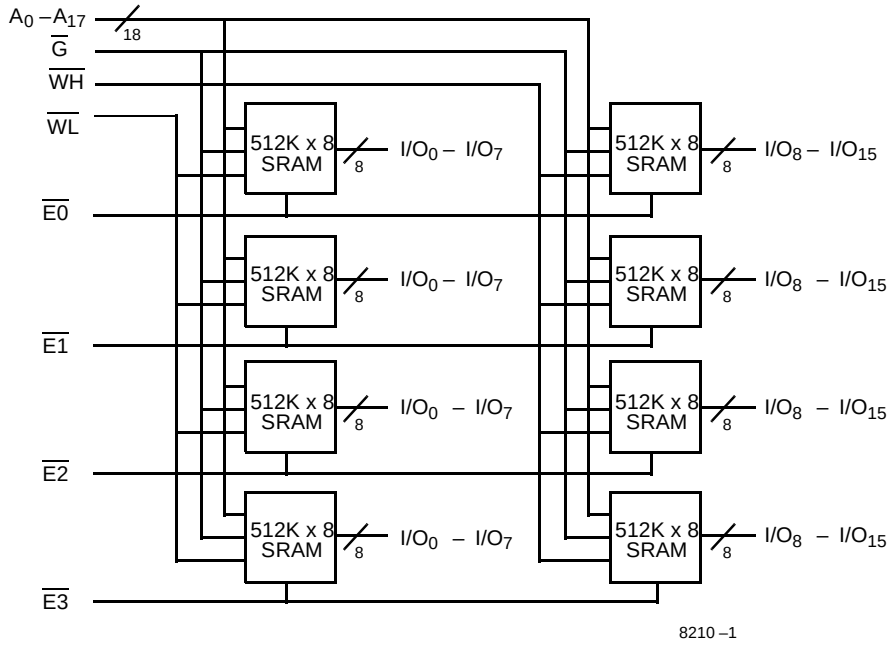
Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the appropriate chip select (E0, E1, E2, E3) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

The CYM8210 module is shipped as a 80 pin SIMM.

Logic Block Diagram

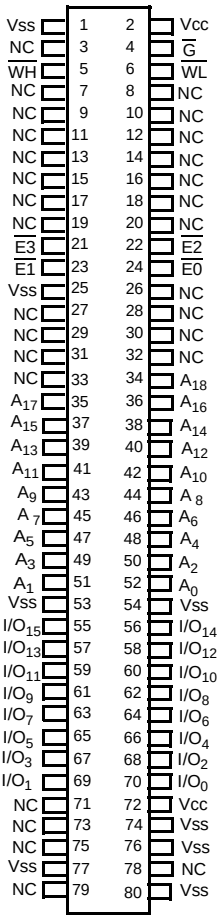


Selection Guide

	8210-70
Maximum Access Time (ns)	70
Maximum Operating Current (mA)	158
Maximum Standby Current (μA)	150

Pin Configurations

80-Pin SIMM Top View



8210 –2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –55°C to +125°C

Ambient Temperature with Power Applied–10°C to +85°C

Supply Voltage to Ground Potential–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State–0.5V to +7.0V

DC Input Voltage–0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

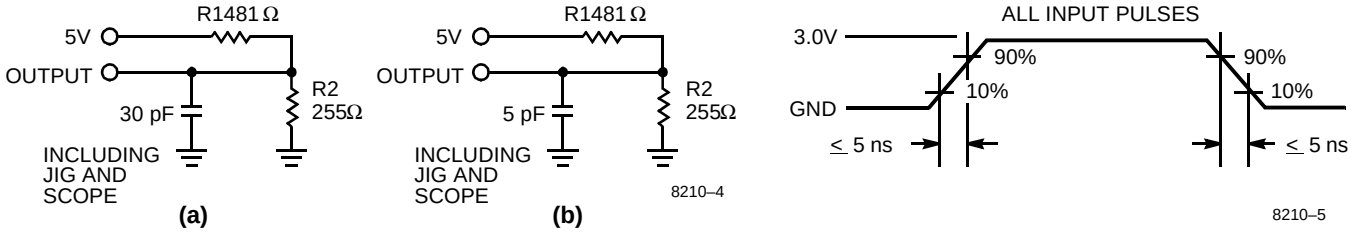
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM8210-70		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		158	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		120	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V		150	µA

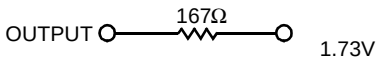
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	60	pF
C_{OUT}	Output Capacitance		50	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. A pull-up resistor to V_{CC} on the $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

Switching Characteristics Over the Operating Range[3]

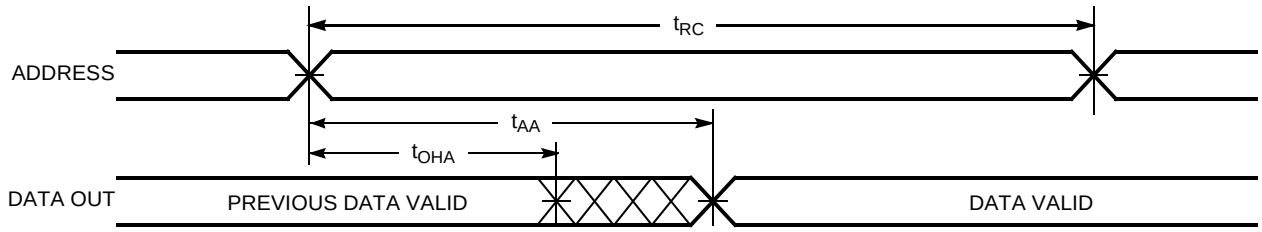
Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Output Hold from Address Change	10		ns
t_{ACS}	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{G}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{G}$ LOW to Low Z	5		ns
t_{HZOE}	$\overline{G}$ HIGH to High Z		25	ns
t_{LZCS}	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ LOW to Low Z[4]	10		ns
t_{HZCS}	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ HIGH to High Z[4, 5]		25	ns
t_{PD}	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ HIGH to Power-Down		70	
WRITE CYCLE[6]				
t_{WC}	Write Cycle Time	70		ns
t_{SCS}	$\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ LOW to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WH}/\overline{WL}$ Pulse Width	55		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WH}/\overline{WL}$ HIGH to Low Z	5		ns
t_{HZWE}	$\overline{WH}/\overline{WL}$ LOW to High Z[5]		25	ns

Notes:

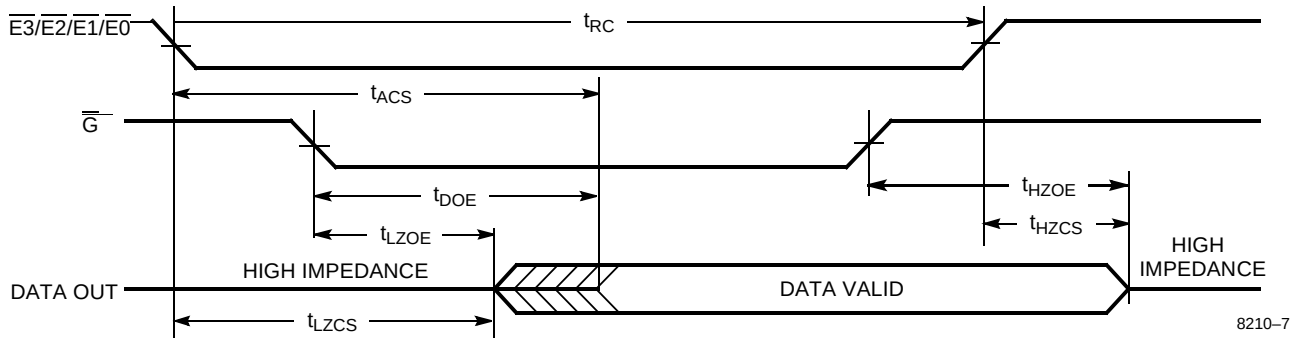
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ LOW and $\overline{WH}/\overline{WL}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

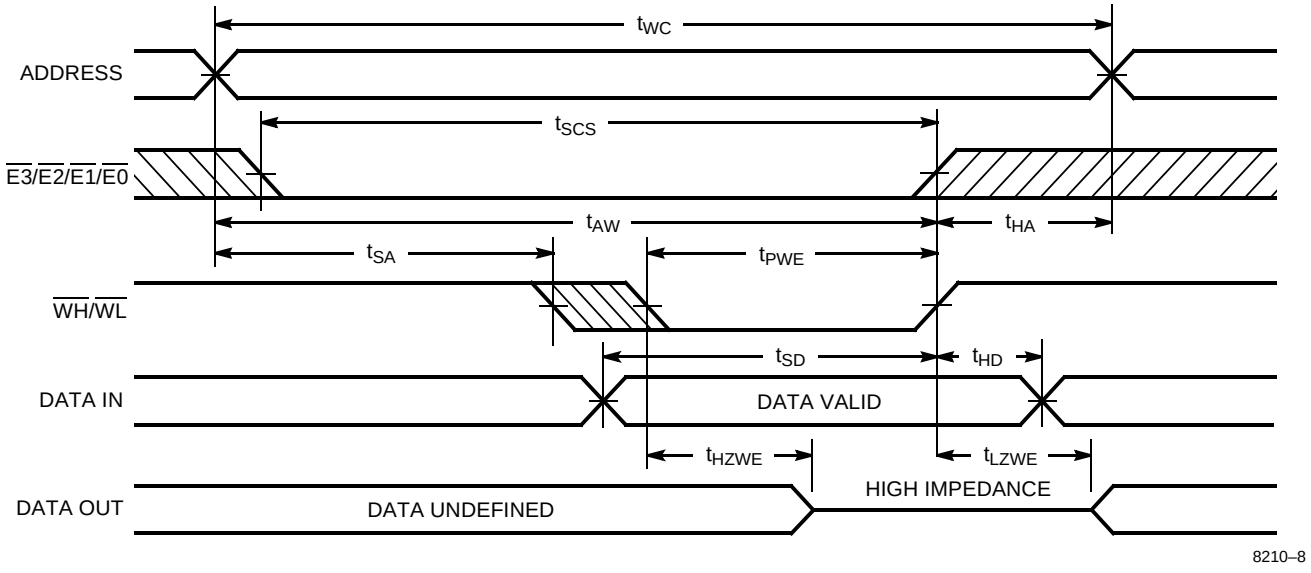
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



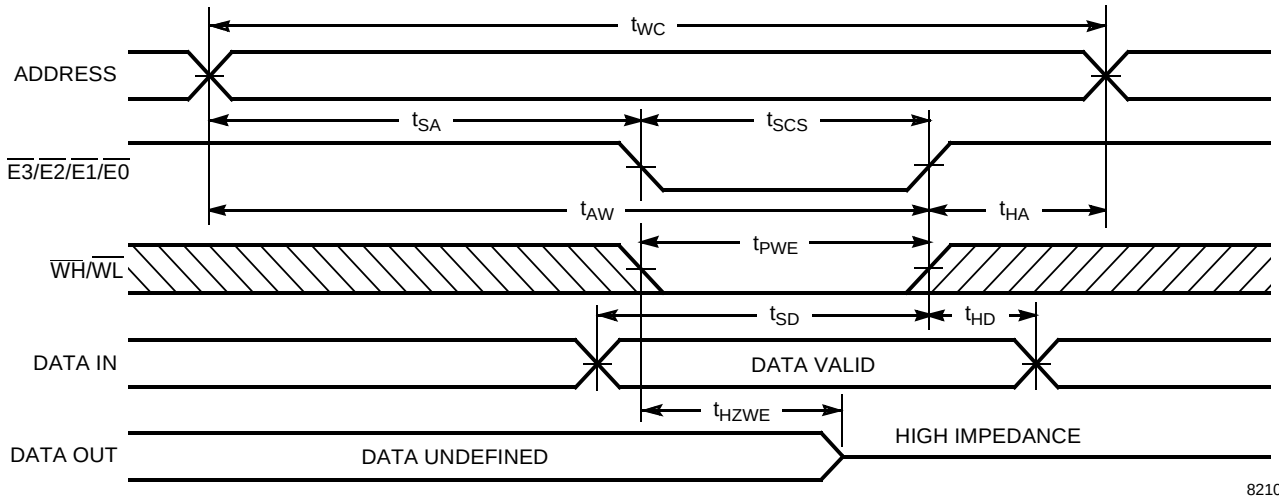
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Notes:
7. $\overline{WH}/\overline{WL}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0} = V_{IL}$ and $\overline{G} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ Controlled)[6, 10]



Note:

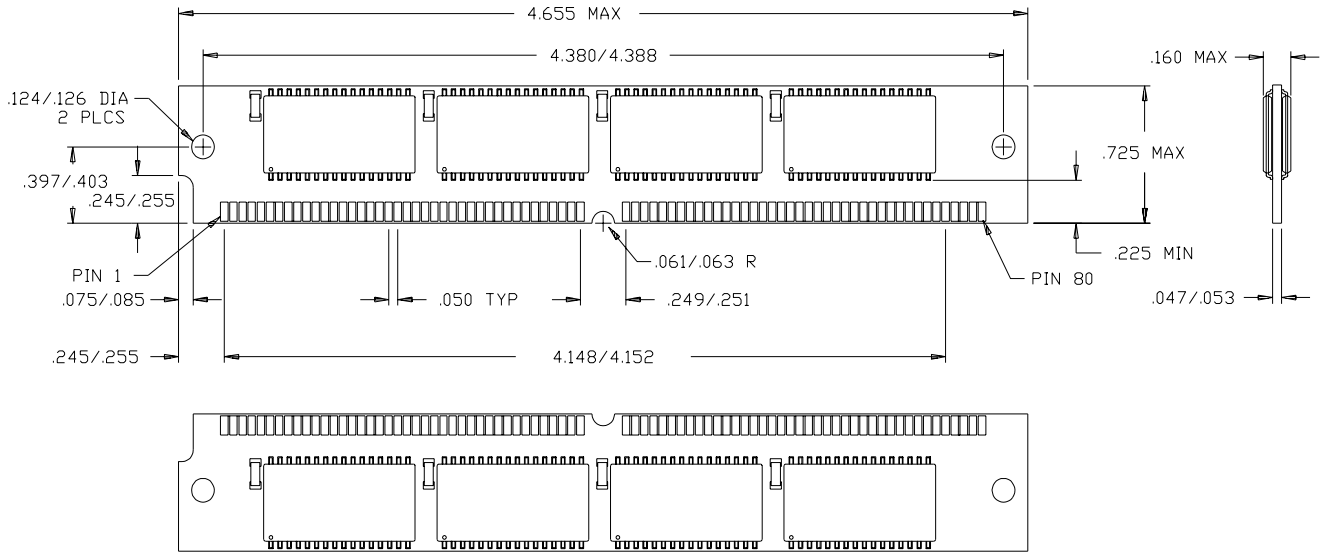
10. If $\overline{E3}/\overline{E2}/\overline{E1}/\overline{E0}$ goes HIGH simultaneously with $\overline{WH}/\overline{WL}$ HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYM8210BPM-70C	PM49	80-Pin Plastic SIMM Module	Commercial

Package Diagrams

80-Pin Plastic SIMM Module PM49



Document Title: CYM8210BPM 2M X 16 SRAM Module Datasheet Document Number: 38-05008				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106011	05/07/01	MEG	New Data Sheet