# 512K/1M x 72 Flowthrough NoBL SRAM Module

## Features

- **Operates at 66 MHz**
- **Uses 256K/512K x 18 high performance Flowthrough NoBL synchronous SRAMs**
- **3.3V data inputs/outputs**

## Functional Description

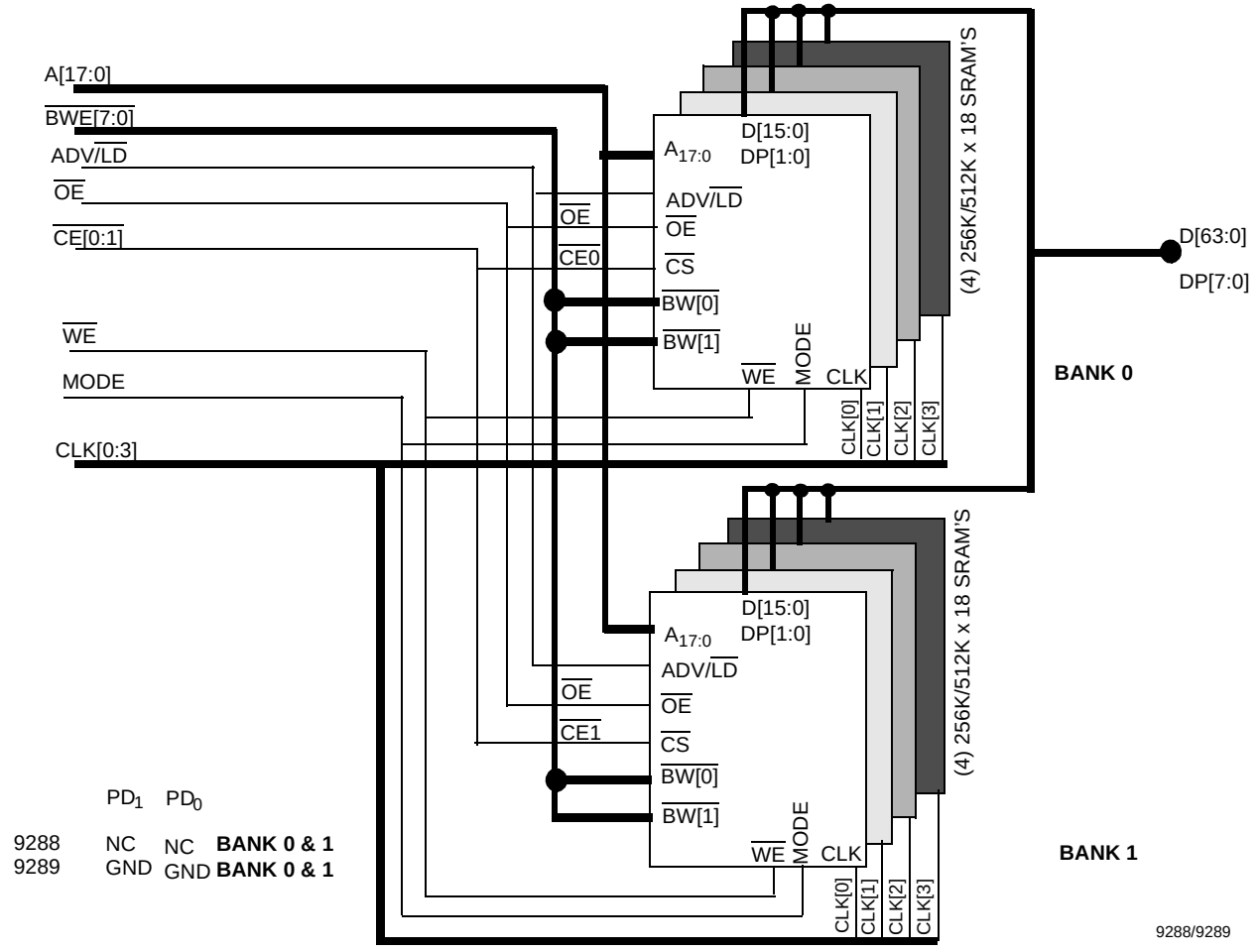
The CYM9288/9289 are high-performance synchronous Flowthrough NoBL memory modules organized as 512K/1M by 72 bits. These modules are constructed from 256K/512K x 18 NoBL SRAM's in plastic surface mount packages on an epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

Modules are configured as either one or two banks, where each bank has separate chip select controls. Separate clocks are provided for every pair of SRAMs.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 200 micro-inches (minimum) of 90/10 tin/lead over 50 micro-inches of nickel.

## Logic Block Diagram - CYM9288/9289

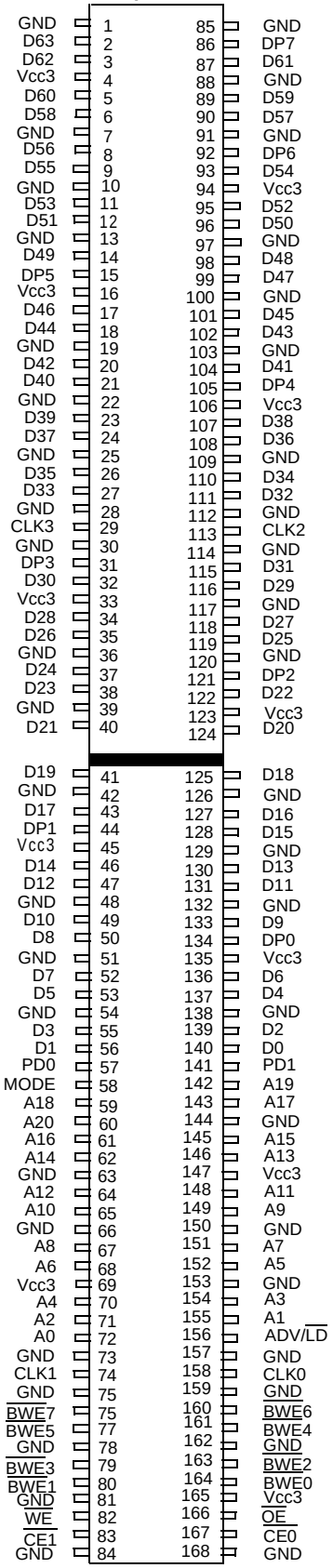


## Selection Guide

| | NoBL Synchronous Module | | | |
|---|---|---|---|---|
| **Part Number** | **CYM9288-60** | **CYM9288-66** | **CYM9289-60** | **CYM9289-66** |
| Cache Size | 512 K x 72 | 512 K x 72 | 1M x 72 | 1M x 72 |
| SRAMs Used | 8 of 256K x 18 | 8 of 256K x 18 | 8 of 512K x 18 | 8 of 512K x 18 |
| System Clock (MHz) | 60 | 66 | 60 | 66 |
| Data $t_{CDV}$ | 12 ns | 10.5 ns | 12 ns | 10.5 ns |

## Pin Configuration

**Dual Read-Out ZIP**
**Top View**




9288/9289

## Pin Definitions

| Signal | Description |
|---|---|
| $V_{CC3}$ | 3.3V supply |
| GND | Ground |
| A[20:0] | Addresses from processor |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{BWE[7:0]}$ | Byte Write Enables |
| $\overline{CS}$[1:0] | Chip Select for the two banks |
| $PD_0$–$PD_1$ | Presence Detect output pins |
| D[63:0] | Data lines from processor |
| DP[7:0] | Data Parity lines from processor |
| CLK[0:3] | Clock lines to the module |
| ADV/$\overline{LD}$ | Advance Load Signal from processor |
| Mode | Mode pin for Burst Selection |
| NC | Signal not connected on module |
| RSVD | Reserved |

## Presence Detect Pins

| | **$PD_1$** | **$PD_0$** |
|---|---|---|
| CYM9288 - 512K x 72 | NC | NC |
| CYM9289 - 1M x 72 | GND | GND |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –55°C to +125°C

Ambient Temperature
with Power Applied 0°C to +70°C

Supply Voltage to Ground Potential –0.5V to +4.5V

DC Voltage Applied to Outputs
in High Z State –0.5V to +4.6V

DC Input Voltage –0.5V to +4.6V

Output Current into Outputs (LOW)20 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 5% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | –0.3 | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. $I_{OH}$ = –4 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. $I_{OL}$ = 8 mA | | 0.4 | V |
| $I_{CC}$ (9288) | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | | 2400 | mA |
| $I_{CC}$ (9289) | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | | 2400 | mA |

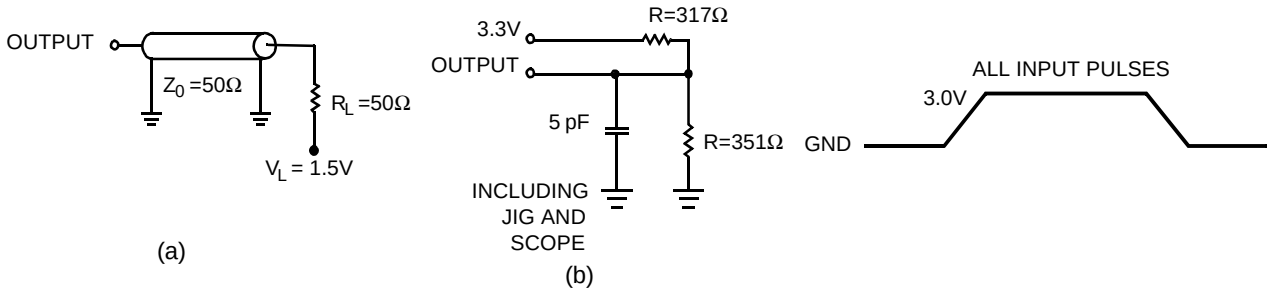
## Capacitance[1]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_A$ | Address Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 48 | pF |
| $C_I$ | Control Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 48 | pF |
| $C_O$ | Input/Output Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 16 | pF |
| $C_{CLK}$ | Clock Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 12 | pF |

**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



## Switching Characteristics Over the Operating Range[2]

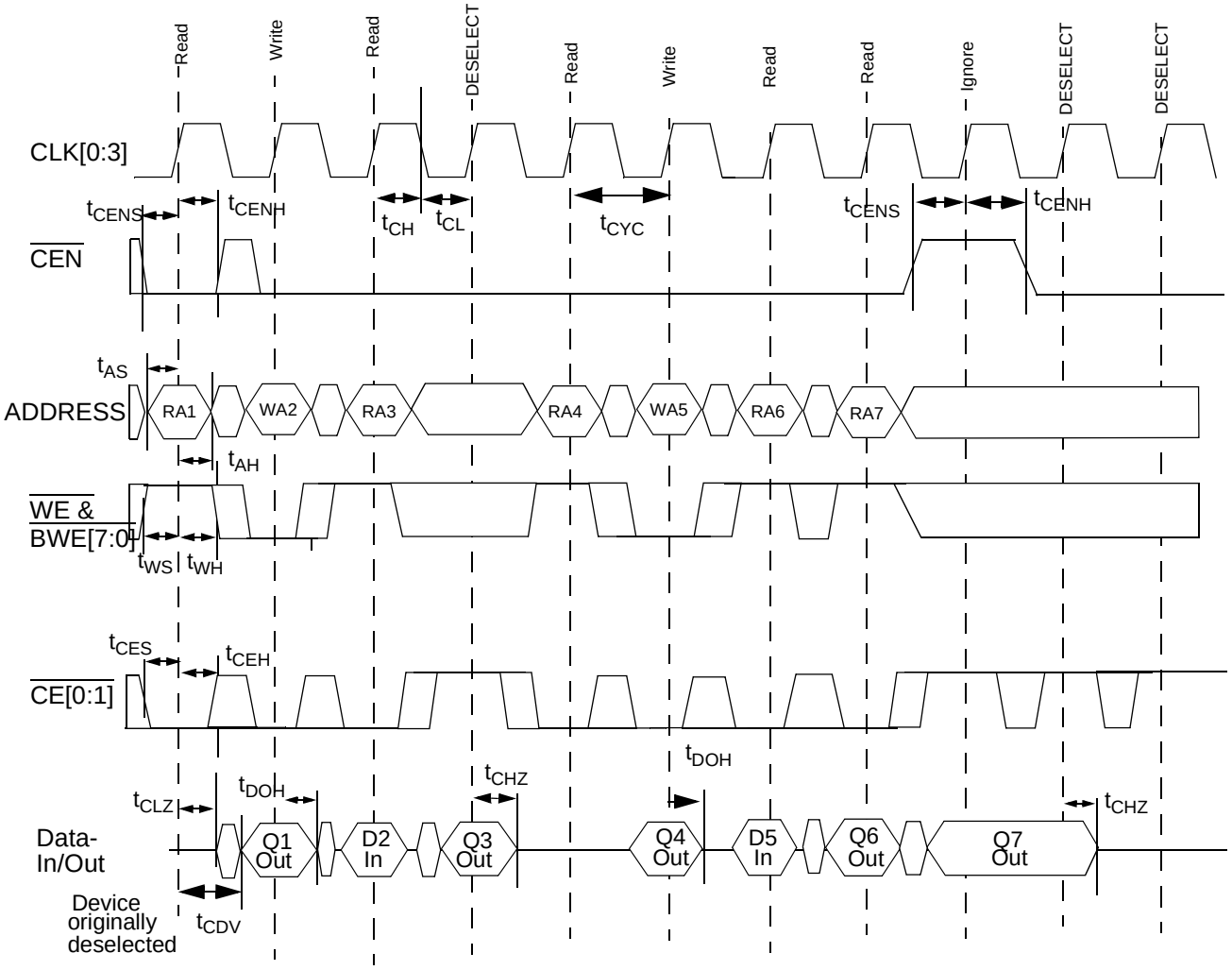
| Parameter | Description | 60 | | 66 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **Clock** | | | | | | |
| $t_{CYC}$ | Clock Cycle Time | 16.6 | | 15.0 | | ns |
| $F_{MAX}$ | Maximum Operating Frequency | | 60 | | 66 | MHz |
| $t_{CH}$ | Clock HIGH | 6.0 | | 5.0 | | ns |
| $t_{CL}$ | Clock LOW | 6.0 | | 5.0 | | ns |
| **Output Times** | | | | | | |
| $t_{CDV}$ | Data Output Valid After CLK Rise | | 12 | | 10.5 | ns |
| $t_{EOV}$ | $\overline{OE}$ LOW to Output Valid[3, 5] | | 6 | | 6 | ns |
| $t_{DOH}$ | Data Output Hold After CLK Rise | 1.5 | | 1.5 | | ns |
| $t_{CHZ}$ | Clock to High-Z[3, 4, 5] | | 5.0 | | 5.0 | ns |
| $t_{CLZ}$ | Clock to Low-Z[3, 4, 5] | 3.0 | | 2.0 | | ns |
| $t_{EOHZ}$ | $\overline{OE}$ HIGH to Output High-Z[3, 4, 5] | | 6.0 | | 6.0 | ns |
| $t_{EOLZ}$ | $\overline{OE}$ LOW to Output Low-Z[3, 4, 5] | 0 | | 0 | | ns |
| **Setup Times** | | | | | | |
| $t_{AS}$ | Address Set-Up Before CLK Rise | 2.5 | | 2.0 | | ns |
| $t_{DS}$ | Data Input Set-Up Before CLK Rise | 2.5 | | 2.0 | | ns |
| $t_{WES}$ | $\overline{WE}$, $\overline{BWE}_{[7:0]}$ Set-Up Before CLK Rise | 2.5 | | 2.0 | | ns |
| $t_{ALS}$ | ADV/$\overline{LD}$ Set-Up Before CLK Rise | 2.5 | | 2.0 | | ns |
| $t_{CES}$ | Chip Selects Set-Up | 2.5 | | 2.0 | | ns |
| **Hold Times** | | | | | | |
| $t_{AH}$ | Address Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{DH}$ | Data Input Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{WEH}$ | $\overline{WE}$, $\overline{BWE}_{[7:0]}$ Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{ALH}$ | ADV/$\overline{LD}$ Hold after CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{CEH}$ | Chip Selects Hold After CLK Rise | 0.5 | | 0.5 | | ns |

**Notes:**

2. AC test conditions assume signal transition time of 2 ns or less, timing reference levels, input pulse levels and output loading shown in part (a) of AC Test Load for 3.3V devices and (c) for 2.5V devices. .
3. $t_{CHZ}$, $t_{CLZ}$, $t_{OEV}$, $t_{EOLZ}$, and $t_{EOHZ}$ are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
4. At any given voltage and temperature, $t_{EOHZ}$ is less than $t_{EOLZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
5. This parameter is sampled and not 100% tested.

## Switching Waveforms

### Read/Write/Deselect Timing



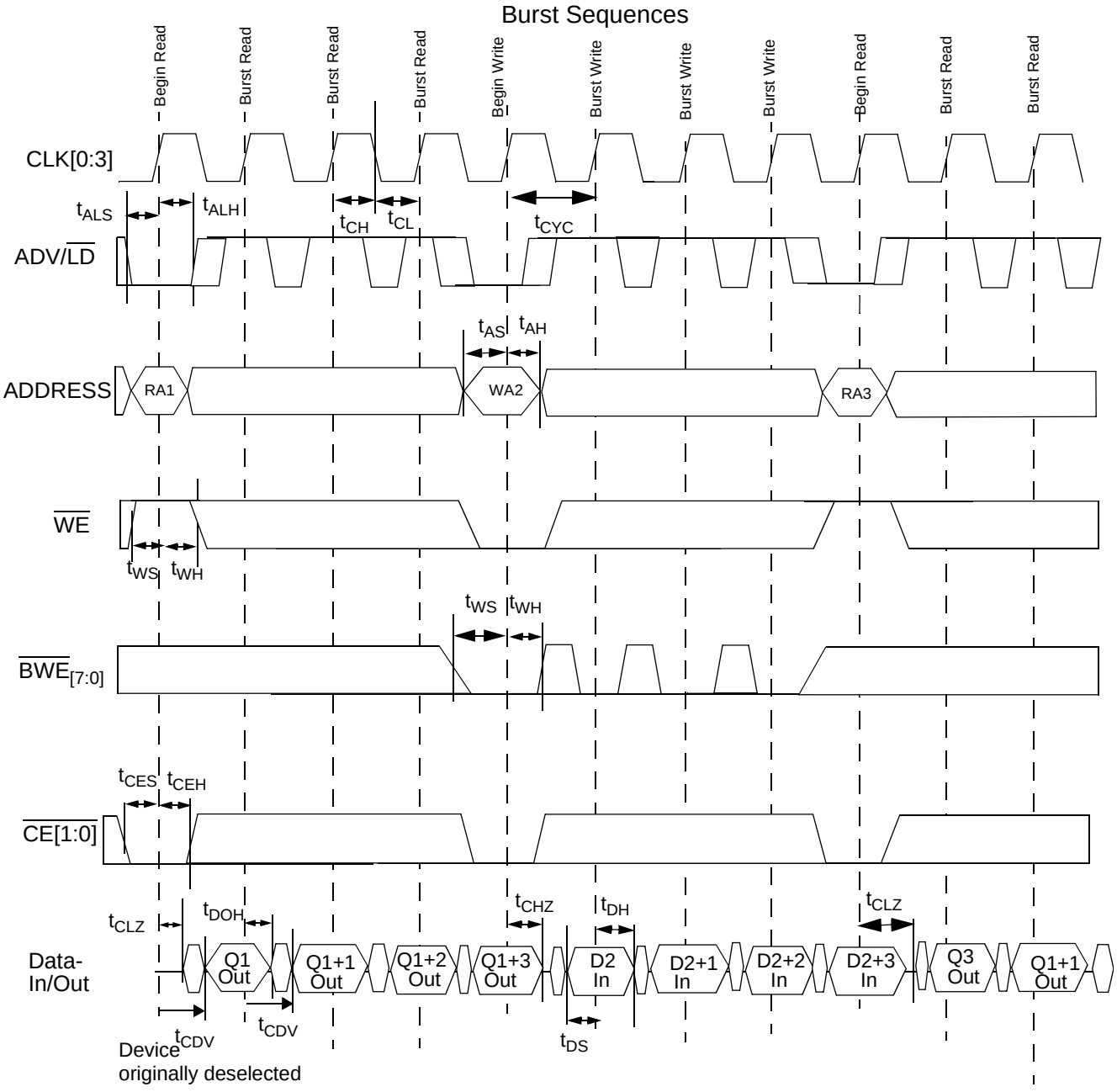

$\overline{WE}$ is the combination of $\overline{WE}$ & $\overline{BWE}_X$ to define a write cycle (see Write Cycle Description table).

RAx stands for Read Address X, WAx stands for
Write Address X, Dx stands for Data-in X, Qx stands for Data-out X.

= DON'T CARE = UNDEFINED

## Switching Waveforms (continued)

### Read/Write/Deselect Timing



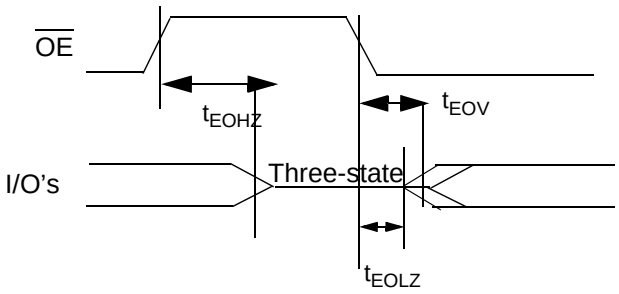

The combination of $\overline{WE}$ & $\overline{BWE}_{[7:0]}$ define a write cycle.

RAx stands for Read Address X, WAx stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWE}_{[7:0]}$ input signals. Burst order determined by the state of the Mode input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

## Switching Waveforms (continued)

### $\overline{OE}$ Timing




## Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Description | Operating Range |
|---|---|---|---|---|---|
| 60 | CYM9288APZ-60C | PZ12 | 168-Pin Quad-Row ZIP | Flowthrough NoBL 512K x 72 | Commercial |
| 66 | CYM9288APZ-66C | | | Flowthrough NoBL 512K x 72 | |
| 60 | CYM9289BPZ-60C | PZ12 | 168-Pin Quad-Row ZIP | Flowthrough NoBL 1M x 72 | Commercial |
| 66 | CYM9289BPZ-66C | | | Flowthrough NoBL 1M x 72 | |

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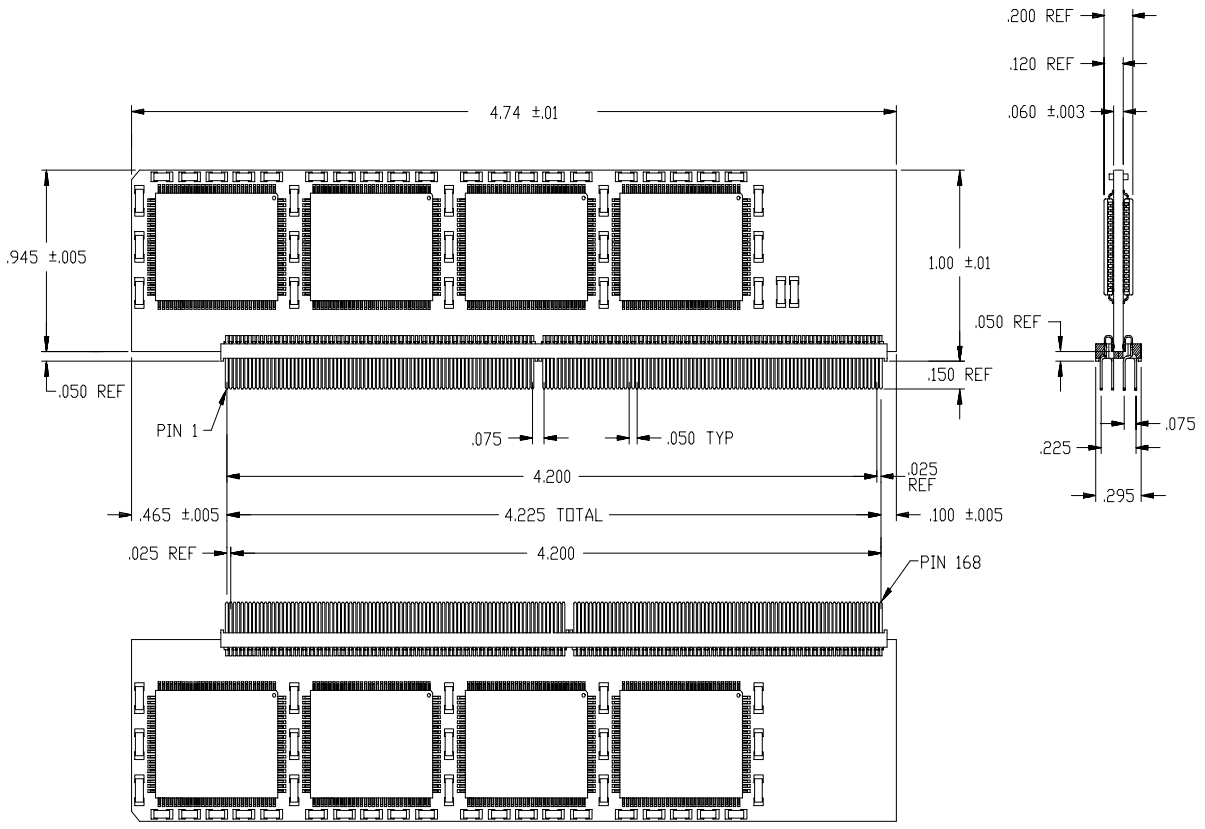
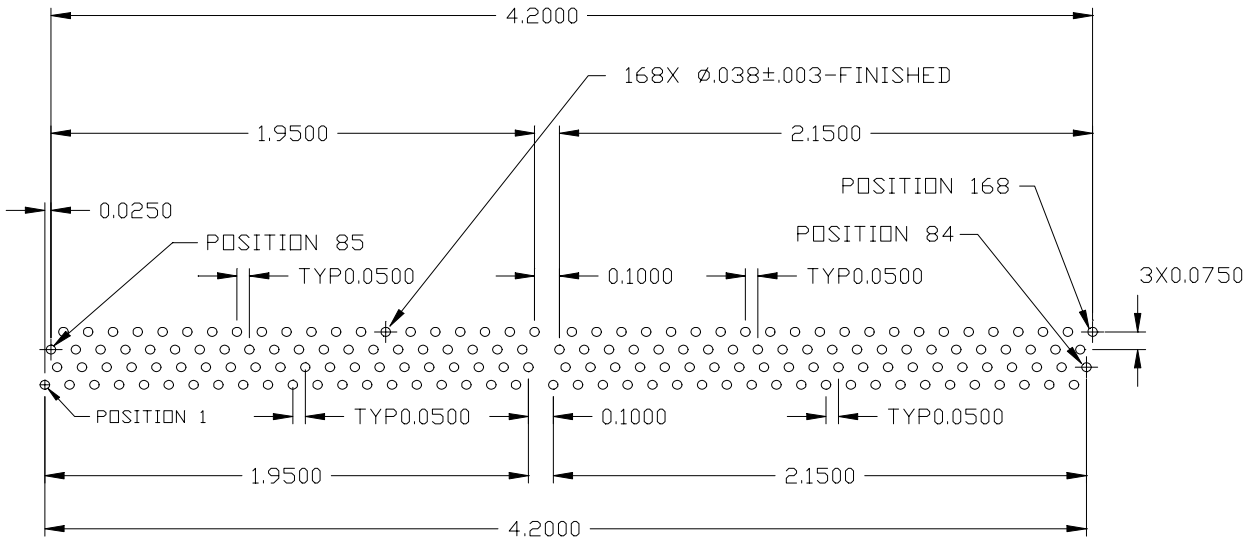
## Package Diagrams

### PZ12: 168 Pin Quad Row ZIP Module




RECOMMENDED HOST CARD LAYOUT (COMPONENT SIDE)