**ADVANCE INFORMATION**

# CY7C0851V25
# CY7C0852V25

## 2.5V 64K/128K x 36 Sync Dual-Port Static RAM

### Features

- **True Dual-Ported memory cells that allow simultaneous access of the same memory location**
- **Sync. Pipelined 4.5 Megabit devices**
  - **64K x 36 organization (CY7C0851V25)**
  - **128K x 36 organization (CY7C0852V25)**
- **Pipelined output mode allows fast 100-MHz operation**
- **0.18-micron CMOS for optimum speed/power**
- **High-speed clock to data access: 5 ns (max.)**
- **2.5V Low operating power**
  - **Active = 150 mA (typical)**
  - **Standby = 10 mA (typical)**
- **HSTL class 1 I/O (0.75 Vref)**
- **Counter wraparound control**
  - **Internal mask register controls counter wraparound**
  - **Counter-Interrupt flags to indicate wraparound**
  - **Memory Block Retransmit Operation**
- **Counter readback on address lines**
- **Mask register readback on address lines**
- **Interrupt flags for message passing**
- **Global Master reset**
- **Width and Depth expansion capabilities**
- **Dual Chip Enables on both ports for easy depth expansion**
- **Separate byte enables on both ports**
- **Commercial and Industrial temperature ranges**
- **IEEE 1149.1 JTAG boundary scan**
- **172-ball BGA (1-mm pitch) (15 mm x 15 mm x 0.51 mm)**

### Functional Description

The CY7C0851V25/CY7C0852V25 is a 4.5-Megabit pipelined synchronous true dual-port Static RAM. This is a high-speed, low-power 2.5V CMOS dual-port static RAM. Two ports are provided, permitting independent, simultaneous access for reads from any location in memory. A particular port can write to a certain location while the other port is reading that location simultaneously. The result of writing to the same location by more than one port at the same time is undefined. Registers on control, address, and data lines allow for minimal set-up and hold time.

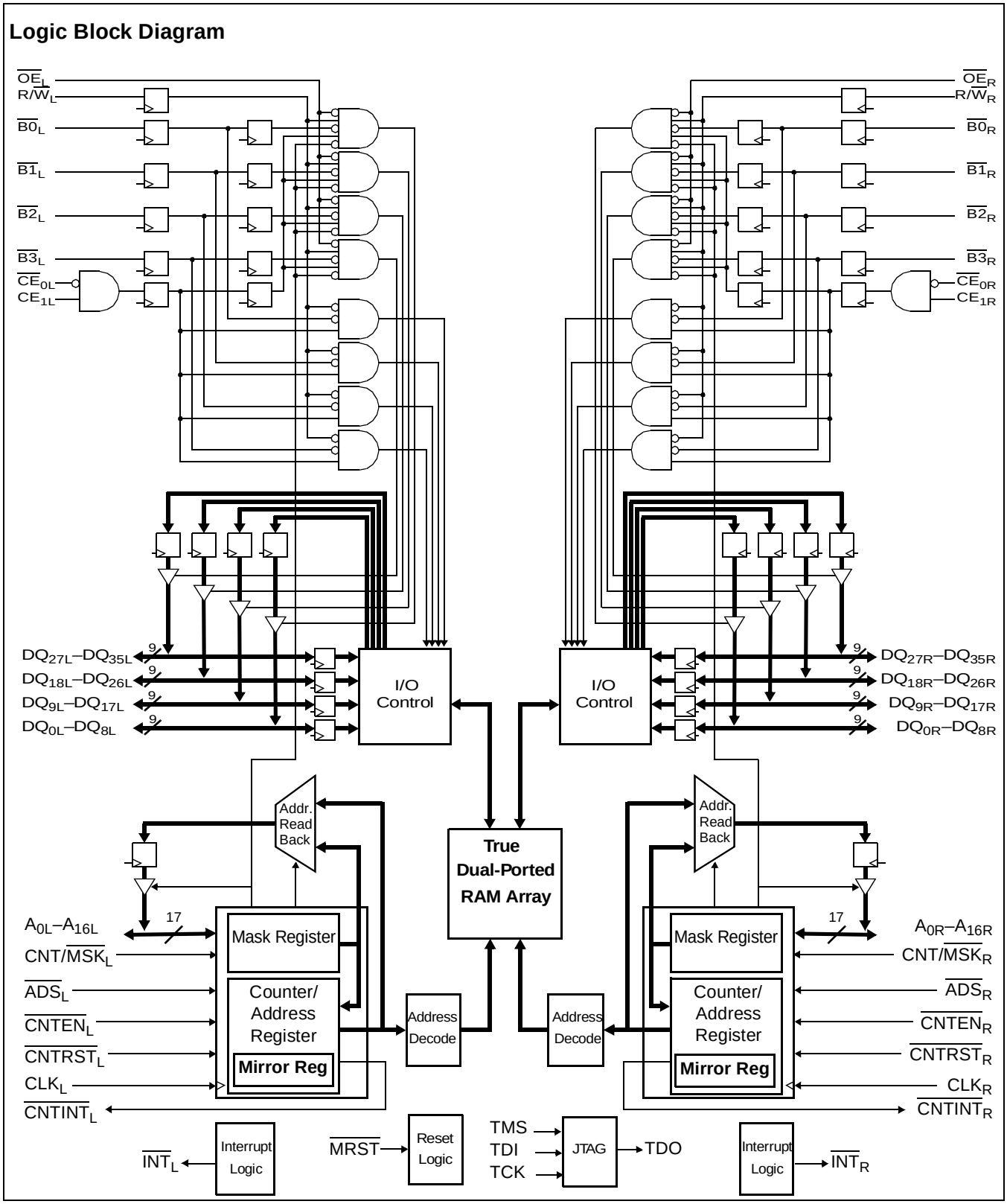
During a read operation, data is registered for decreased cycle time. Clock to data valid $t_{CD2}$ = 5 ns. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address the counter will self-increment the address internally (more details to follow). The internal write pulse width is independent of the duration of the R/W input signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE0}$ or LOW on CE1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. One cycle is required with chip enables asserted to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded when the port's address strobe ($\overline{ADS}$) and ($\overline{CNTEN}$) signals are LOW. When the port's counter enable ($\overline{CNTEN}$) is asserted and the $\overline{ADS}$ is deasserted, the address counter will increment on each LOW to HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until $\overline{CNTEN}$ is deasserted. The counter can address the entire memory array and will loop back to the start. Counter reset ($\overline{CNTRST}$) is used to reset the unmasked portion of the burst counter to 0s. A counter-mask register is used to control the counter wrap. The counter and mask register operations are described in more detail in the following sections.

New features added to the CY7C0851V25/CY7C0852V25 include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap-around and counter interrupt ($\overline{CNTINT}$) flags, readback of mask register value on address lines, retransmit functionality, interrupt flags for message passing, JTAG for boundary scan, and asynchronous Master Reset.

## Logic Block Diagram



## Pin Configuration

**172-Ball Grid Array (BGA)**

**Top View**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | DQ32L | DQ30L | **$\overline{\text{CNTINTL}}$** | VSSQ | DQ13L | VDDQ | DQ11L | DQ11R | VDDQ | DQ13R | VSSQ | **$\overline{\text{CNTINTR}}$** | DQ30R | DQ32R |
| **B** | A0L | DQ33L | DQ29 | DQ17L | DQ14L | DQ12L | DQ9L | DQ9R | DQ12R | DQ14R | DQ17R | DQ29R | DQ33R | A0R |
| **C** | **VREFL** | A1L | DQ31L | DQ27L | **$\overline{\text{INTL}}$** | DQ15L | DQ10L | DQ10R | DQ15R | **$\overline{\text{INTR}}$** | DQ27R | DQ31R | A1R | **VREFR** |
| **D** | A2L | A3L | DQ35L | DQ34L | DQ28L | DQ16L | VSSQ | VSSQ | DQ16R | DQ28R | DQ34R | DQ35R | A3R | A2R |
| **E** | A4L | A5L | **CE1L** | $\overline{\text{B0L}}$ | **VDDQ** | **VSSA** | | | **VDDA** | **VDDQ** | **$\overline{\text{B0R}}$** | **CE1R** | A5R | A4R |
| **F** | VDD | A6L | A7L | $\overline{\text{B1L}}$ | **VDDA** | | | | | **VSSA** | **$\overline{\text{B1R}}$** | A7R | A6R | VDD |
| **G** | $\overline{\text{OEL}}$ | $\overline{\text{B2L}}$ | $\overline{\text{B3L}}$ | $\overline{\text{CE0L}}$ | | | | | | | $\overline{\text{CE0R}}$ | **$\overline{\text{B3R}}$** | **$\overline{\text{B2R}}$** | $\overline{\text{OER}}$ |
| **H** | VSS | R/$\overline{\text{W}}$L | A8L | CLKL | | | | | | | CLKR | A8R | R/$\overline{\text{W}}$R | VSS |
| **J** | A9L | A10L | VSS | $\overline{\text{ADSL}}$ | **VSSA** | | | | | **VDDA** | $\overline{\text{ADSR}}$ | **$\overline{\text{MRST}}$** | A10R | A9R |
| **K** | A11L | A12L | **A15L** | $\overline{\text{CNTRSTL}}$ | **VDDQ** | **VDDA** | | | **VSSA** | **VDDQ** | $\overline{\text{CNTRSTR}}$ | **A15R** | A12R | A11R |
| **L** | **CNT/$\overline{\text{MSKL}}$** | A13L | $\overline{\text{CNTENL}}$ | DQ26L | DQ25L | DQ19L | VSSQ | VSSQ | DQ19R | DQ25R | DQ26R | $\overline{\text{CNTENR}}$ | A13R | CNT/**$\overline{\text{MSKR}}$** |
| **M** | **A16L** | A14L | DQ22L | DQ18L | **TDI** | DQ7L | DQ2L | DQ2R | DQ7R | **TCK** | DQ18R | DQ22R | A14R | **A16R** |
| **N** | DQO24L | DQ20L | DQ8L | DQ6L | DQ5L | DQ3L | DQ0L | DQ0R | DQ3R | DQ5R | DQ6R | DQ8R | DQ20R | DQ24R |
| **P** | DQ23L | DQ21L | TDO | VSSQ | DQ4L | VDDQ | DQ1L | DQ1R | VDDQ | DQ4R | VSSQ | TMS | DQ21R | DQ23R |

## Selection Guide

| | CY7C0851V25/CY7C0852V25 -100 |
|---|---|
| $f_{MAX}$ (MHz) | 100 |
| Max. Access Time (ns) (Clock to Data) | 5 |
| Typical Operating Current $I_{CC}$ (mA) | 150 |
| Typical Standby Current for $I_{SB1}$ (mA) (Both Ports TTL Level) | |
| Typical Standby Current for $I_{SB3}$ (mA) (Both Ports CMOS Level) | 10 |

## Pin Definitions

| Left Port | Right Port | Description |
|---|---|---|
| $A_{0L}$–$A_{16L}$ | $A_{0R}$–$A_{16R}$ | Address Inputs. |
| $\overline{ADS}_L$ | $\overline{ADS}_R$ | Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW to assert the part using the externally supplied address on Address Pins and to load this address into the Burst Address Counter. |
| $\overline{CE0}_L$ | $\overline{CE0}_R$ | Active Low Chip Enable Input. |
| $CE1_L$ | $CE1_R$ | Active High Chip Enable Input. |
| $CLK_L$ | $CLK_R$ | Clock Signal. Maximum clock input rate is $f_{MAX}$. |
| $\overline{CNTEN}_L$ | $\overline{CNTEN}_R$ | Counter Enable Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. Increment is disabled if ADS or CNTRST are asserted LOW. |
| $\overline{CNTRST}_L$ | $\overline{CNTRST}_R$ | Counter Reset Input. Asserting this signal LOW resets to zero the unmasked portion of the burst address counter of its respective port. CNTRST is not disabled by asserting ADS or CNTEN. |
| CNT/$\overline{MSK}_L$ | CNT/$\overline{MSK}_R$ | Address Counter Mask Register Enable Input. Asserting this signal LOW enables the access to the mask register. When tied HIGH the mask register is not accessible and the address counter operations are enabled based on the status of the counter control signals. |
| $DQ_{0L}$–$DQ_{35L}$ | $DQ_{0R}$–$DQ_{35R}$ | Data Bus Input/Output. |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable Input. This asynchronous signal must be asserted LOW to enable the DQ data pins during read operations. |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Mailbox Interrupt Flag Output. Mailbox permits communications between ports. The upper two memory locations can be used for message passing. $INT_L$ is asserted LOW when right port writes to the mailbox location of left port and vice versa. Interrupt to a port is deasserted HIGH when it reads the contents of its mailbox. |
| $\overline{CNTINT}_L$ | $\overline{CNTINT}_R$ | Counter Interrupt Output. This pin is asserted LOW when the unmasked portion of the counter is incremented to all “1s.” |
| R/$\overline{W}_L$ | R/$\overline{W}_R$ | Read/Write Enable Input. Assert this pin LOW to write to, or HIGH to read from the dual-port memory array. |
| $\overline{B}_{0L}$–$\overline{B}_{3L}$ | $\overline{B}_{0L}$–$\overline{B}_{3L}$ | Byte Select Inputs. Asserting these signals enables read and write operations to the corresponding bytes of the memory array. |
| $\overline{MRST}$ | | Master Reset Input. $\overline{MRST}$ is an asynchronous input and affects both ports. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A MRST operation is required at power-up. |
| TMS | | JTAG Test Mode Select Input. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK. |
| TDI | | JTAG Test Data Input. Data on the TDI input will be shifted serially into selected registers. |
| TCK | | JTAG Test Clock Input. |
| TDO | | JTAG Test Data Output. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP. |
| $V_{SS}$, $V_{SSA}$, $V_{SSQ}$ | | Ground Inputs (A: for address lines, Q: for data lines). |
| $V_{DD}$, $V_{DDA}$, $V_{DDQ}$ | | Power Inputs (A: for address lines, Q: for data lines). |

## Ordering Information

**64K x 36 (2 Meg) 2.5V Synchronous CY7C0851V25 Dual Port SRAM**

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 100 | CY7C0851V25-100BBC | BB172 | 172-Ball Grid Array (BGA) | Commercial |

**128K x 36 (4 Meg) 2.5V Synchronous CY7C0852V25 Dual Port SRAM**

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 100 | CY7C0852V25-100BBC | BB172 | 172-Ball Grid Array (BGA) | Commercial |
| | CY7C0852V25-100BBI | BB172 | 172-Ball Grid Array (BGA) | Industrial |

Shaded areas contain advanced information

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## Package Diagram

**172-Ball FBGA BB172**