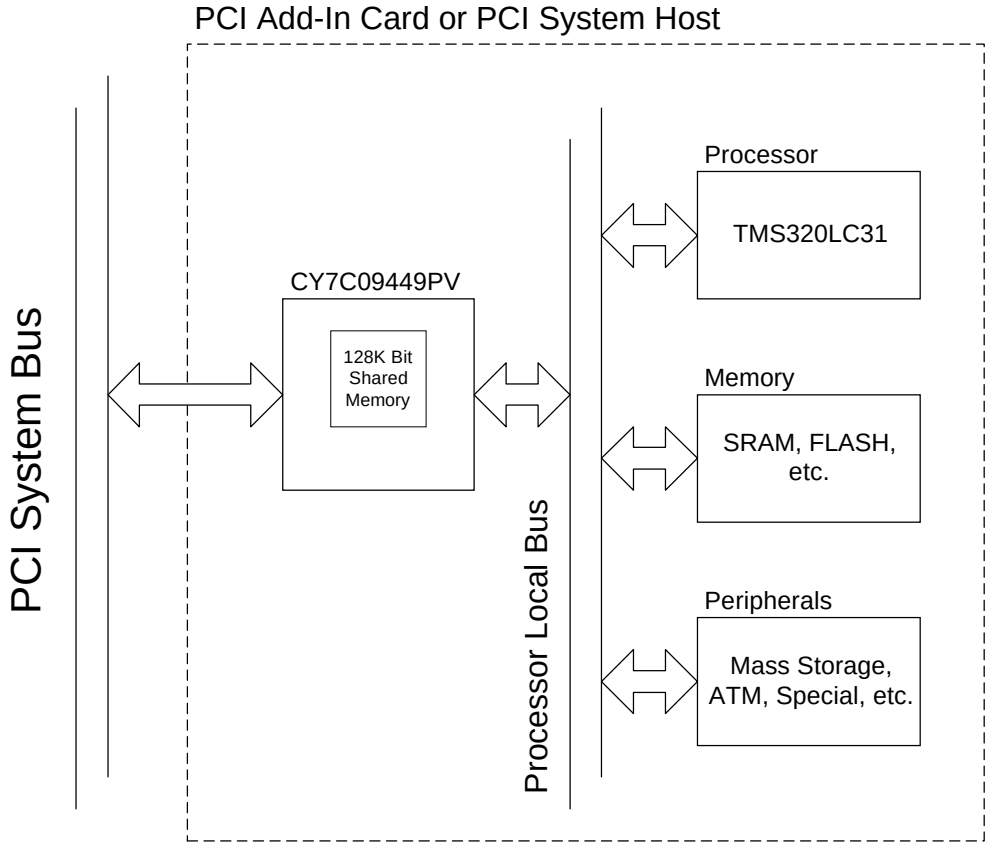
CY7C09449PV/TMS320LC31 Interconnection

Overview

The CY7C09449PV interfaces directly to the TI TMS320LC31 Digital Signal Processor. The interface described in this application note connects a 32-bit, 40-MHz TMS320LC31 to the CY7C09449PV.

System Block Diagram

The CY7C09449PV connects the primary bus of a TMS320LC31 to the PCI system bus.



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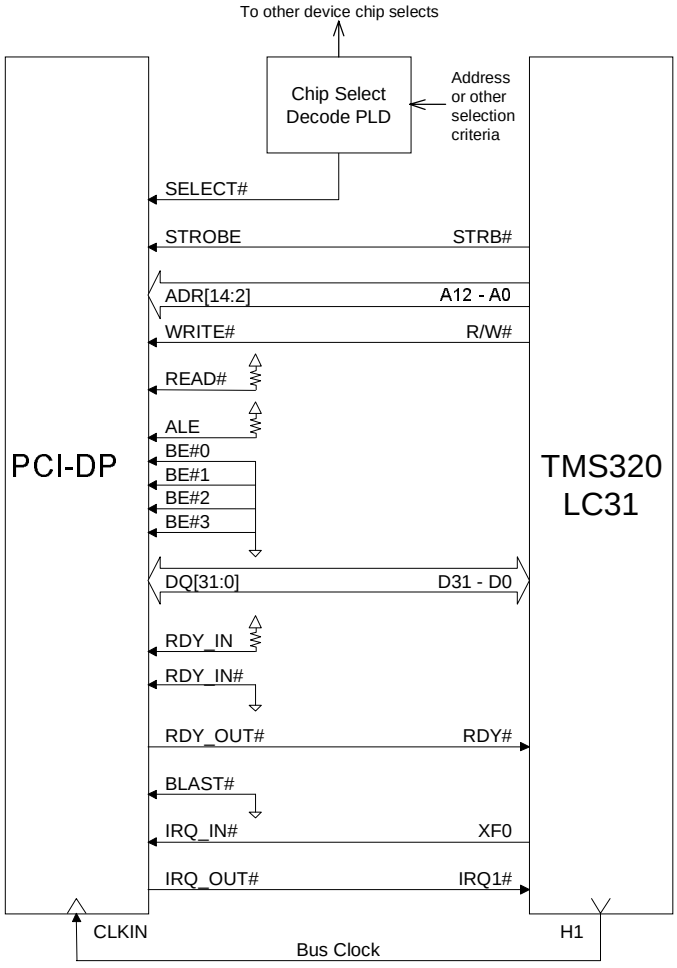
Wiring Diagram

Wiring the CY7C09449PV to the TMS320LC31 is simple. A programmable logic device (PLD) is used to generate the chip select for the CY7C09449PV. This PLD may contain chip select decoding for other devices in the TMS320LC31 system. The interrupt connections in the diagram are not required for the bus interface; they are only included for illustrative purposes.



CY7C09449PV Configuration Programming

The CY7C09449PV Local Bus Configuration register must be programmed to support the TMS320LC31 external bus architecture. This may be loaded either at power-up from a PROM via the I2C interface or from the PCI system host. The value for the register is:

LBUSCFG = 0x010A91

Timing

This section includes timing diagrams for the processor bus interface between the TMS320LC31 and the CY7C09449PV. The interface is based on a 40-MHz TMS320LC31 component.

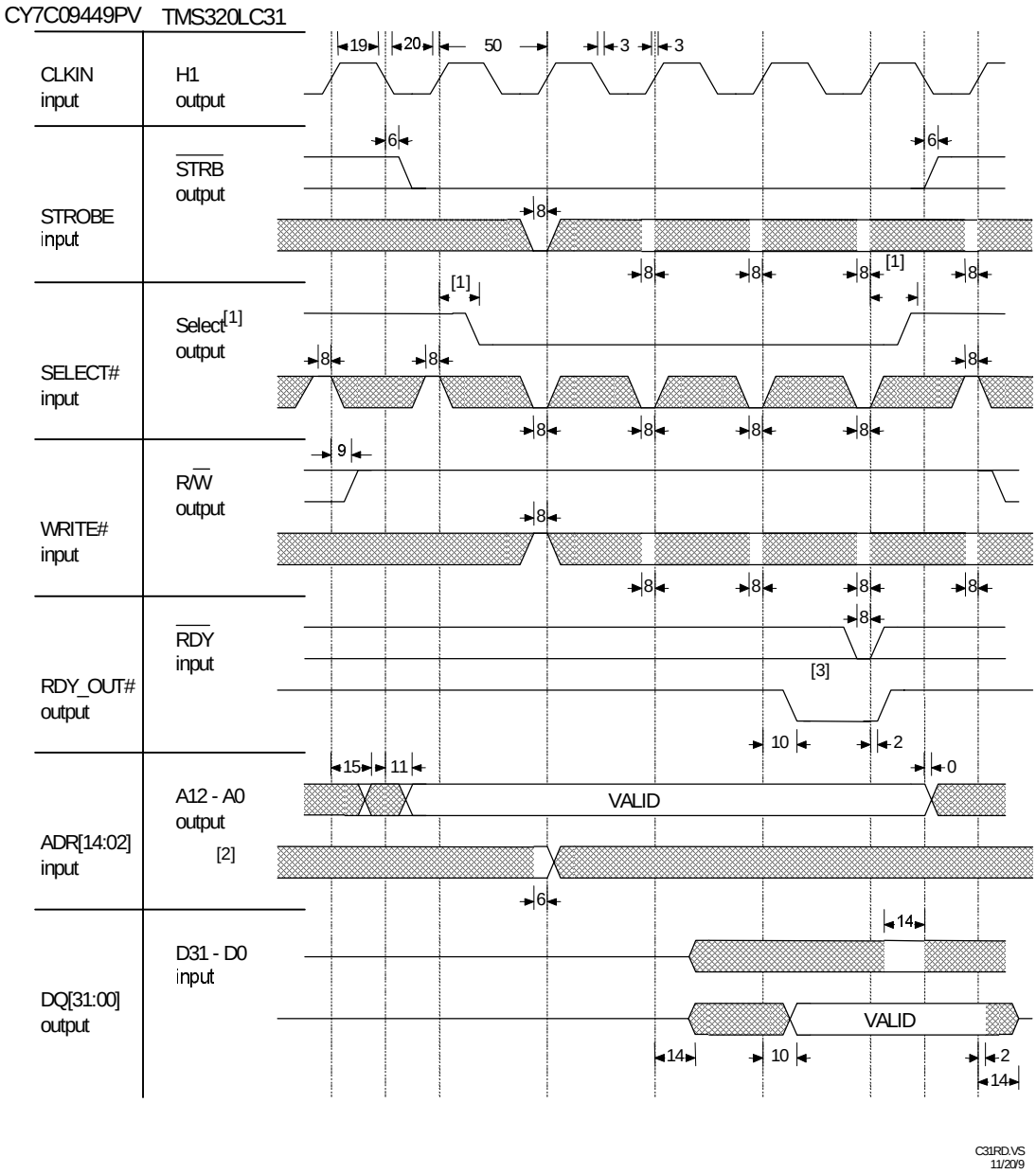
In this application note, the chip select to the CY7C09449PV is generated by circuits other than the TMS320LC31. For example, a 7.5-ns programmable logic device (PLD) could be used to decode the processor's address lines to generate a select to the CY7C09449PV. The decoded signal should be clocked on the rising edge of the H1 clock before presentation to the CY7C09449PV $\overline{\text{SELECT}}$ input. Chip selects for other devices in the TMS320LC31 system could be generated by this PLD.

In order to support back-to-back operations, the $\overline{\text{SELECT}}$ input to the CY7C09449PV must deactivate for at least one cycle after the $\overline{\text{RDY\_OUT}}$ output is asserted. This function can be performed by the PLD. If back-to-back cycles are not to occur and a faster decoding is desired, one choice is to use the most significant address bit of the TMS320LC31 as a chip select. This would speed the access by one cycle.

Explanation and key to reading timing diagrams --

- Timing data are taken from the TMS320LC31 and CY7C09449PV specifications; see References.
- Timing numbers are in nanoseconds and worst case commercial environment.
- Clock pulse widths and clock cycle time are minimum values.
- All input hold times are 0 ns, minimum; if relevant, minimum data hold times for outputs are shown.
- Where relevant, maximum data valid output timing is shown to support set-up calculations.
- Where relevant, minimum data input set-up timing is shown to support set-up calculations.

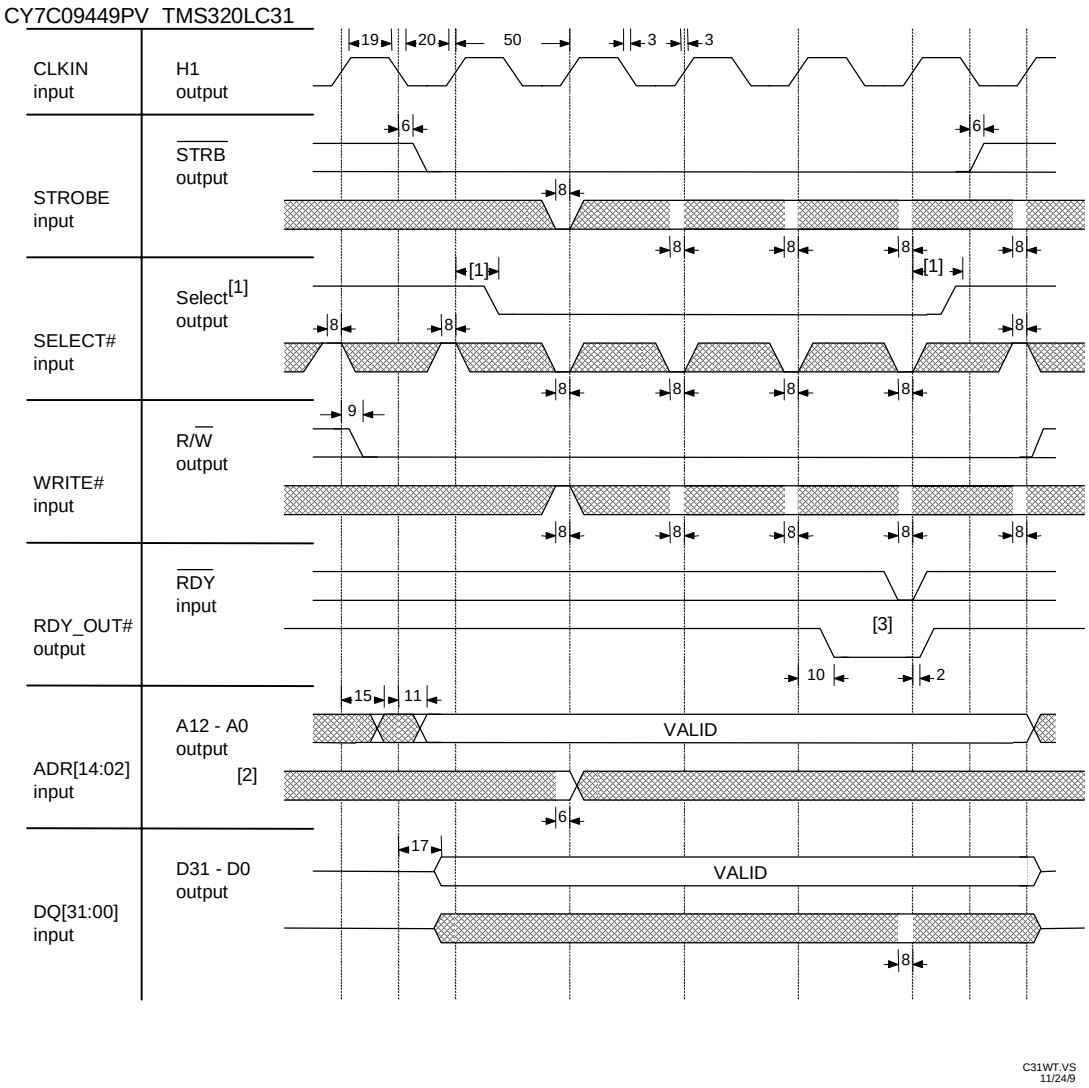
The following is the timing diagram for TMS320LC31 read access to the CY7C09449PV.



Notes

1. The chip select to the CY7C09449PV is application dependent. It may come from several sources. In this timing diagram, it is to be clocked from an address decode. A faster method is discussed in the text.
2. The address change leading into the current cycle may occur on a rising or falling edge. If the immediately prior cycle was a write access, the TM320LC31 address will change on the clock's rising edge. If the immediately prior cycle was a read access, the TM320LC31 address will change on the clock's falling edge.
3. Wait states occur when the CYC7C09449PV delays assertion of $\overline{\text{RDY\_OUT}}$ to later cycles. Zero wait states are illustrated here.

The following is the timing diagram for TMS320LC31 write access to the CY7C09449PV.



From the two diagrams, timing margin for a TMS320LC31 to CY7C09449PV bus interconnect can be extracted. The timing shown is worst case commercial environment. Loading beyond the specification, signal line lengths, and other environmental constraints beyond commercial worst case can use this margin and still comply to specification. Some timings will have margin spanning more than one cycle. This is because in some cycles the signal is not used but the output signal remains valid across cycles. Timing margin is listed here in terms of input set-up times.

Read and Write Access to the CY7C09449PV

CY7C09449PV STROBE input set-up, first cycle	56 ns
CY7C09449PV STROBE input set-up, last cycle	6 ns
CY7C09449PV $\overline{\text{SELECT}}$ input set-up (assumes an 8 ns PLD)	34 ns
CY7C09449PV $\overline{\text{WRITE}}$ input set-up, first cycle	83 ns
TMS320LC31 $\overline{\text{RDY}}$ input set-up	32 ns
CY7C09449PV ADR[14:02] input set-up	53 ns

Data Bus for Read Access to the CY7C09449PV

TMS320LC31 D31-D0 input set-up	45 ns

Data Bus for Write Access to the CY7C09449PV

CY7C09449PV DQ[31:00] input set-up	195 ns

Performance

Throughput between the TMS320LC31 and the shared memory of the CY7C09449PV is 16 MB/s. Throughput can be increased to 20 MB/s if an address line is used directly for the chip select; see the Timing section for more discussion. Access to the CY7C09449PV Operation Registers or FIFO may incur wait states.

CY7C09449PV mastered DMA bursting from the CY7C09449PV shared memory to system host memory has been measured to be approximately 120 MB/s on an unloaded PCI bus.

References

Specifications used as input to this application note are listed below.

PCI-DP CY7C09449PV data sheet, 128K Bit Dual-Port SRAM with PCI Bus Controller, Cypress Semiconductor Corporation.

TMS320C3x User's Guide, revision L, July 1997, Literature Number SPRU031E, Texas Instruments Incorporated.

TMS320C31, TMS320LC31 Digital Signal Processors, Revised July 1997, Literature Number SPRS035A, Texas Instruments Incorporated.

Additional component literature may be downloaded from web sites at Cypress Semiconductor and Texas Instruments. The two main sites are listed below.

Cypress Multi-Port RAMs

- http://www.cypress.com/dualport/index.html

TI DSP Products

- http://www.ti.com/sc/docs/products/dsp/index.htm

The PCI 2.2 specification may be purchased from the PCI Special Interest Group (SIG) or other sources. The web site for the PCI SIG is:

- http://www.pcisig.com/

A related Cypress application note is listed below.

- PCI-DP: Programming Bus Master DMA Transfers