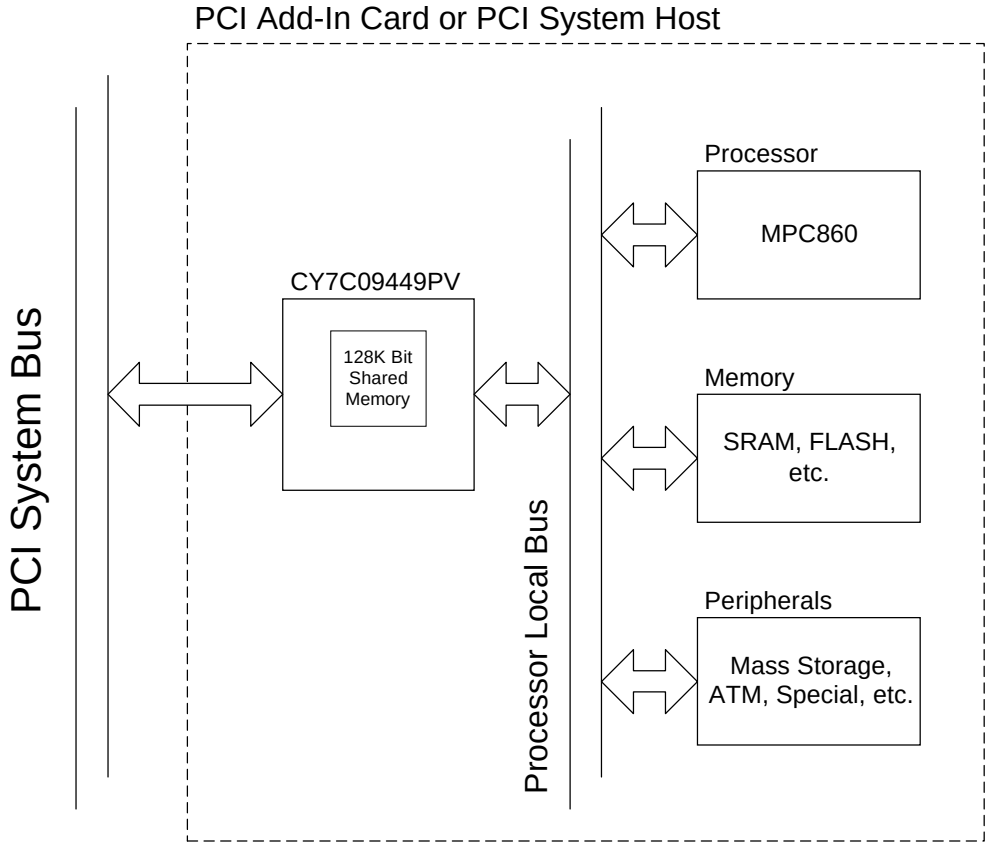
CY7C09449PV/MPC860 Interconnection

Overview

The CY7C09449PV interfaces directly to the Motorola MPC860 PowerQUICC processor. The interface described in this application note connects a 32-bit, 40-MHz MPC860 to the CY7C09449PV.

System Block Diagram

The CY7C09449PV connects the MPC860 to the PCI system bus.



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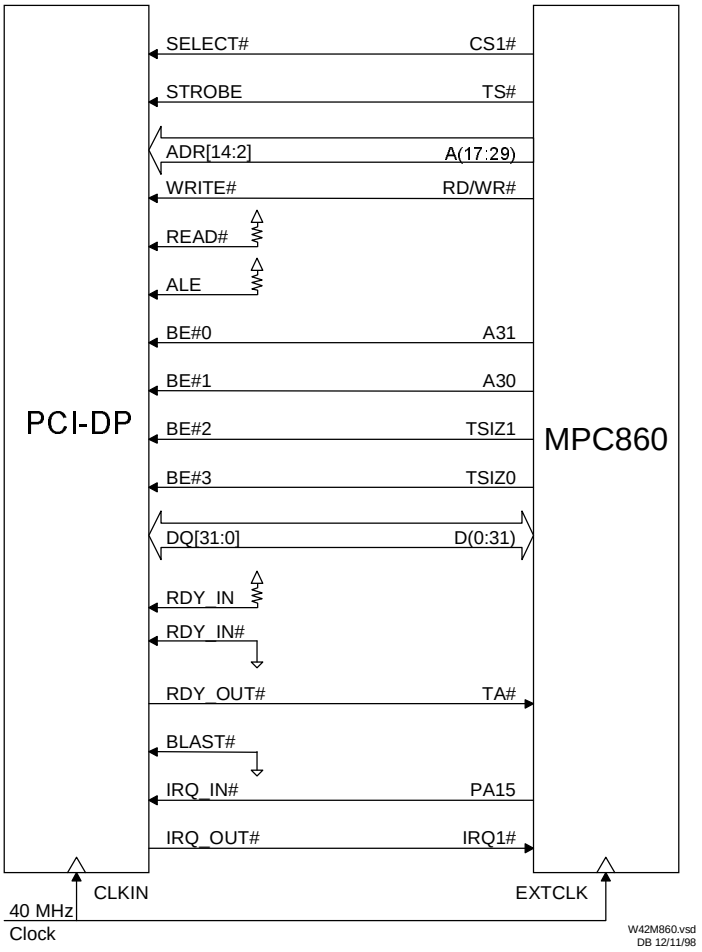
Wiring Diagram

Wiring the CY7C09449PV to the MPC860 is simple. The interrupt connections in the diagram are not required for the bus interface; they are only included for illustrative purposes. Note that the MPC860 signal naming convention is that least significant bits have the higher bit numbers. For instance, the least significant data bit of a 32-bit bus is D31 and the most significant bit is D0. The CY7C09449PV signal naming convention is consistent with that of the PCI bus and other little endian conventions. To maintain proper significance in bit ordering, the signals are connected as shown in the diagram. For example the MPC860 data bit 31 is connected to the CY7C09449PV data bit 0. The addresses are wired in the same way.



CY7C09449PV Configuration Programming

The CY7C09449PV Local Bus Configuration register must be programmed to support the MPC860 external bus architecture. This includes a setting to implement byte enable decoding for the big endian MPC860 format. The decoding is performed on the CY7C09449PV $\overline{BE}$ lines. The configuration register may be loaded either at power-up from a PROM via the I2C interface or from the PCI system host. The value for the register is:

LBUSCFG = 0x010B50

The value given for the LBUSCFG is the default setting for the CY7C09449PV. Therefore, if no other power-up loading via the I2C interface PROM is needed, then the configuration PROM may be eliminated.

Timing

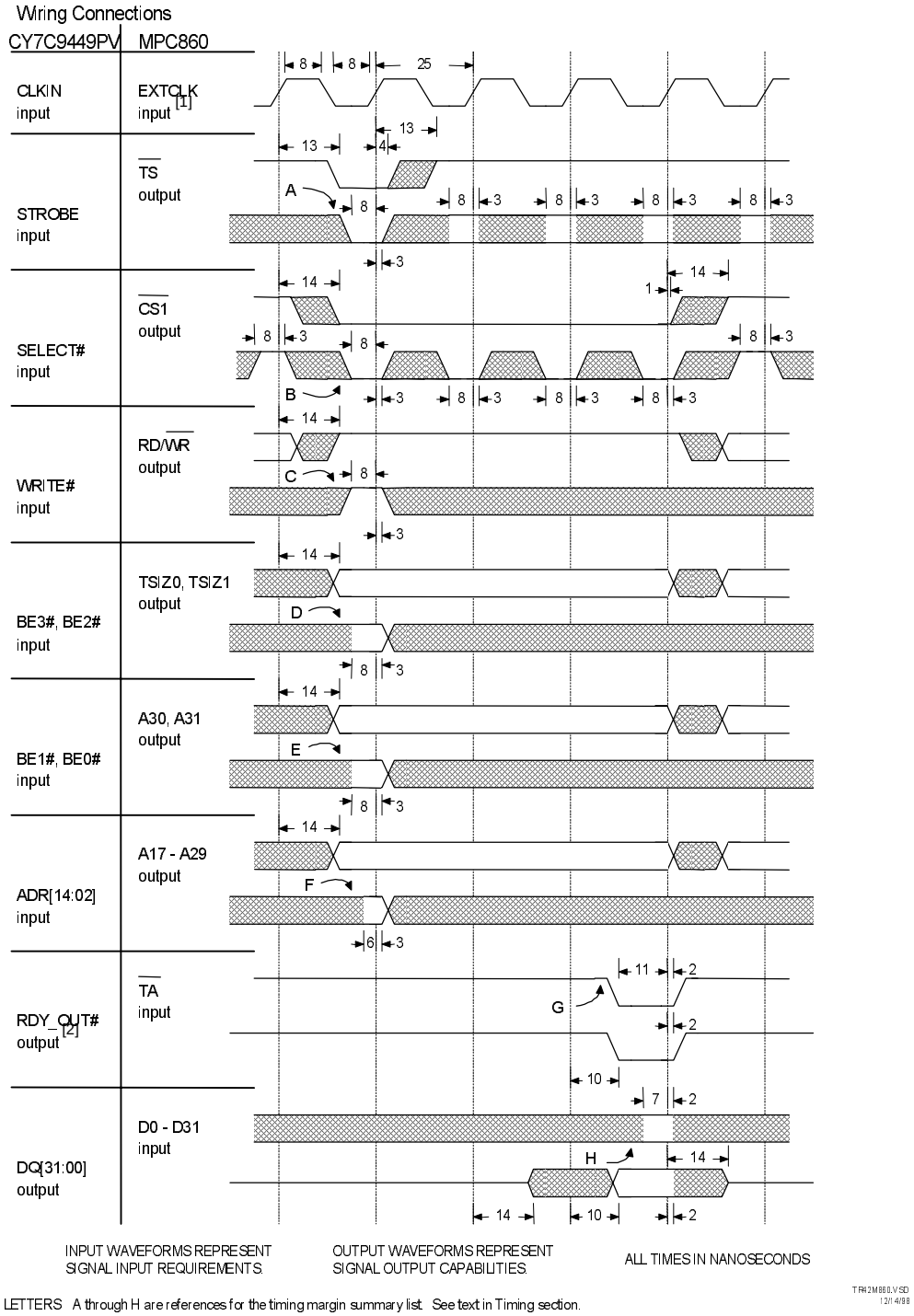
This section includes timing diagrams for the processor bus interface between the MPC860 and the CY7C09449PV. The interface is based on a 40-MHz MPC860 component.

The timing diagrams show waveforms organized in pairs. One member of the pair is the signal name of the CY7C09449PV and the other member is signal name of the MPC860. As shown in the Wiring Diagram, these signals are directly wired together. The intention of the timing diagrams is to show that the two components have compatible timing. The waveforms for the output signals illustrate the signals' characteristics and the waveforms for the input signals illustrate the signals' input requirements. In this way, both component specifications can be viewed together. After the diagrams, a summary of timing margin for each signal pair is provided.

Explanation and key to reading timing diagrams --

- Timing data are taken from the MPC860 and CY7C09449PV specifications; see References.
- Timing numbers are in nanoseconds and worst case commercial environment.
- Clock pulse widths and clock cycle time are minimum values.
- Where relevant, maximum data valid output timing is shown to support set-up calculations.
- Output waveform timing represents signal output characteristics and capabilities.
- Where relevant, minimum data input set-up timing is shown to support set-up calculations.
- Input waveform timing represents signal input requirements.

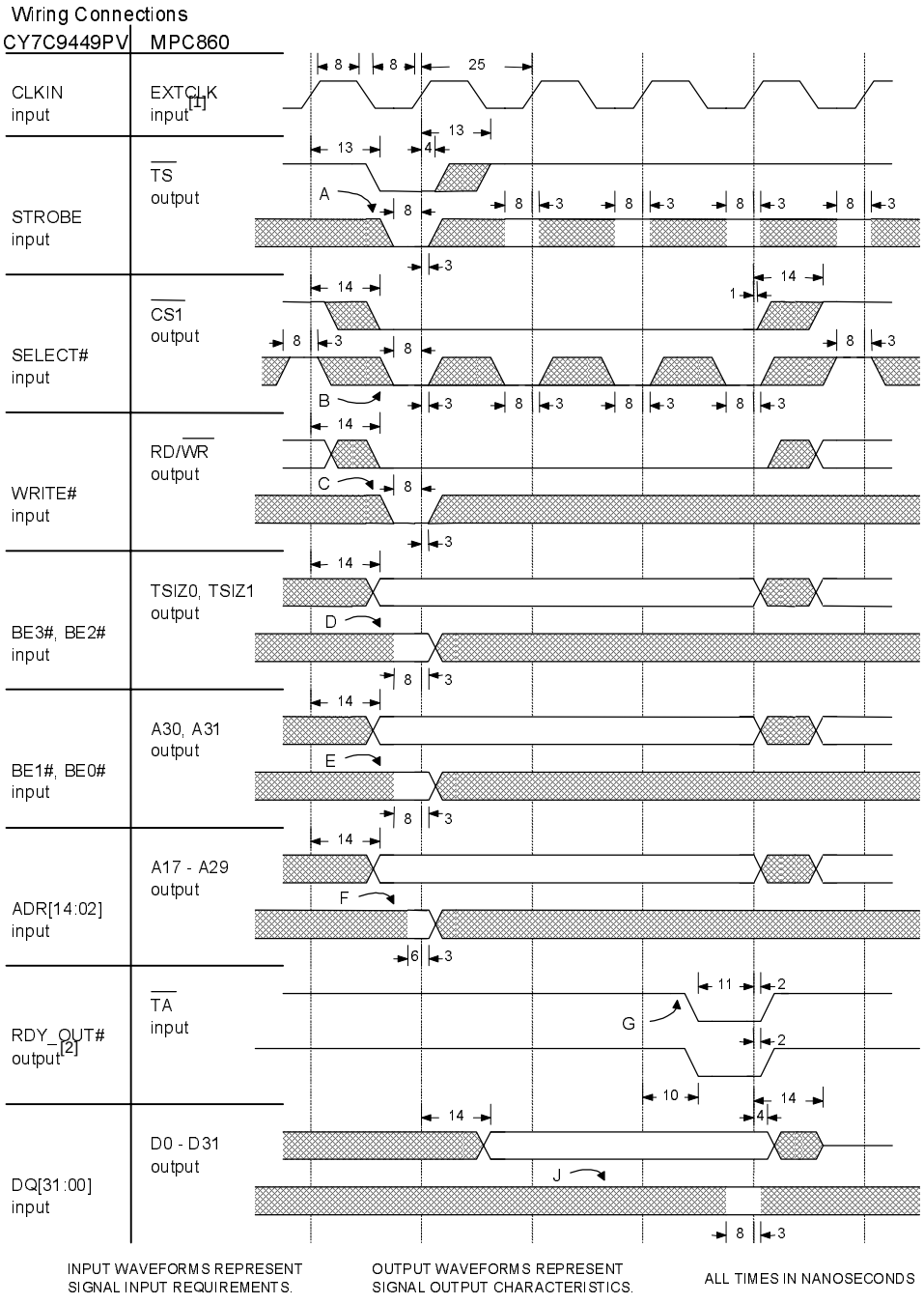
The following is the timing diagram for MPC860 read access to the CY7C09449PV.



Notes

1. MPC860 bus interface timing is related to its CLKOUT signal output. A phase-locked loop within the MPC860 keeps the phase skew between its EXTCLK input and CLKOUT output at ±0.9 ns. That value is factored into this timing diagram. The minimum high and low times for the CY7C09449PV CLKIN input are shown.
2. Wait states occur when the CY7C09449PV delays assertion of $\overline{\text{RDY\_OUT}}$ to later cycles. Zero wait states are illustrated here.

The following is the timing diagram for MPC860 write access to the CY7C09449PV.



LETTERS A through G and J are references for the timing margin summary list. See text in Timing section.

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From the two diagrams, timing margin for a MPC860 to CY7C09449PV bus interconnect can be extracted. The timing shown is worst case commercial environment. Loading beyond the specification, signal line lengths, and other environmental constraints beyond commercial worst case can use this margin and maintain a compatible interface. Identifying letters are shown on the two timing diagrams.

Read and Write Access to the CY7C09449PV

A	CY7C09449PV STROBE input set-up	4 ns
B	CY7C09449PV $\overline{\text{SELECT}}$ input set-up	3 ns
C	CY7C09449PV $\overline{\text{WRITE}}$ input set-up	3 ns
D	CY7C09449PV $\overline{\text{BE3}}$, $\overline{\text{BE2}}$ input set-up	3 ns
E	CY7C09449PV $\overline{\text{BE1}}$, $\overline{\text{BE0}}$ input set-up	3 ns
F	CY7C09449PV ADR[14:02] input set-up	5 ns
G	MPC860 $\overline{\text{TA}}$ input set-up	4 ns

Data Bus for Read Access to the CY7C09449PV

H	MPC860 D0–D31 input set-up	8 ns

Data Bus for Write Access to the CY7C09449PV

J	CY7C09449PV DQ[31:00] input set-up (output stable across cycles)	53 ns

Performance

Throughput between the MPC860 and the shared memory of the CY7C09449PV is 32 MB/s. Access to the CY7C09449PV Operation Registers or FIFO may incur wait states during concurrent accesses by the PCI bus.

CY7C09449PV mastered DMA bursting from the CY7C09449PV shared memory to system host memory has been measured to be approximately 120 MB/s on an unloaded PCI bus.

References

Specifications used by this application note are listed below.

PCI-DP CY7C09449PV data sheet, 128K Bit Dual-Port SRAM with PCI Bus Controller, Cypress Semiconductor Corporation.

MPC860 PowerQUICC User's Guide, Revision 1, July 1998, MPC860UM/AD, Motorola, Incorporated.

Errata to MPC860 PowerQUICC User's Guide Rev 1, September 30, 1998, Motorola, Incorporated.

MPC860 Rev 1.1 Specification, Section 21 MPC Electrical Characteristics, Motorola Semiconductor Products Sector.

Additional component literature may be downloaded from web sites at Cypress Semiconductor and Motorola. The two main sites are listed below.

Cypress Multi-Port RAMs

- http://www.cypress.com/dualport/index.html

Motorola Netcomm Publications

- http://www.mot.com/SPS/RISC/netcomm/docs/pubs/

The PCI 2.2 specification may be purchased from the PCI Special Interest Group (SIG) or other sources. The web site for the PCI SIG is:

- http://www.pcisig.com/

A related Cypress application note is listed below.

- PCI-DP: Programming Bus Master DMA Transfers