Understanding The FLEx36 Dual-Port SRAMs

Introduction

Dual-port memory devices are used in many different applications to communicate and share data between two systems.

The Cypress FLEx36 family of dual-port SRAMs offers 36-bit wide data buses on both ports with a number of features that are new to dual-port architectures. Designers using 32-bit interface devices and data streams are now able to greatly simplify their designs as well as eliminate multiple devices using the FLEx36 and as a result reduce the total cost of their systems.

This family offers both synchronous and asynchronous devices. The CY7C056V and the CY7C057V are the asynchronous devices with densities of half a megabit (16k x 36) and one megabit (32k x 36) respectively. The CY7C09569V and the CY7C09579V are the synchronous versions.

All devices in this family operate on 3.3V power with performance of up to 100 MHz for the sync parts. New features included in this family are: bus matching, which allows the user to select one of three bus sizes on the right port; burst counter read-back feature, which allows the user to read the contents of the internal address counters over the I/O lines; and the byte select feature which allows read/write control of the four bytes of data from the left port.

This application note discusses these new features in detail and provides examples of interfacing these devices to the Power Quicc processor and a TI DSP processor.

Bus Matching in the FLEx36 Family

The FLEx36 family of dual-port SRAMs offers a bus matching feature on the right port. This feature allows the designer to transfer the four bytes (9 bits/byte) of data in the standard x36 format as well as x18 and x9 formats. This capability makes it easy to interface between buses of varying sizes. Systems using 32-bit processors can now easily communicate with devices having lower bus widths without external logic.

In the bus matching mode, a number of control inputs are provided to enable the user to select the bus size as well as the order in which data is driven on the I/O pins. Bus matching is implemented in a slightly different way in the sync versus the async devices. The differences will be covered in detail in the following sections.

Bus Matching in the Sync Device

As mentioned above, the right port of the FLEx36 family of dual-port SRAMs can be configured to operate in three bus size formats. These formats are selected using the control inputs BM (Bus Mode), SIZE (Bus Size) and BE (Big Endian).

The BM and SIZE Control Inputs

The BM and SIZE inputs in the sync devices are used to select the bus width at which the right port will operate, i.e., x36, x18, or x9. *Figure 1* shows the bus matching block diagram for the sync devices.

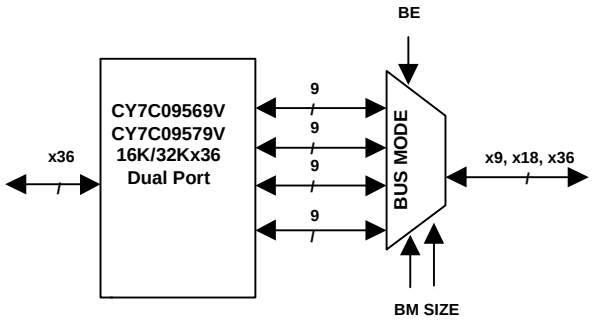

Figure 1. Sync Device Bus Match Operation Diagram

The mapping of the bytes, words (18 bits), and long-words (36 bits) onto the I/O pins is shown in *Table 1*.

In the x9 format, the four bytes of data are transferred on I/O_{0-8} in four clock cycles, and in the x18 format the two words of data are transferred on I/O_{0-17} in two clock cycles. In the x36 format all of the 36 bits (long-word) will be transferred at once on the I/O pins in a single clock cycle.

Table 1. Sync Device Right Port Configuration

BM	SIZE	Configuration	I/O Pins Used
0	0	x36	I/O_{0R-35R}
1	0	x18	I/O_{0R-17R}
1	1	x9	I/O_{0R-8R}

The BE Control Input

The BE input (Big Endian) is used to select between the Big Endian and the Little Endian data sequencing formats. In the Big Endian case (BE = 1) the data will be transferred on the I/O pins, from the most to the least significant Byte or Word. In the Little Endian configuration (BE = 0) the opposite will take place. This is accomplished internally with a two-bit sub-counter that counts down when BE = 1 and counts up when BE = 0. These two bits called WA and BA, effectively function as the LSBs of the address bus. We will see in a later section that, when reading back the internal address counter, these two bits will be read out in addition to the counter content.

Table 2 shows in detail the sequence in which the bytes (in the x9 format) and the words (in the x18 format) are transferred.

Table 2. Sync Device Right Port Operation

Configuration	BE	Data on 1st Cycle	Data on 2nd Cycle	Data on 3rd Cycle	Data on 4th Cycle
x18	0	$DQ_{0R–17R}$	$DQ_{18R–35R}$	-	-
x18	1	$DQ_{18R–35R}$	$DQ_{0R–17R}$	-	-
x9	0	$DQ_{0R–8R}$	$DQ_{9R–17R}$	$DQ_{18R–26R}$	$DQ_{27R–35R}$
x9	1	$DQ_{27R–35R}$	$DQ_{18R–26R}$	$DQ_{9R–17R}$	$DQ_{0R–8R}$

Bus Matching in the Async Devices

Bus matching in the async devices differs from the sync devices only in the sequencing control of the byte and word transfers. The async devices provide the BM and SIZE inputs but, instead of the BE input, they provide inputs for the word and byte address bits referred to as WA and BA respectively. *Figure 2* shows the bus matching block diagram for the async devices.

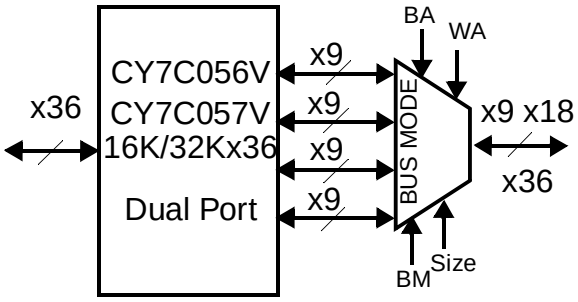

Figure 2. Async Device Bus Match Operation Diagram

The BM and SIZE Control Inputs

The BM and SIZE inputs in the async devices are used the same way as in the sync devices. The mapping of the data onto the I/O pins is done in the same way as well. Refer to *Table 1* above.

The WA and BA Control Inputs

Data sequencing in the async devices is controlled in a slightly different way. Instead of the BE pin, which allows a fixed data sequence (most to least or least to most), the async devices have a pair of control inputs (WA and BA) to individually address the bytes or words within the 36-bit long-word. These inputs allow the designer to transfer the bytes or words in any desired sequence. The WA and BA inputs are essentially extensions of the right port address bus and exhibit the same timing specification.

In the x18 format, the 36 bits of data is broken up into two words. This means only one bit (WA) is needed to select between them. The BA input in this case will be a “don't care.”

In the x9 format on the other hand, both bits are needed to select between the four bytes of the 36-bit data. Refer to *Table 3* for the data transfer configurations.

The Burst Counter

The sync dual-ports have a built-in burst counter on each of the two ports of the device. The counter is capable of addressing the whole memory array and will loop back to the start. It is also possible to interleave memory accesses between the internal counter address and the externally supplied address using the control inputs $\overline{ADS}$ and $\overline{CNTEN}$.

The loading and incrementing of the address counter takes place at the rising edge of a port's clock and is controlled by the above two signals. *Table 4* shows the truth table for the counter operation.

Table 3. Async Device Right Port Operation

Configuration	WA	BA	Data Accessed	I/O Pins Used
x36	X	X	$DQ_{0–35}$	$I/O_{0–35}$
x18	0	X	$DQ_{0–17}$	$I/O_{0–17}$
x18	1	X	$DQ_{18–35}$	$I/O_{0–17}$
x9	0	0	$DQ_{0–8}$	$I/O_{0–8}$
x9	0	1	$DQ_{9–17}$	$I/O_{0–8}$
x9	1	0	$DQ_{18–26}$	$I/O_{0–8}$
x9	1	1	$DQ_{27–35}$	$I/O_{0–8}$

Table 4. Address Counter Control Operation

Address	Previous Address	CLK	$\overline{OE}$	R/$\overline{W}$	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	Mode	Operation
X	X	⎍	X	X	X	X	L	Reset	Counter Reset
A_n	X	⎍	X	X	L	L	H	Load	Address Load into Counter
A_n	A_n	⎍	L	H	L	H	H	Hold + Read	External Address Blocked - Counter Address Readout
X	A_n	⎍	X	X	H	H	H	Hold	External Address Blocked - Counter Disabled
X	A_n	⎍	X	X	H	L	H	Increment	Counter Increment

Read-Back of Internal Address Counters

The FLEx36 family of dual-port SRAMs allows the user to read back the value of the internal address counter over the data I/O pins (*Figure 3*). Because the bus matching feature is not available on the left port of the device, reading back the contents of the left port address counter is a straight forward operation compared to reading the right port address counter. The following sections will discuss the details of accessing the internal counters of both ports of the device.

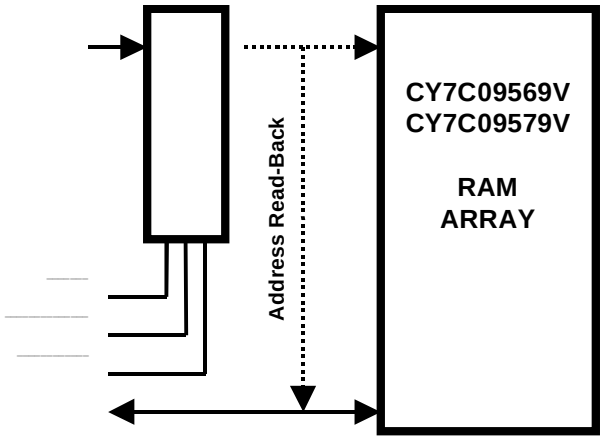

Figure 3. SYNC Device Counter Operation

Read-Back of the Left Port Address Counter

When reading back the left port address counter, the 15 address bits of the 32K device are simply enabled onto pins $I/O_{3–17}$ with the MSB (A_{14}) mapped to I/O_{17} and the LSB (A_0) mapped to I/O_3. For the 16K device, the 14 bits of address are enabled onto $I/O_{3–16}$ with the MSB (A_{13}) mapped to I/O_{16} and the LSB (A_0) mapped to I/O_3. Reading the address will take place in one clock cycle. Note that $I/O_{0–2}$ are not used here. *Table 5* shows the details of the mapping

Read-Back of the Right Port Address Counter

When reading back the right port address counter, the mapping of the counter bits depends on the bus matching format in use.

In the x36 format, the read back of the address counter is exactly the same as the left port read back (see the previous section).

In the x18 format, the address counter bits will be read out plus the Word Address bit (WA). Therefore, in the 32K deep device a total of 16 bits will be read out. Reading back this address requires only a single clock cycle and the bits are mapped as follows: address bits $A_{0–14}$ are enabled onto $I/O_{3–17}$, and the WA bit is mapped onto I/O_2. Note that $I/O_{0–1}$ are not used here and $I/O_{18–35}$ are not available.

If the x9 format is selected, two extra bits will be read out in addition to the 15 bits (32K deep device) of the address counter itself for a total of 17 bits. The two additional bits are the Word and Byte address bits (WA and BA) from the internal sub-counter mentioned earlier. WA and BA will represent the LSBs of the address bus.

Reading back the address in the x9 mode will require two clock cycles because only 9 I/O pins are available and we have 15 address bits. The MSBs of the address will be read out in the first cycle and the LSBs in the second cycle. The mapping will be as follows:

In the first clock cycle, address bits $A_{6–14}$ of the burst counter are enabled onto $I/O_{0–8}$. In the second clock cycle, address bits $A_{0–5}$ are enabled onto $I/O_{3–8}$, the WA bit is mapped onto I/O_2, and the BA bit onto I/O_1. I/O_0 will be unused. *Table 5* shows the details of the mapping and *Figure 4* and *Figure 5* show a visual diagram.

Table 5. Readout of Internal Address Counter for the 32K Device

Configuration	Address on 1st Cycle	I/O Pins used on 1st Cycle	Address on 2nd Cycle	I/O Pins used on 2nd Cycle
Left Port x36	A_{0L-14L}	I/O_{3L-17L}	-	-
Right Port x36	A_{0R-14R}	I/O_{3R-17R}	-	-
Right Port x18	WA, A_{0R-14R}	I/O_{2R-17R}	-	-
Right Port x9	A_{6R-14R}	I/O_{0R-8R}	BA, WA, A_{0R-5R}	I/O_{1R-8R}

Pins used	IO_{17} ..... IO_3	IO_2	IO_1	IO_0
X36 mode	A_{14} ..... A_0	X	X	X
X18 mode	A_{14} ..... A_0	WA	X	X
Pins used	IO_8 ..... IO_3	IO_2	IO_1	IO_0
X9 mode(1st cycle)	A_{14} ..... A_9	A_8	A_7	A_6
X9 mode(2nd cycle)	A_5 ..... A_0	WA	BA	X

Figure 4. Burst Counter Read on the Right Port of a 32K Device

Pins used	IO_{17} IO_{16} ..... IO_3	IO_2	IO_1	IO_0
X36 mode	X A_{14} ..... A_0	X	X	X
X18 mode	X A_{14} ..... A_0	WA	X	X
Pins used	IO_8 IO_7 ..... IO_3	IO_2	IO_1	IO_0
X9 mode (1st cycle)	X A_{13} ..... A_9	A_8	A_7	A_6
X9 mode (2nd cycle)	A_5 ..... A_0	WA	BA	X

Figure 5. Burst Counter Read on the Right Port of a 16K Device

Byte Select Feature on the Left Port

Both the sync and the async devices offer the byte select feature on their left port. This feature is accessible using the four control pins $\overline{B0}$–$\overline{B3}$.

The byte select control pins enable the user to select which byte or bytes of the 36 bit long-word is written or read to/from the memory array. When a byte is deselected the corresponding I/O lines will be three-stated. For example when a read or write operation is taking place from the left port, and $\overline{B0}$ and $\overline{B1}$ are both LOW while $\overline{B2}$ and $\overline{B3}$ are both HIGH, the two least significant bytes will be written or read on I/O_{0-17} while the upper I/O pins will be three-stated.

Table 6 shows the truth table of the byte selection process.

Simultaneous Accesses in the Sync Devices

The sync devices, unlike the async versions, do not have built-in arbitration logic or the capability to signal a conflict between the two ports. If simultaneous accesses are expected to occur, the user will need to implement arbitration outside the device to detect and react to contention cases.

An access is considered simultaneous when the two port clocks occur within a period of time specified as t_{CCS}, which is the clock-to-clock set-up time specified in the data sheet. As long as the two port clocks are apart by more than t_{CCS} no contention will occur and the desired data will be obtained as expected.

The four possible address contention cases are: simultaneous reads, simultaneous writes, a write before a read, and a read before a write (separated by a time less than the t_{CCS} maximum).

In simultaneous reads, the true dual-ported memory cell architecture allows data to be accessed simultaneously on both ports of the device. In the FT mode, the data will be available t_{CD1} after the rising edge of the address clock and in the pipelined mode, the data will be available t_{CD2} after the first rising edge following the address clock (refer to the data sheet Timing Diagrams)

When writing simultaneously to the same location in memory, the resulting data will be undefined.

Table 6. Byte Select Control

Inputs				Outputs	
CE	**R/$\overline{W}$**	**OE**	**$\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$**	**I/O_0–I/O_{35}**	**Operation**
H	X	X	X	High Z	Deselected: Power-Down
X	X	X	All H	High Z	Deselected: Power-Down
L	L	X	H/L	Data In and High Z	Write to Selected Bytes Only
L	L	X	All L	Data In	Write to all Bytes
L	H	L	H/L	Data Out and High Z	Read Selected Bytes Only
L	H	L	All L	Data Out	Read All Bytes
X	X	H	X	High Z	Outputs Disabled

In the case of a write on one port followed by a read on the other within the t_{CCS} window, the write operation will proceed unobstructed and the read port will get the newly written data after a delay of t_{CWDD}. In other words, in the flow-through mode, the written data will be valid on the I/O pins of the read port, t_{CWDD} after the rising edge of the write port address clock (assuming that the read address was not modified). Prior to that time data will be undefined. In the pipelined mode the newly written data will appear at the read port after a delay of t_{CCS} (whatever it happens to be) plus one cycle of latency plus t_{CD2}.

In the case of a read on one port followed by a write on the other, the write operation will proceed unaffected. The read data, on the other hand, will be undefined on the read port due to the write operation occurring within the t_{CCCC} specified time. However, if the read data is sampled t_{CWDD} after the rising edge of the write clock, assuming the read address remained unchanged, the newly written data will be obtained on the read port. In pipelined mode data will be valid after 2 latency cycles plus t_{CD2} from the read clock rising edge at which address was strobed.

Application Examples

Interfacing the Async FLEx36 Dual-Port to the Power QUICC Microprocessor

This section describes how to interface the asynchronous FLEx36 devices to Motorola's MPC860 Power QUICC microprocessor. The MPC860 features a 32-bit PowerPC CPU core and a communications processor module that incorporates among other things, an Ethernet and an HDLC controller. This processor is used in communications and networking applications. The MPC860 has a built-in memory controller that allows a glueless interface to various types of external memories. Control signals such as $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$ are available to connect to external memories. The controller can be programmed to activate chip select outputs for various memory-mapped address spaces as well as to adjust the timing of the control signals to match the requirements of the memories in use. This is accomplished using a General Purpose Chip-select Machine (GPCM).

Figure 6 shows the connection between the MPC860 and the 32Kx36 asynchronous dual-port device. $\overline{CS1}$ from the memory controller is connected to $\overline{CE0}$ of the dual-port. The memory controller of the MPC860 provides eight $\overline{CS}$<7:0> outputs. Any one of them can be used except $\overline{CS0}$, which is dedicated to boot ROM address decoding. The $\overline{WE}$ signal from the controller is connected to the R/W input and the $\overline{OE}$ signal is connected to the $\overline{OE}$ input of the dual-port. $\overline{CS2}$ is connected to the $\overline{SEM}$ input and enables writing and reading the semaphore locations. The dual-port memory data bus is connected to the 32-bit data bus of the MPC860 as well as its parity bits DP<3:0>.

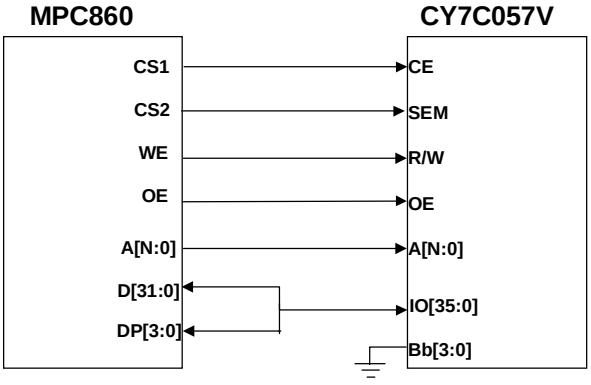

Figure 6. Async FLEx36 to MPC860 Interface

The MPC860 provides parity generation and checking for data transfers on the four bytes of data. Signal DP0 is the parity bit associated with byte0 (D0–D7), DP1 is associated with byte1 and so on.

The timing diagram in *Figure 7* shows the external bus read timing of the MPC860 controlled by the GPCM and running at 33 MHz. *Figure 8* shows the OE-controlled read timing of the CY7C056V/057V-12 dual-port devices.

The CY7C05x family offers -12 and -15 speeds. The following timing analysis will show that the -15 device is fast enough to interface to the 33-MHz version of the processor with some margin to spare.

In the read cycle, there are two critical MPC860 timing parameters. The first is the processor's CLKOUT rising edge to $\overline{OE}$ falling edge time (t_3 max = 9 ns) and the second is the read data set-up time (t_2 min = 6 ns). The dual-port critical spec is t_{DOE} which is the time it takes for the memory data to be available on the I/O pins from the falling edge of $\overline{OE}$

With a CLKOUT period of 30 ns (33 MHz) we can see that 15 ns are used up for the t_3 and t_2 parameters. This means that the dual-port device will have no more than 15 ns to have its data available on the bus. With a t_{DOE} of 10 ns we will have a margin of 5 ns. This will be more than sufficient to account for flight time delays (delay due to PCB trace length).

For the write cycle, the two parameters that must be met are the set-up and hold times of the dual-port. The MPC860 write timing diagram (*Figure 9*) shows that the processor's write data is available 14.33 ns max. (t_1) after the rising edge of CLKOUT. The diagram also shows a hold time of 5.58 min. (t_4). This means we have at least 15.67 ns available for data set-up, into the dual-port, prior to the rising edge of $\overline{WE}$. With a dual-port set-up requirement of 10 ns and a hold of 0 ns (*Figure 10*) we have plenty of margin to complete a successful write.

For a complete timing analysis, please refer to the data sheets of the MPC860 and the CY7C056/7.

Note that in a read followed by a write sequence, the CY7C056V/057V meets the MPC860 specification as well. Analysis of the timing specification shows that, in the worst case scenario, the dual-port will be off the bus 19 ns into the first clock period of the MPC860 write cycle. Notice that the processor enables its write data on the I/O lines during the second clock period of its write cycle. The write followed by read operation meets the spec as well.

Interfacing the Sync FLEx36 Dual-Port to the TMS320C6201B DSP Processor

The 6201B is a high-performance fixed-point Digital Signal Processor intended for use in many applications such as telecom and instrumentation.

The 6201B device has a built-in External Memory Interface (EMIF) controller that supports various memory types. The

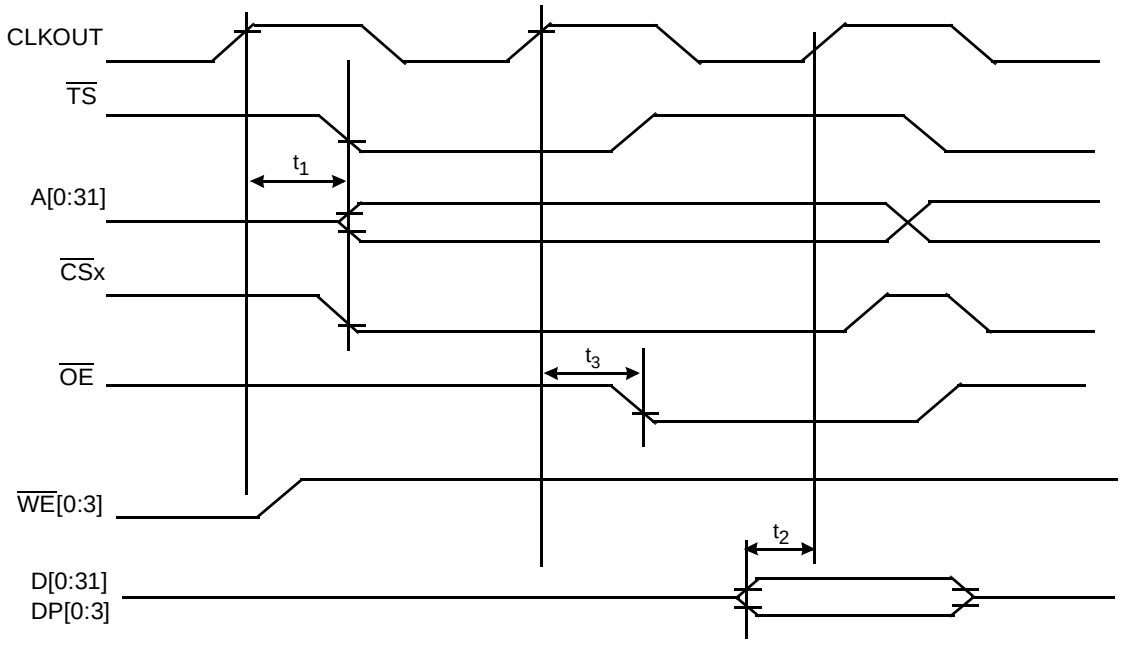

Figure 7. MPC 860 External Bus Read Timing (GPCM Controlled-ACS = 00)

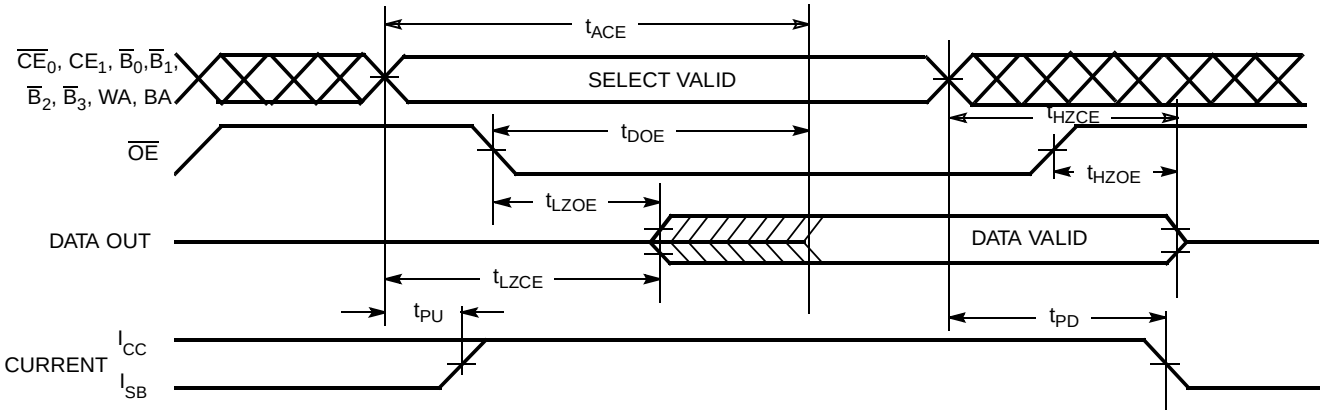

Figure 8. Async Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)

EMIF is user-programmable to generate various chip selects as well to adjust certain interface timing parameters. Its SBSRAM (Sync Burst SRAM) control unit allows glueless interfacing to synchronous memory devices and will be used in this example to interface to the sync FLEx36 dual-port configured for pipelined operations (see *Figure 11* for the connection diagram).

Figure 12 shows the read timing diagram of the 6201B with four memory accesses and *Figure 13* shows the FLEx36 sync dual-port read timing in the pipelined mode. The 6201B EMIF SBSRAM controller supports memory interfaces at ½x and 1x the CPU speed. This application will show the interface between the CY7C095x9V-6 and the 6201B-167 with the memory interface running at ½ the CPU clock frequency. That's an SSCLK cycle time of 12 ns.

In the read case the critical timing is the data set-up time for the processor. The FLEx36 device clocks in the address, and 6.5 ns (t_{CD2}) after the following clock edge the data will be valid on the I/O pins. With a t_{SU} of 3.5 ns for the processor we will have 2 ns available for the flight time. The lower cost -7 device will only leave 1 ns for the flight time. In this case shorter traces and low capacitive loading on the data bus will be essential. Note that a similar analysis of the 6201B-200 interfaced to the -6 device will also have 1 ns of margin. In the write case the address and data set-up and hold times are easily met by the FLEx36 device (*Figure 14*).

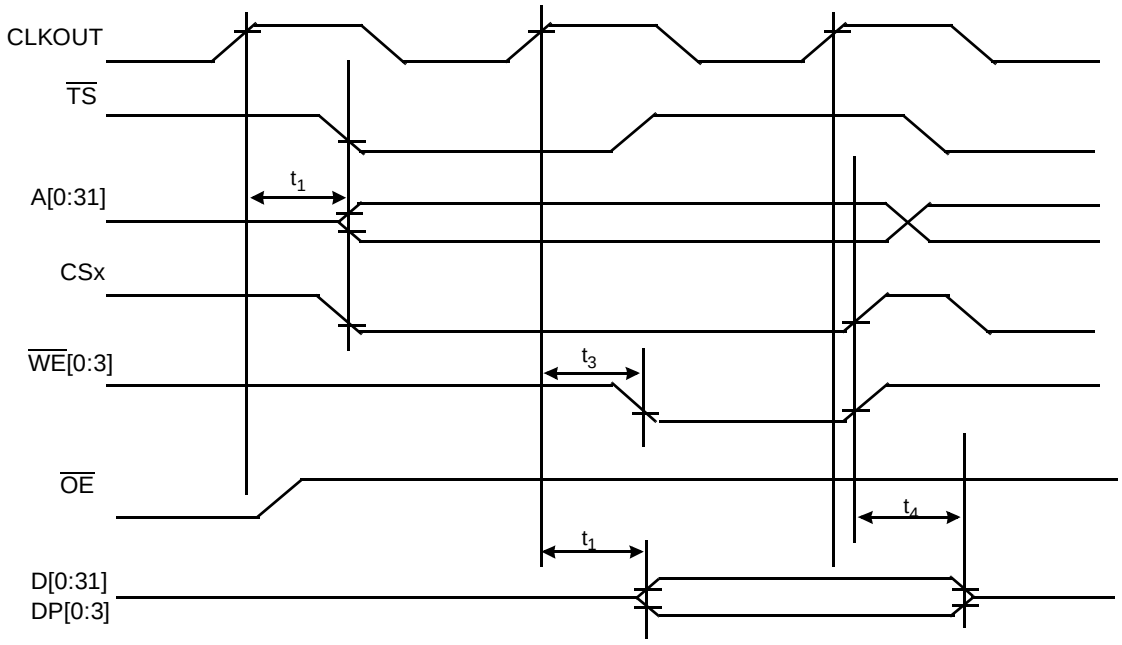

Figure 9. MPC 860 External Bus Write Timing (GPCM Controlled -- TRLX = 0, CSNT = 0

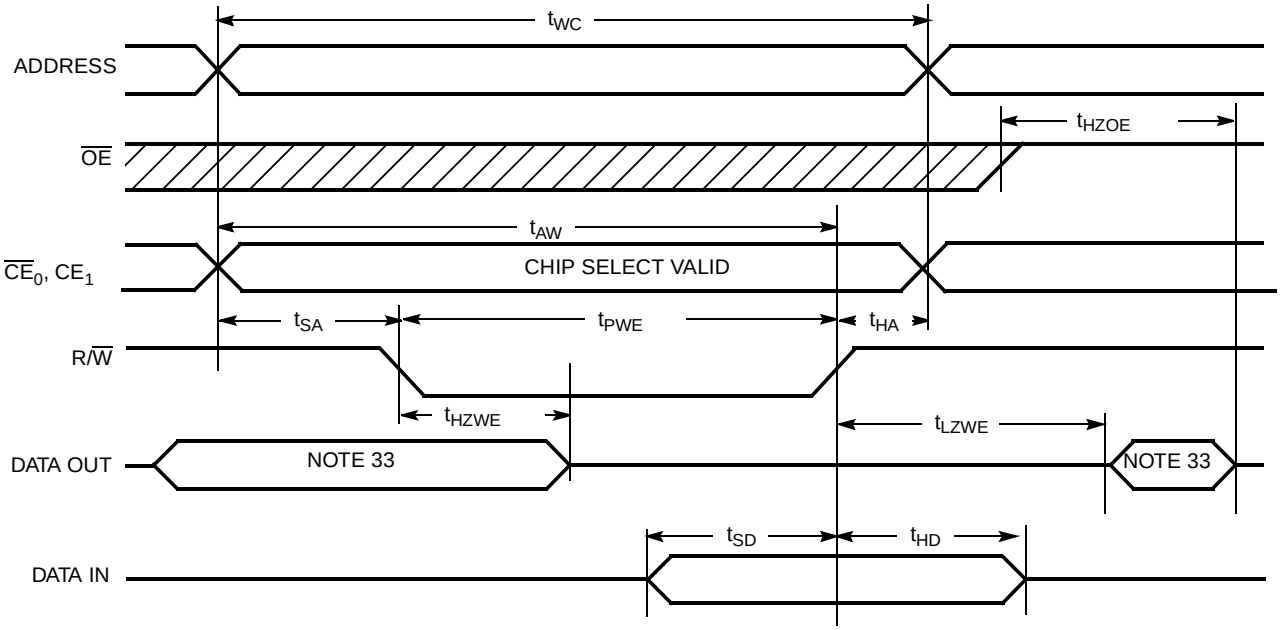

Figure 10. Async Write Cycle No. 1: R/W Controlled Timing

Conclusion

Dual-port architectures have been used in many applications for some time. The FLEx36 family brings these architectures to a new level of speed and flexibility. This results in much higher performance systems with reduced board space and lower cost.

References

1. CY7C05XV and CY7C095X9V FLEx36 Dual-Port SRAM data sheets, Cypress Semiconductor, 1999
2. MPC860 Hardware Specifications, Motorola, 1998
3. TMS320C6201B data sheet, Texas Instruments, 1998

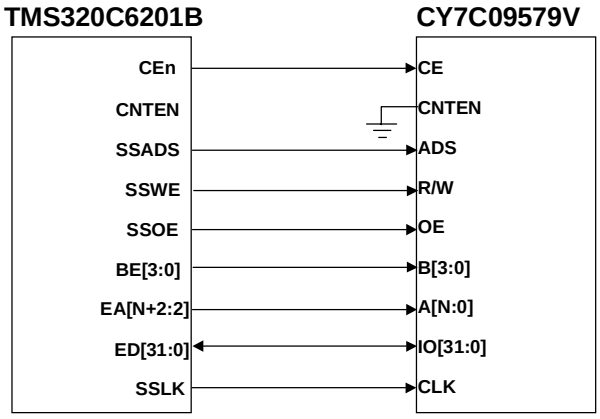

Figure 11. Sync FLEx36 to TMS320C6201B interface

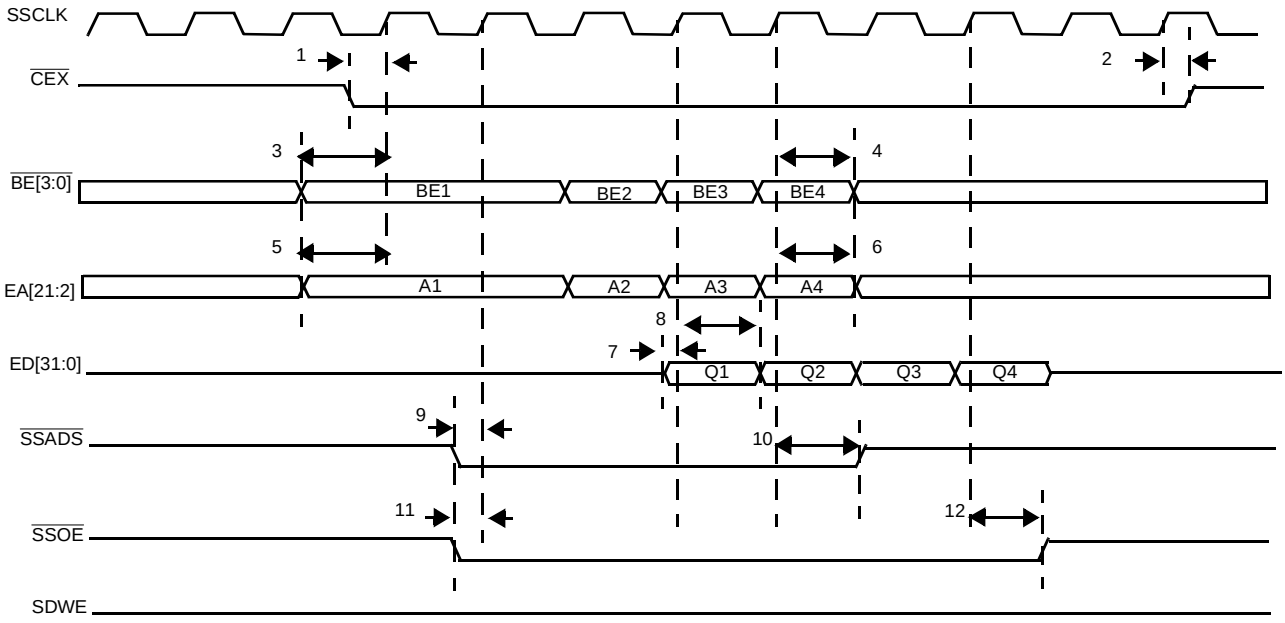

Figure 12. SBSRAM Read Timing (1/2 Rate SSCLK)

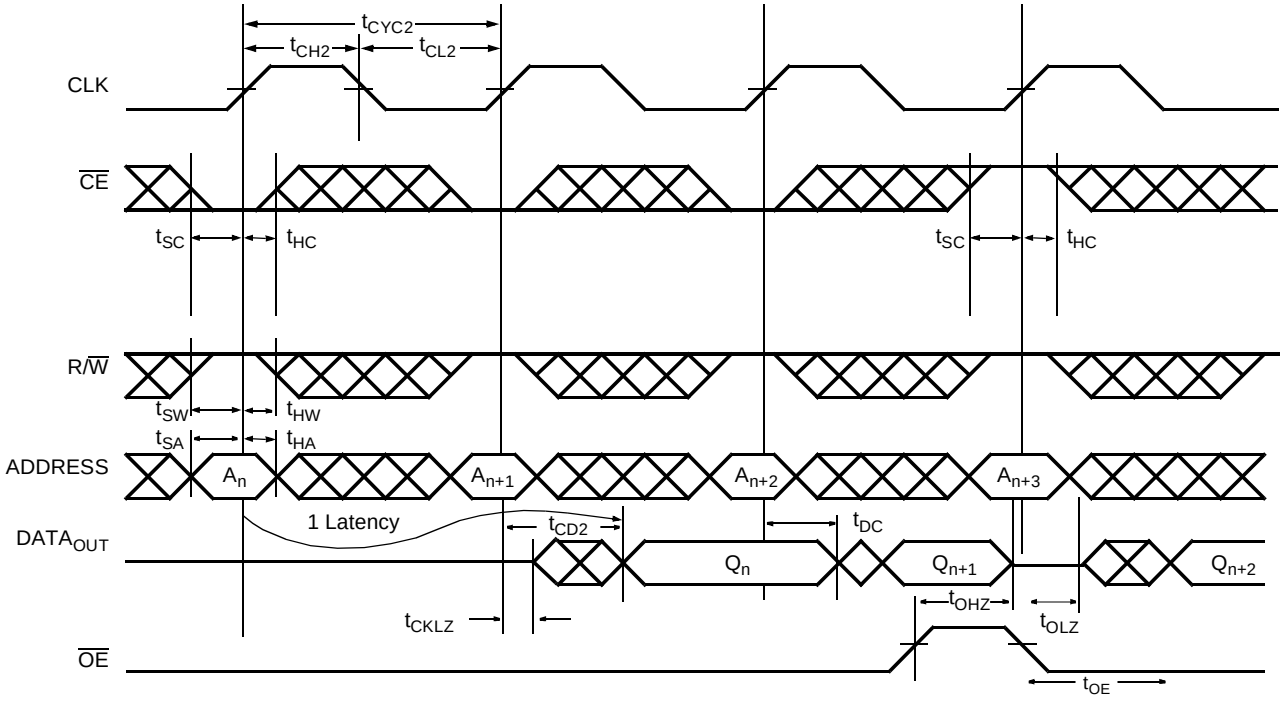

Figure 13. Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE = V_{IH})

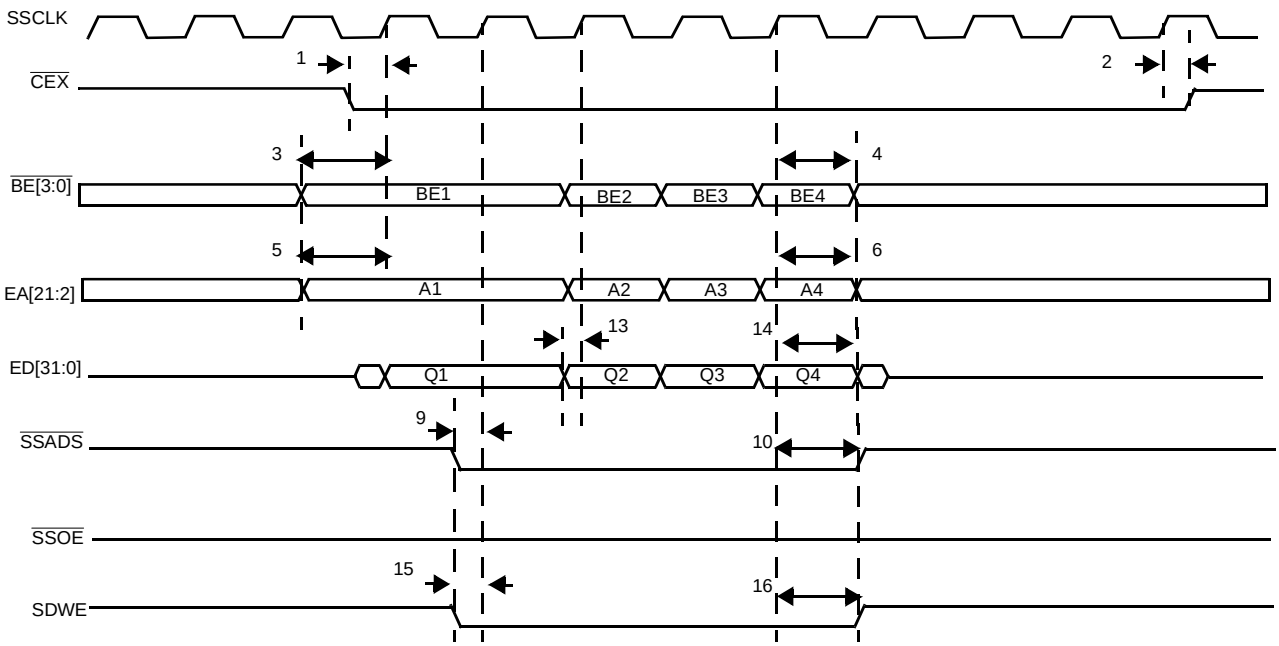

Figure 14. SRAM Write Timing (1/2 Rate SSCLK)