# Input Signal Integrity for CMOS Dual-Port Products

Memory arrays are typically sensitive to noise and glitches at the input. Excessive undershoot or line noise may cause memory upset and data loss. When designing a circuit board, a good termination scheme is needed to maintain signal integrity. For details about the kinds of termination and transmission lines, please refer to the application notes “System Design Considerations When Using Cypress CMOS Circuits,” and “Using Decoupling Capacitors.” The focus here will be on the input side, and what is considered a valid input signal and what is not.

To begin with, *Figure 1* shows the timing waveform of a clock and a data input. For Cypress 1-Meg Dual-Port RAMs (DPRAMs) such as CY7C038, both rise time ($t_R$) and fall time ($t_F$) are specified to be less than or equal to 3 ns. The maximum value for low-level input voltage ($V_{IL}$) is specified to be 0.8V, and the minimum value for high-level input voltage ($V_{IH}$) is specified to be 2.2V. Most manufacturers (including Cypress) center the input threshold level of their devices near 1.5 volts nominal for TTL-compatible input devices. Cypress DPRAMs are CMOS devices that are TTL-compatible, and the threshold levels are somewhat uniform. The CMOS specification for the input level is guaranteed to be a logic HIGH when the input voltage is above 2.2V and a logic LOW when the input voltage level is below 0.8V. This leaves a 1.4-volt range of input voltage for input threshold variation across power supply and temperature changes.

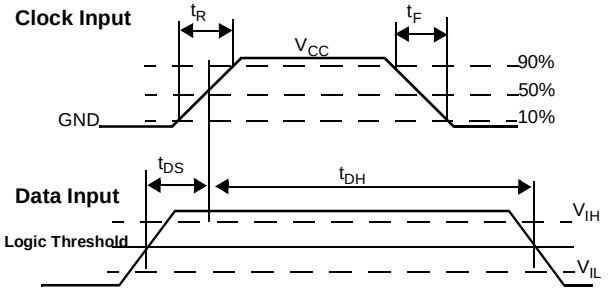


**Figure 1. Input Signal Levels and Timing**

## Ground and Power Supply Bounce

Ground bounce and power supply bounce are two of the primary causes of false switching in high-speed components and are a major cause of poor signal quality. Ground bounce is a voltage oscillation between the ground pin on a device package and the ground reference level on the device die. The main cause is a current passing through the lead inductance of the package. The effect is worst when all outputs switch simultaneously.

False switching may occur when the die ground or die $V_{CC}$ reference voltage bounces enough to cause the input logic threshold (typically at 1.5V) to shift enough to pass through a guaranteed logic LOW or HIGH level (0.8V or 2.2V). In 5V parts, $V_{CC}$ levels are not close to 1.5V and the shifting of the threshold point relative to $V_{CC}$ has a minimal effect of false switching. Therefore, for 5V parts, Ground Bounce is more likely to cause a problem while $V_{CC}$ Bounce is much less of a problem. In 3.3V devices, operating with power supply voltages as low as 2.7V, $V_{CC}$ is much closer to the input threshold point and has more influence in output and input levels. Therefore, $V_{CC}$ Bounce can become a significant factor. As shown in *Figure 2*, if the power signals are bouncing and ringing, the power supply and ground noise will extend directly to the device output and input into the signal path. *Figure 2* also shows 500 mV as the limit of undershoot allowed by Cypress DPRAMs.

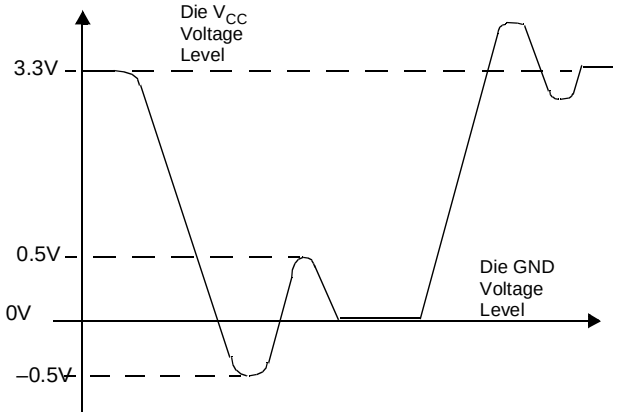


**Figure 2. Ground and Power Supply Bounce for 3.3V**

Memory arrays are some of the most sensitive devices in common usage. With a high-speed memory array, undershoot on input signals is very likely to cause data loss at random times when crossing address boundaries. If the undershoot is excessive, some memory devices may be permanently damaged by the excessive voltage levels.

Ground Bounce is not the only cause of overshoot and undershoot, especially when driving a capacitive load with an inductive line. When undershoot is seen in these applications, another area of investigation would be the line termination. It is extremely important to have the proper termination and matching of the driver to the load. The system designer should take into consideration problems associated with transmission lines such as impedance mismatch. This topic is explained in detail in the application note “System Design Considerations when Using Cypress CMOS Circuits,” which is available at www.cypress.com.

## Oscillation Around Threshold

In the design of high-speed logic, it is important to eliminate any source of noise that would cause the input to the dual port memory device to oscillate around the logic threshold. Such noise problems arise from several causes among which are

the high clock frequency (in synchronous DPRAMs) and the need for fast edge rates (in both synchronous and asynchronous DPRAMs). Noise problems that can develop include double clocking (oscillation), false clocking, and waveform distortion. Oscillation in the input signal as shown in *Figure 3* can occur due to the presence of a noise glitch allowing the input signal to transition through the logic threshold more than once, possibly toggling the input with each transition.

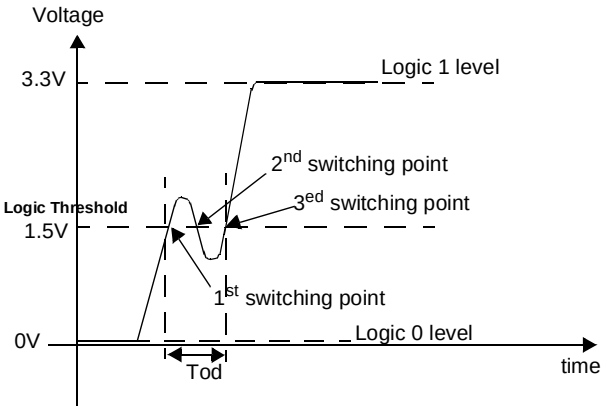


**Figure 3. Oscillation (Multiple Clocking) Around Input Threshold**

False switching can occur if a signal reflects in the transmission line or if a noise pulse couples into the transmission line from an adjacent source, causing the input to transition through the logic threshold. The presence of such transitions in the data input to dual-port memory products could lead to writing the incorrect data to the memory cell. For example, consider the transition from logic 0 to logic 1 at the data-in as shown above. Initially the memory location is written “0”. As the input ramps up towards the logic threshold, a “1” is written to the internal register, but before writing “1” to the memory location, the change in data-in ends the write pulse and so writing “1” to the memory location is not successful. The oscillation around threshold, which could vary in time (Tod is oscillation duration), could lead to false data being written to the memory location. The above situation can also be true for data-in transition from logic 1 to logic 0.

Ground Bounce, overshoot, undershoot and false switching around threshold are some of the noise effects that could cause devices like DPRAMs to fail. It requires a combined effort from IC designers and system designers to overcome such problems. Assuming that the IC manufacturers (such as Cypress) ensure that their components are designed to meet the data sheet specifications, it is the duty of the system engineer to follow these specifications and to provide clean input signals. Memory upset and data loss can be caused by undershoot. These would be transient errors that occur when the driving component is making an address boundary change and undergoing Ground Bounce. Also, some memories may be damaged by excessive undershoot. Off course, undershoot and Ground Bounce would not only affect memory products, but may damage other components such as high speed processors.

## Design Considerations

As mentioned before, it is the job of the system (board) designer to follow certain guidelines (see list ) that will assist in the elimination and suppression of noise sources, noise coupling, and noise reception. One of the most important requirements when designing a circuit board is to have a good ground plane. This is needed to provide the return path of current to its source. Having a good ground plane will also minimize the noise voltage from currents flowing through ground impedances. The next step is to design the power system. Power lines should run parallel to the ground lines if physically possible. If not, the board designer should not compromise the ground layout for the sake of the power layout. Power system noise can be decoupled using decoupling capacitors or filters, but the ground system cannot. Using decoupling capacitors reduces the load on the power lines and removes unwanted glitches in the power system. The application note “Using Decoupling Capacitors” provides more details about this subject.

After layout of power and ground traces, signal layout follows. The most sensitive signals are the clocks, enables, and interrupt lines. The following guidelines should serve as a short check list to help reduce the noise in the system:

1. If possible, use a multi-layer board to minimize power and ground inductance.
2. Use wide traces for power and ground. Use a similar approach for critical traces.
3. Use the lowest frequency clock and the slowest rise time that satisfies system specifications.
4. Place the clock circuit near the connector if the clock goes off the board. Otherwise, place it at the center of the board and close to the receiver.
5. Place clock termination circuitry at the receiver side.
6. Keep clock traces, buses, and enables separate from I/O lines and connectors.
7. Keep digital signal lines, especially the clock, as far away as possible from analog inputs.
8. When working with mixed-signal components, do not cross digital and analog lines. Route the signals away from each other.
9. Minimize the trace lengths on decoupling capacitors. Also, shorten the length of traces for sensitive pins such as clocks, R/W signals, and enables.
10. Use high-frequency, low-inductance ceramic disk or multi-layer ceramic capacitors for IC decoupling. Use 0.01–0.1 µF value depending on the frequency of the system.
11. Locate decoupling capacitors next to each IC in the system.
12. Connect all unused inputs to power or ground.
13. Use series termination to attenuate transmission line reflections.

## Conclusion

There are several factors that affect signal quality in high-speed circuits. There is always a need to pay careful attention to design rules and follow specific guidelines. Doing so will reduce the system and signal noise such as Ground Bounce and double clocking. Dual-Port products (and other memory products) are extremely sensitive to noise. It is important to have a quiet system in order to avoid false switching and the writing of false data into the memory array.