Application Note 002: LNI7010 in 32-bit Applications

1 USING THE LNI7010 NETWORK SEARCH ENGINE IN 32-BIT APPLICATIONS

The CYNSE70032/LNI7010 Network Search Engine (NDSE) is ideal for layer 2 and layer 3 applications requiring word-widths from 68 to 272 bits. This device has been designed to be able to handle varying widths that are optimally greater than 64 bits. 32 bits may often be required, however, in asynchronous transfer mode (ATM) and/or Internet protocol (IP) addresses. For these 32-bit applications, the results can be achieved in two clock (CLK) cycles, thereby ensuring that the NDSE is fully utilized.

2 WRITE OPERATIONS USING THE GLOBAL MASK REGISTER

The LNI7010 is usually organized into 68-bit widths. Data is written into the device using the global mask register (GMR). By setting a 1 in the GMR, data can be written into the LNI7010. A 0 in the GMR will not modify the data. As 34 bits of data are available, information has to be written into both the left and right halves of the 68-bit word.

The first step is to write to two of the eight GMRs with the patterns shown in Figure 1.

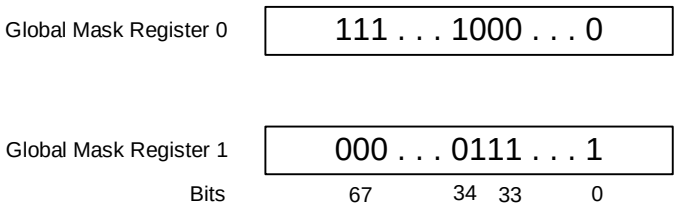

FIGURE 1. PATTERNS REQUIRED IN THE GLOBAL MASK REGISTER

After this data is loaded in the device by performing a WRITE operation that uses GMR 1 until the left half of the data array is completely full. This operation stores the left half of the 68-bit data word (or 34 bits) in the data array.

In Figure 2, bits 67-36 are shown in one section that represents a 32-bit word. Bits 35 and 34 are shown separately. For example, bits 67-36 can represent IP addresses. Bits 35 and 34 can be user-defined. In this application, 34-bit operations occur in each half-section of the NDSE's data and mask arrays.

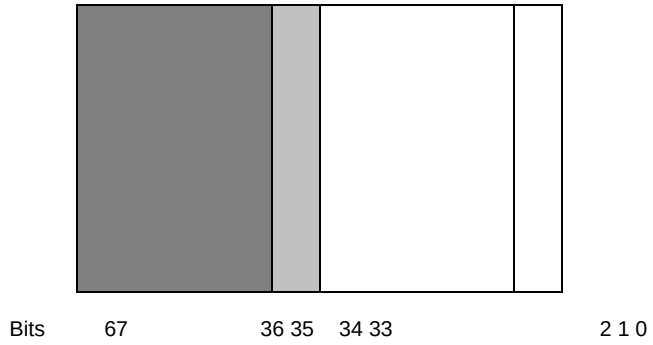

FIGURE 2. STORING THE LEFT HALF OF THE DATA ARRAY OR MASK ARRAY

Bits 67 through 34 are stored in the data array, and the entire left half must be filled before proceeding to the right half. **Note**. Bits 35 and 34 are shown separately in the figure and it is recommended that the user define bit 34 as a valid bit. The LNI7010 device is very flexible: it is acceptable if another bit position is defined as a valid bit, and essentially the user has all 34 bits at his disposal.

After the left half is completely full, the right half must be written. GMR 1 is used for this purpose, and for performing WRITE operations. In this operation, the right half of the 68-bit word is stored in the rightmost

34 bits of the data array. Not all locations have to be written, because the array can be partially full on the right or even the left side.

Now a SEARCH operation can proceed. The SEARCH operations are performed twice, on the left half and on the right half (in that order). **Note**. A “1” in the GMR enables a COMPARE during a SEARCH operation and a “0” forces a match condition regardless of the state of the data bit. The SEARCH throughput for 34-bit operations is half of that of 68-bit operations. The SEARCH is performed using GMR 0 for the left half of the 68-bit word, after which a SEARCH on the right half of the 68-bit word is performed using GMR 1. The order is important, as the left half has a higher priority than the right half. For example, if a SEARCH on the left half produces a match and a search on the right half also produces a match, then the left half has the higher priority. If only one unique match exists in a particular system, a match on the left side may alleviate the need to do a SEARCH on the right half.

3 CASCADING LNI7010 SEARCH ENGINES AND 32-BIT OPERATIONS

When depths greater than 32K are desired, the 32-bit operations can also be performed in cascaded mode. The data has to be written in an ordered manner: the entire left half must be written across boundaries and then right half. Figure 3 shows the required sequence for writing into the device.

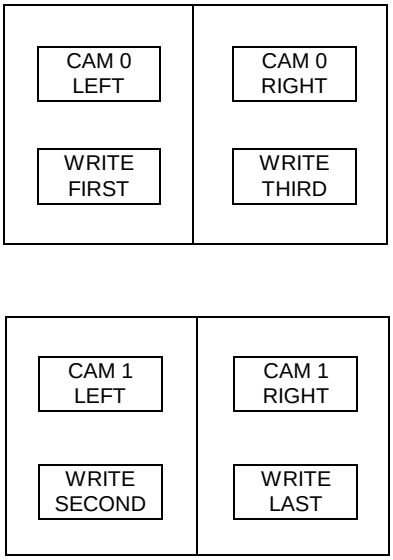

FIGURE 3. WRITE ORDER OF ENTRIES FOR CASCADED 32-BIT OPERATIONS

After the data arrays have been written using the GMR, they are ready for searches using two cycles as explained earlier in the standalone CAM application.

4 CONCLUSION

The LNI7010 is a configurable NDSE. Although it was optimized for 68-bit, 136-bit , and 272-bit operations, it can efficiently handle 32-bit look-ups as well.

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