Application Note 004: Multiple Search Table Management Using LNI70X0 Network Search Engines

1 INTRODUCTION

This application note explains how multiple search tables with variable widths can be configured within the LNI70X0 Network Search Engines (NSEs). Since the internal architecture of the LNI7010 and LNI7020 is similar, the following discussion on table management applies to both of these NSE devices. The table management has been simplified in the discussion surrounding the LNI7040 NSE, for reasons that will be developed below.

2 USING LNI70XO NSES WITH ASSOCIATIVE PROCESSING TECHNOLOGY ™

The LNI70X0 devices are high-performance, pipelined, synchronous NSEs. The LNI7010 device is organized as 8K x 136 bits, but can also be configured as 4K x 272 bits or 16K x 68 bits. The LNI7020 device is organized as 16K x 136 bits, but can also be configured as 8K x 272 bits or 64K x 72 bits. The LNI7040 device is organized as 32K x 144 bits, but can also be configured as 16K x 288 bits or 16K x 68 bits. The LNI7010 device can sustain 83 million searches per second on any subfield of a 68- or 136-bit field, while the LNI7040 device can sustain 100 million searches per second on any subfield of a 72- or 144-bit field. This capability makes these devices the fastest NSEs in the market. These high-speed, high-capacity chips can be employed in a variety of networking and communications applications that require fast table searches.

A unique feature of the LNI70X0 devices is their flexibility in their ability to configure multiple search tables of different widths within the same device. By simultaneously comparing the desired information against the entire list of pre-stored entries, the LNI70X0 devices provide performance advantages over other memory search algorithms such as binary or tree-based searches which give them an order-of-magnitude reduction in search time. Figure 1 shows four 68-bit-wide quadrants in the LNI7010 device.

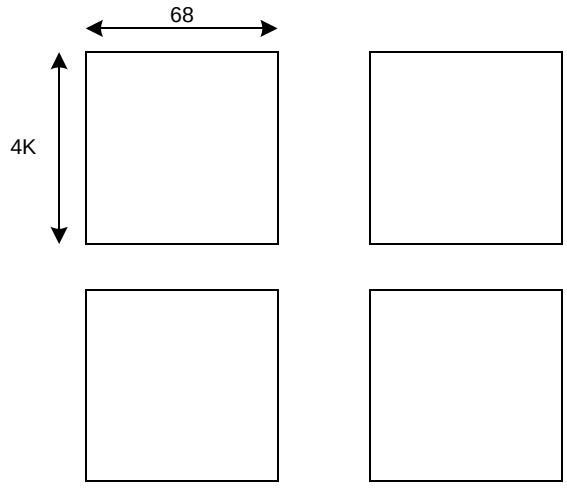

FIGURE 1. FOUR 68-BIT-WIDE QUADRANTS IN LNI7010 NSE

The LNI7010 NSE consists of 16K x 68-bit storage cells referred to as data bits. There is a mask cell corresponding to each data cell. Figure 2 below shows three different configuration (CFG) tables based on the value of CFG bits[16:9] in the command register of the device. The LNI7020 NSE consists of 32K x 68-bit storage cells, and the LNI7040 NSE consists of 64K x 72-bit storage cells.

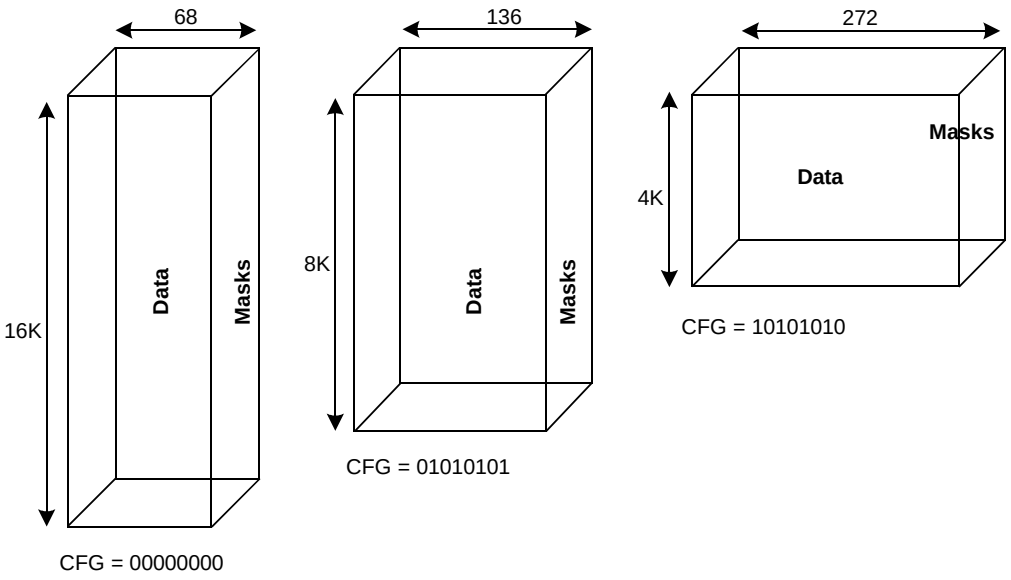

FIGURE 2. LNI7010 NSE STRUCTURE

The LNI7010 NSE is internally divided into four quadrants of 4K x 68-bits, each of which can be arranged as 4K x 68 bits, 2K x 136 bits, or 1K x 272 bits. It can also be configured to contain tables of different widths within the same device (see Figure 3).

There are eight CFG bits in the command register: bits[16:9]. They are subdivided into 2 bits per quadrant, as shown in Table 1. The supported table widths are shown in Table 2. Initially, these CFG bits have values of 00000000. Each quadrant may be set to one of the three configurations, as shown in Figure 3.

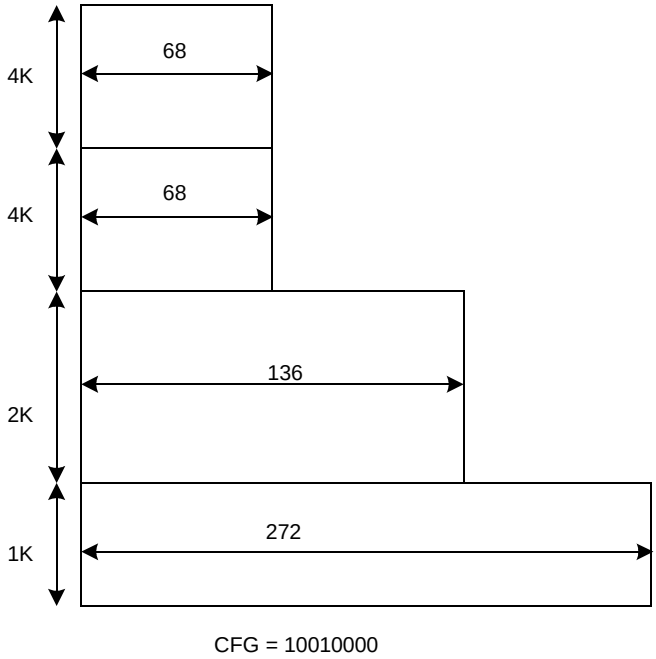

FIGURE 3. MULTIWIDTH CONFIGURATIONS

TABLE 1. CONFIGURATION BITS FOR EACH QUADRANT

QUADRANT	COMMAND BITS
Q1	10:9
Q2	12:11
Q3	14:13
Q4	16:15

TABLE 2. CONFIGURATION BITS AND TABLE WIDTHS

COMMAND BIT	CFG BITS FOR EACH QUADRANT
00	4K x 68 bits
01	2K x 136 bits
10	1K x 272 bits

3 LOGICAL TABLES WITH VARIABLE WIDTHS USING THE LNI70X0 NSES

LNI70X0 NSEs can be configured to contain more than one logical table within the device. To accomplish this, it is necessary to assign table identifier bits. It is possible to create multiple tables within the device with the help of these table identifier bits. **Note**. When creating several tables, the total number of bits in all tables combined may not exceed 1M.

Figure 4 shows an example of maintaining six search tables, each having a width of 68 bits. In this case, the value of the CFG bits[16:9] is 00000000. Bits[3:1] are used as table identifiers. Bit 0 indicates whether the location is Full or Empty, as required by the LEARN mode.*

* See Lara Networks, Inc. datasheets for the LNI70X0 NSE family (on the web at http://www.laranetworks.com) for a description of the LEARN mode.

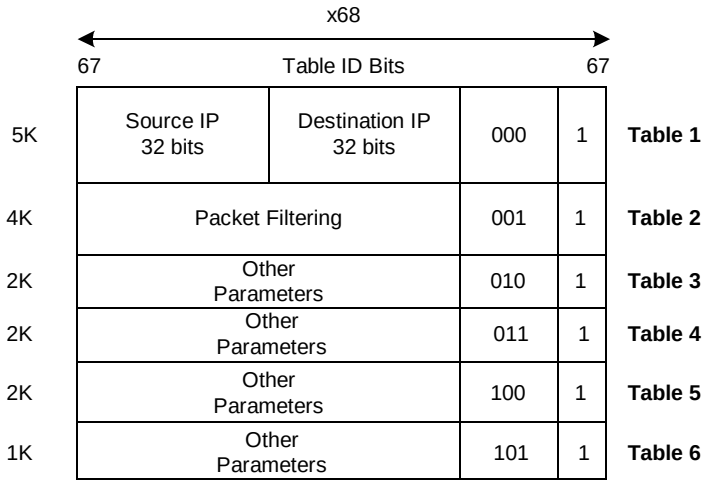

FIGURE 4. SIX 68-BIT-WIDE TABLES

4 SEARCH TABLES WITH MULTIPLE WIDTHS USING LNI7010/LNI7020 NSES

The following example outlines another way in which to create search tables with two different widths. As shown in Figure 5, the device is configured to contain two search tables, one being 8K x 68 bits wide and the other being 4K x 136 bits wide. The CFG bits[16:9] in this case are 01010000. As in the previous example, bits[2:1] are assigned as table identifiers. Bit 0 is used to indicate if the entry is Full or Empty, as required by the LEARN mode.

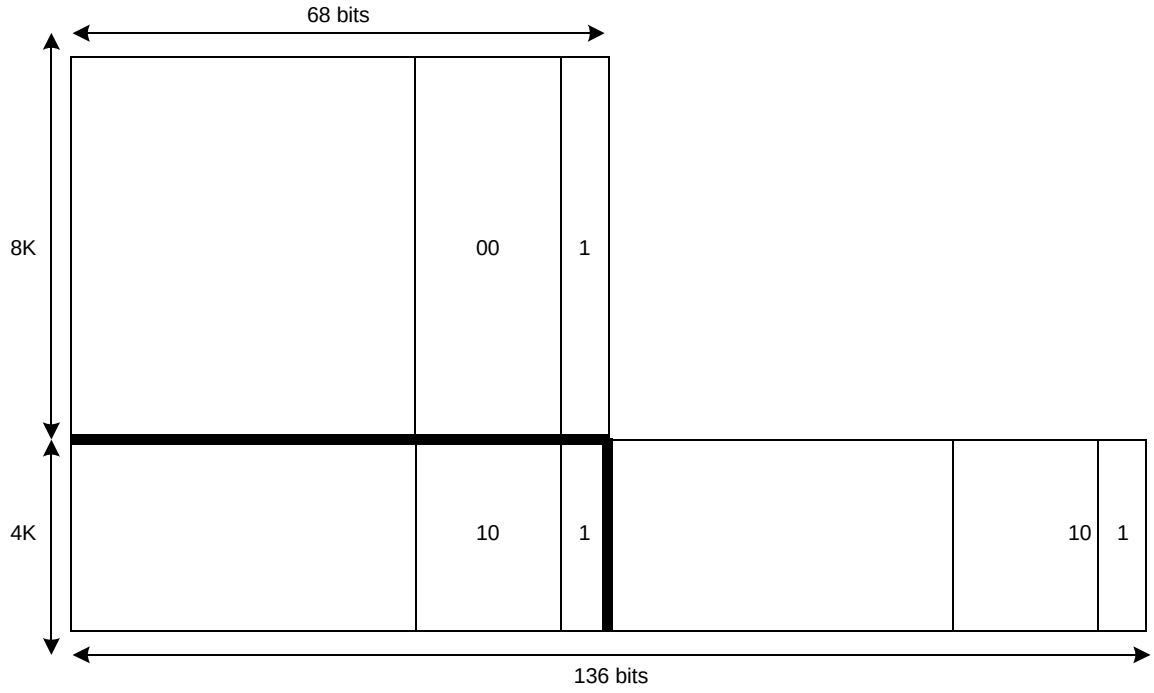

FIGURE 5. 68- AND 136-BIT-WIDE TABLES

For a 136-bit-wide table, it is necessary to enter the table ID bits[2:1] in both 68-bit-wide quadrants because the search starts in both 68-bit quadrants simultaneously. Even though the search is intended in the 136-bit-wide table, it is possible to find an erroneous match in the 68-bit quadrant, if the table ID bits are not used in each 68-bit quadrant.

Figure 6 illustrates an example of creating three tables with different widths. The CFG bits[16:9] in this example are 10010000. Bits[1:0] are assigned as table ID bits. In this example, since the LEARN mode is not used, bit 0 may be used as a table ID bit.

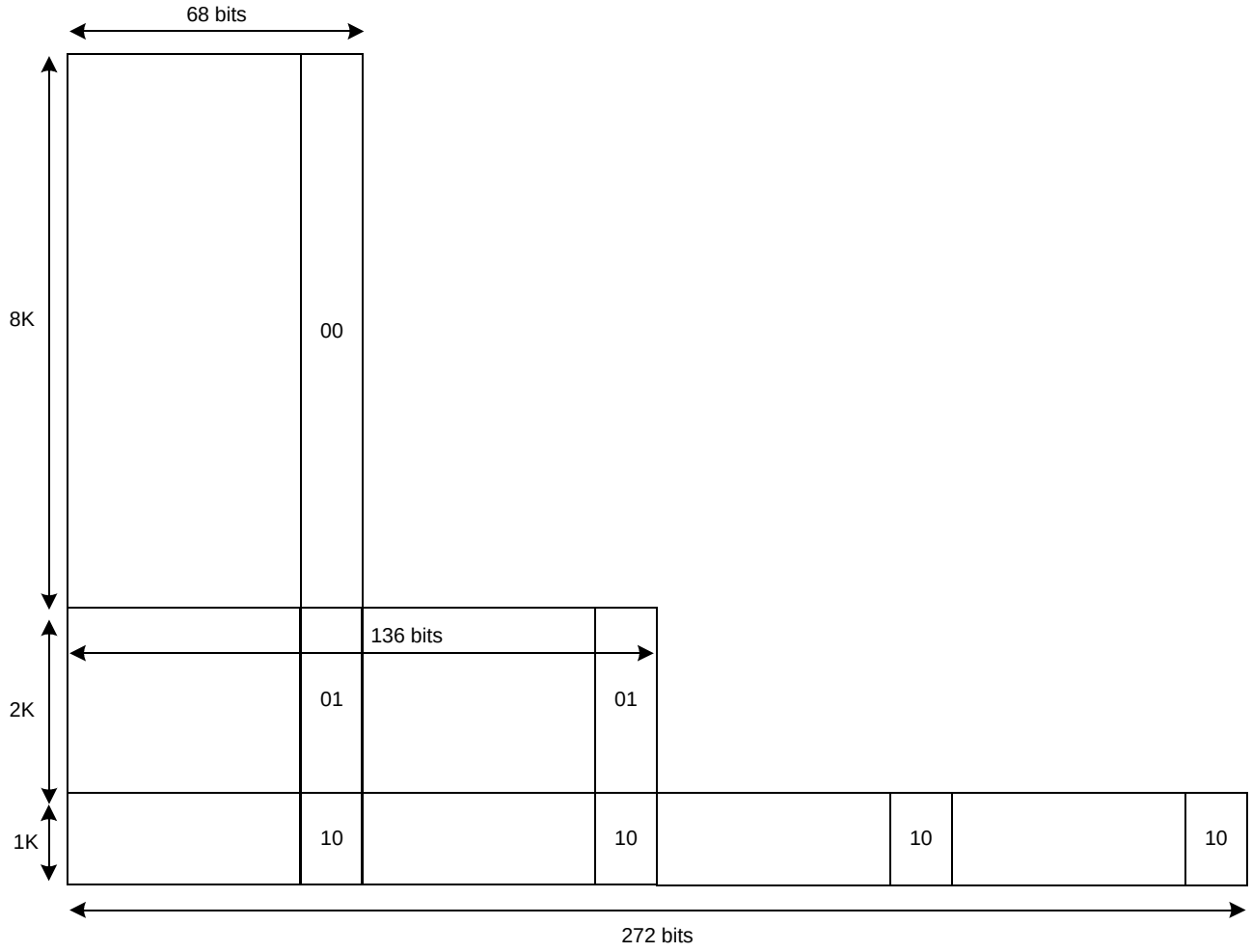

FIGURE 6. TABLE CONFIGURATION WITH DIFFERENT WIDTHS

As with the previous example, it is necessary to enter the table ID bits in each of the 68-bit quadrants. Without doing this, an erroneous match may be found in any quadrant of the 68-bit-wide table.

Table size (TLSZ) ID has been simplified in the LNI7040 NSE with the help of the command bits. CMD[2] and CMD[9] are used to identify the width of the search table, and have SEARCH command formats as identified in Table 2.

TABLE 3. COMMAND PARAMETERS IN THE LNI7040 NSE

COMMAND BIT	CYCLE	VALUE	TABLE SIZE
CMD[2]	A	0	72 bits or 272 bits
		1	288 bits
CMD[9]	A	0	72 bits
		1	144 bits
		X	288 bits

As can be seen from Table 3, the LNI7040 can identify the search table size configuration by combining these command bits and there is no need to assign the table ID bits. However, if the multiple tables within the LNI7040 have same width (e.g. 68-bits), it is necessary to assign table ID bits as shown in Table 2.

5 SUMMARY

Lara's LNI70X0 NSEs allow the creation of search tables of variable widths within the same device, a unique feature. This approach offers a cost-effective solution for small size applications. Another versatile feature is the depth cascading capability of several NSEs at once. Depth cascading of up to eight devices will enable the formation of table sizes of 128K x 68 bits, 64K x 136 bits, or 32K x 272 bits. Depth cascading can be further expanded by cascading up to 31 devices, whereupon the table sizes can be expanded to 496 x 68 bits, 248K x 136 bits, 124K x 272 bits.

With the proliferation of the Internet-related services such as VPN, QoS, and CoS, the demand on very large searches and look-ups is increasing. Consequently, the software search tables that are slow and may become expensive with increasing search table sizes cannot meet these requests.

Using Lara's NSE modules can further expand the table sizes. The LTI7040 is a four-chip module and LTI7080 is an eight-chip module. Up to three eight-chip modules and one eight-chip module can be cascaded. This arrangement will enable the creation of tables of sizes ranging from 384K x 68 bits, 192K x 136 bits, and 96K x 272 bits.

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