CY62157CV18 MoBL2™

512K x 16 Static RAM

Features

- **Low voltage range:**
  - **CY62157CV18: 1.65V–1.95V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE_1}$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

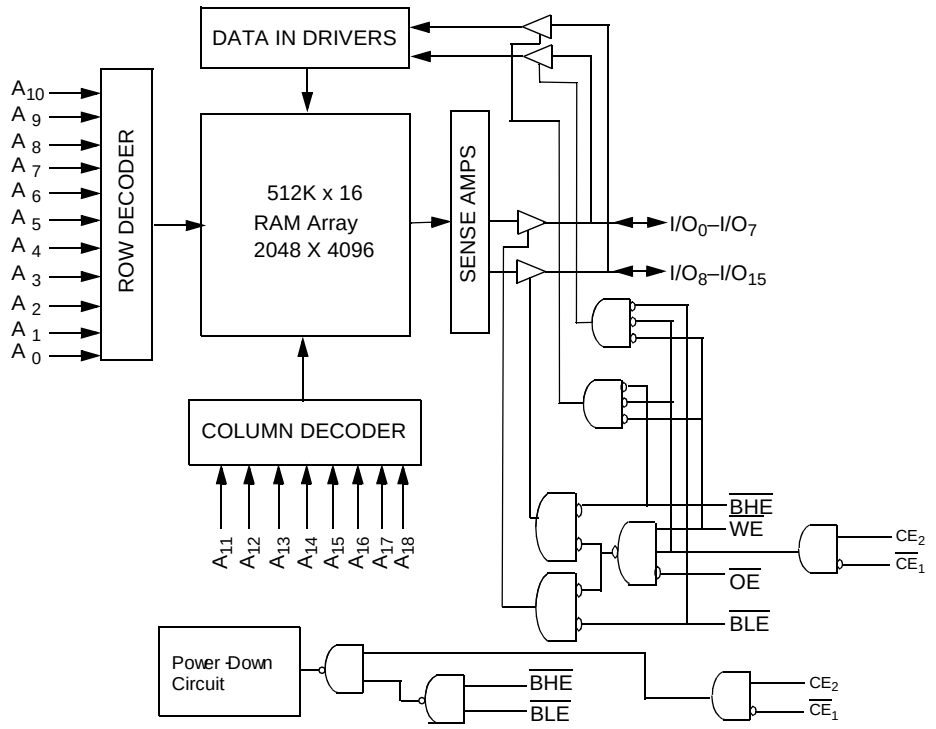
The CY62157CV18 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE_1}$ HIGH or CE_2 LOW). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE_1}$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ($\overline{CE_1}$ LOW, CE_2 HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enables $\overline{CE_1}$ LOW, CE_2 HIGH and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable $\overline{CE_1}$ LOW, CE_2 HIGH and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this datasheet for a complete description of read and write modes.

The CY62157CV18 is available in a 48-Ball FBGA package.

Logic Block Diagram



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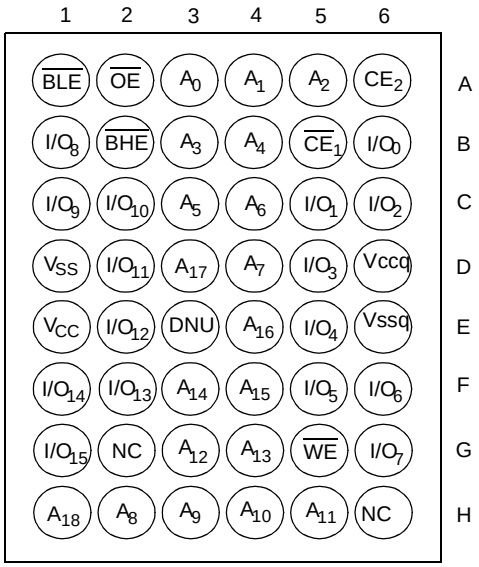
Pin Configuration[1, 2, 3 ,4]

FBGA

Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with
Power Applied–55°C to +125°C

Supply Voltage to Ground Potential–0.2V to +2.4V

DC Voltage Applied to Outputs
in High Z State[5]–0.2V to V_{CC} + 0.2V

DC Input Voltage[5]–0.2V to V_{CC} + 0.2V

Output Current into Outputs (LOW)20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62157CV18	Industrial	–40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating (I_{CC})				Standby (I_{SB2})	
					55 ns		70 ns			
	Min.	Typ.[6]	Max.		Typ.[6]	Max.	Typ.[6]	Max.	Typ.[6]	Max.
CY62157CV18	1.65V	1.8V	1.95V	55, 70 ns	5 mA	15 mA	4 mA	12 mA	2 µA	20 µA

Notes:

1. NC pins are not connected to the die.
2. V_{SS}, V_{SSQ} = groundplane on application
3. V_{CC}, V_{CCQ} = powerplane on application
4. E3 (DNU) can be left as NC or Vss to ensure proper application.
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25, f = f_{max}

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Electrical Characteristics Over the Operating Range[7, 8, 9]

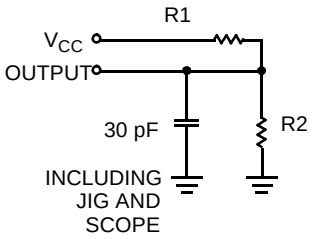
Parameter	Description	Test Conditions		CY62157CV18-55			CY62157CV18-70			Unit
				Min.	Typ.	Max.	Min.	Typ.[6]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65V	1.4			1.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65V			0.2			0.2	V
V_{IH}	Input HIGH Voltage		V_{CC} = 1.95V	1.4		V_{CC} +0.2V	1.4		V_{CC} +0.2V	V
V_{IL}	Input LOW Voltage		V_{CC} = 1.65V	–0.2		0.4	–0.2		0.4	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	±1	+1	–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	±1	+1	–1	+1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS levels	V_{CC} = 1.95V		5	15		4	12	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels			0.5	3		0.5	3	mA
		I_{OUT} = 0 mA, f = 0 Hz, CMOS Levels			1.5	20		1.5	20	µA
I_{SB1}	Automatic CE Power-Down Current— TTL Levels	$\overline{CE}_1$ ≥ V_{CC}–0.2V, or CE_2 ≤ 0.2V V_{IN} = TTL Levels f = f_{MAX} (Address and Data Only, V_{IN}=TTL Levels), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, $\overline{BLE}$, V_{IN}≥Vcc–0.2V, V_{IN}≤0.2V)			1.5	20		1.5	20	µA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	V_{CC} = 1.95V							

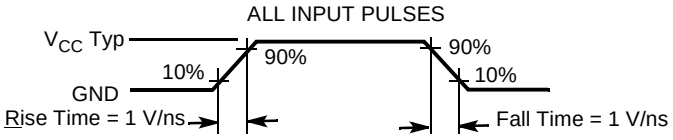
Capacitance[10]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

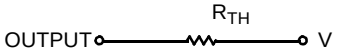
7. Overshoot: V_{CC} + 1.0V, Pulse Width < 20 ns
8. Undershoot: –1.0V, Pulse Width < 20 ns
9. Overshoot and Undershoot specifications are samples and are not tested
10. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

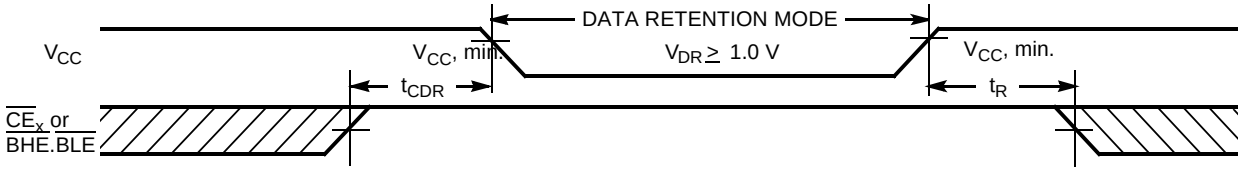


Parameters	1.8V	Unit
R1	13500	Ohms
R2	10800	Ohms
R_{TH}	6000	Ohms
V_{TH}	0.80	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[6]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	62157V18	1.0		1.95	V
I_{CCDR}	Data Retention Current	$\overline{V_{CC}}$= 1.0V $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ No input may exceed V_{CC} + 0.2V		1	10	µA
t_{CDR}[10]	Chip Deselect to Data Retention Time		0			ns
t_R[11]	Operation Recovery Time		100			µs

Data Retention Waveform[12, 13]



Switching Characteristics Over the Operating Range[12, 14]

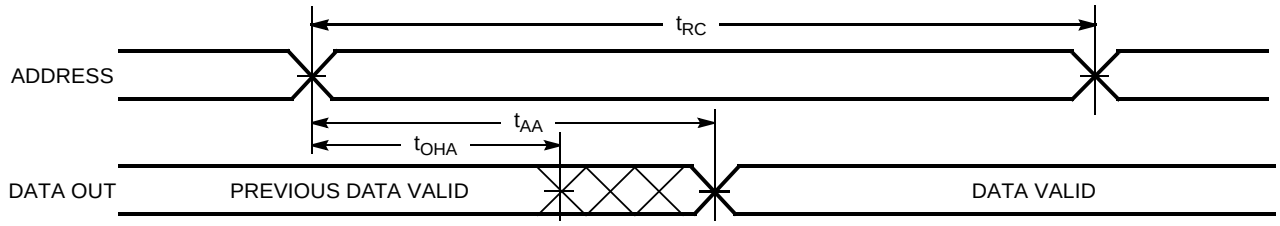
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[15, 16]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16]		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[15]	10		10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[15,16]		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-Down		55		70	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[15]	5		5		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z[15,16]		20		25	ns
WRITE CYCLE[17, 18]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	45		60		ns
t_{AW}	Address Set-Up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	45		60		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[15,16]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[15]	5		10		ns

Notes:

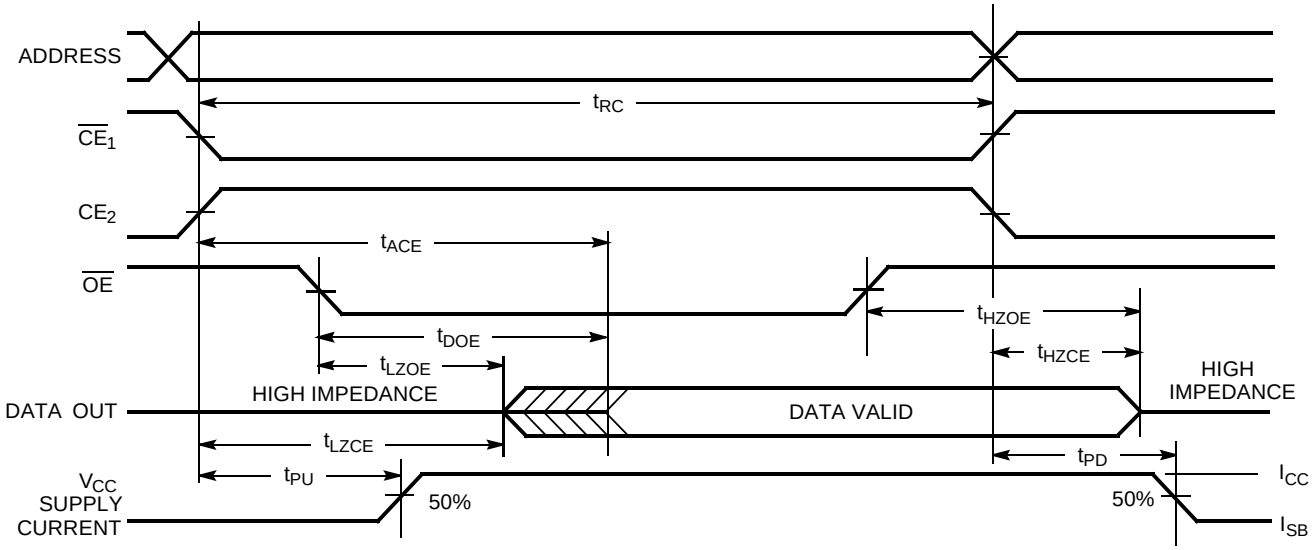
11. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 10$ ms or stable at $V_{CC(min.)} \geq 10$ ms.
12. $\overline{CE}_x$ is the combination of $\overline{CE}_1$ and CE_2.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
14. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE} and t_{HZWE} is less than t_{LZWE} for any given device
16. t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} are specified with C_L = 5 pF. Transition is measured ±200 mV from steady-state voltage
17. The internal write time of the memory is defined by the overlap of WE, $\overline{CE}_1$ =V_{IL} and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and either signal can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms[12]

Read Cycle No. 1 (Address Transition controlled)[19, 20]



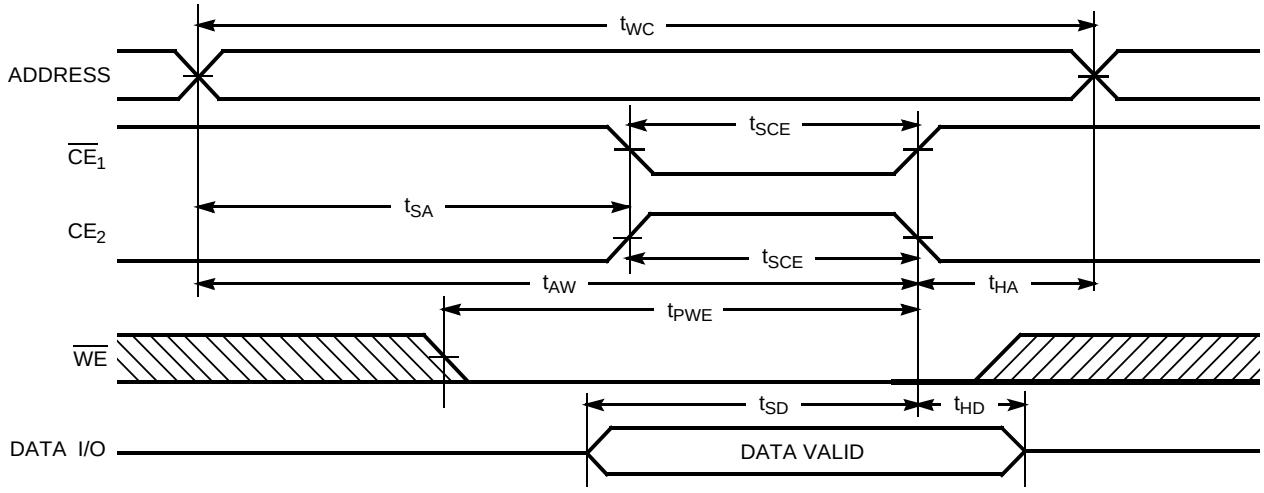
Read Cycle No. 2 ($\overline{OE}$ controlled)[20, 21]



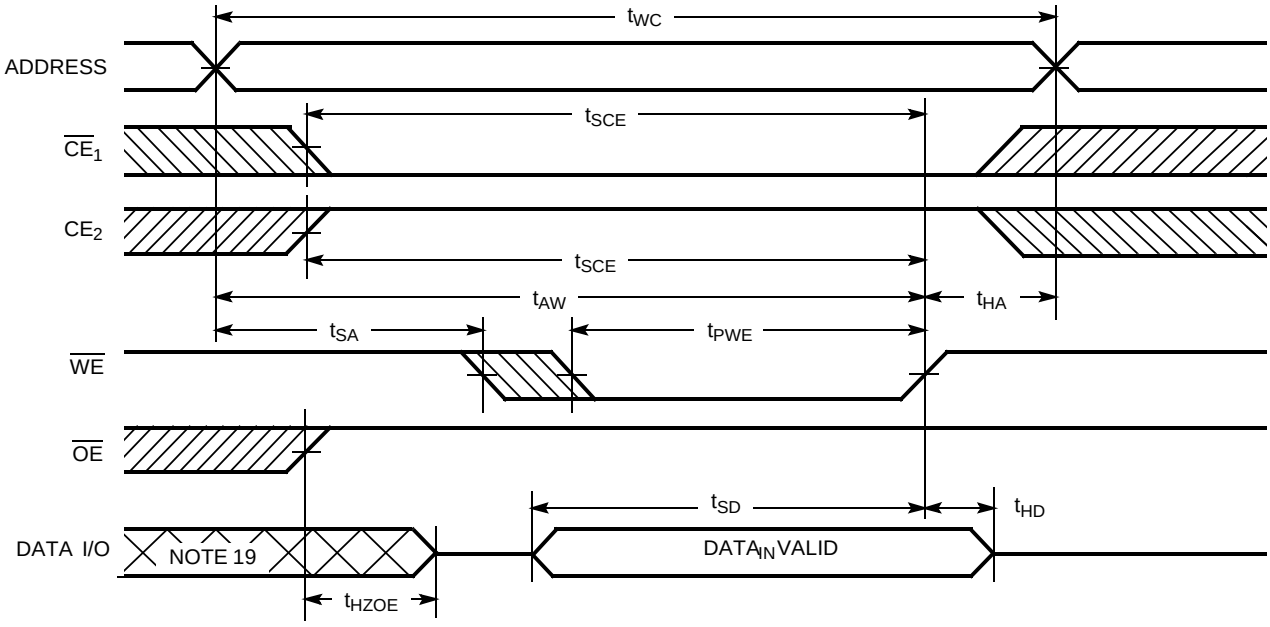
Notes:
19. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms[12] (continued)

Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[22, 23]



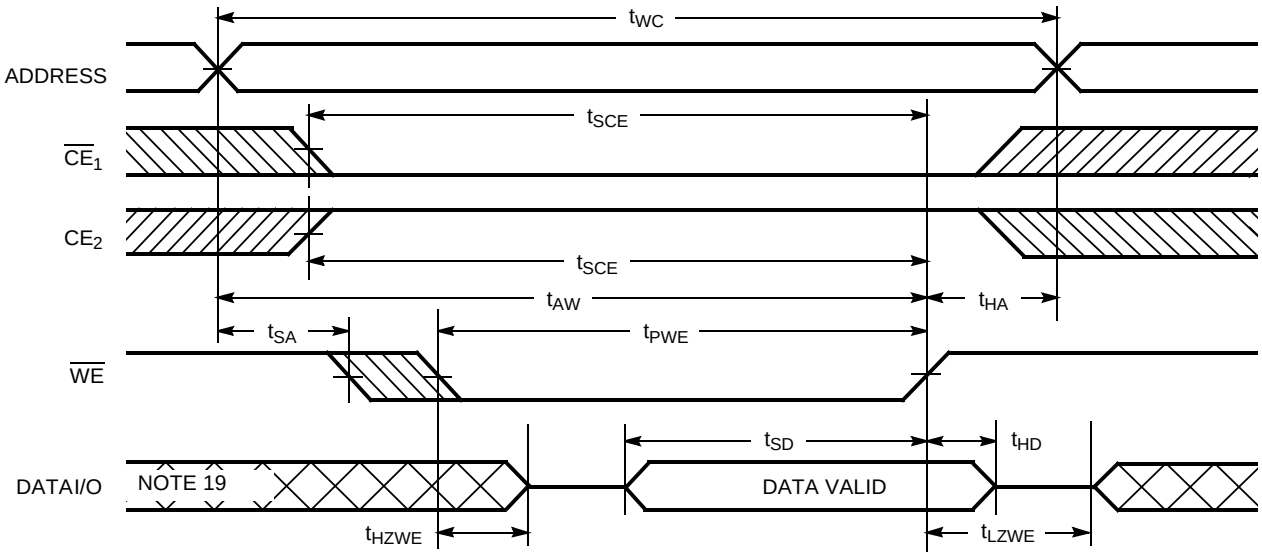
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[22, 23]



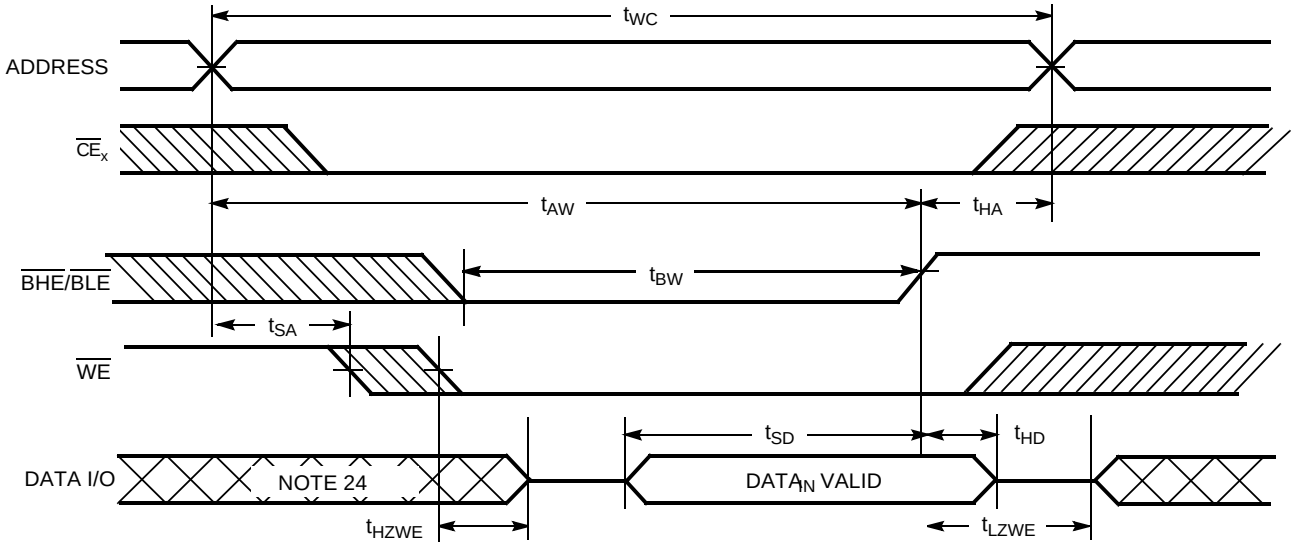
Notes:
22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
23. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
24. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms[12] (continued)

Write Cycle No. 3 (WE Controlled, OE LOW)[18, 23]



Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)[12, 23, 24]



Truth Table

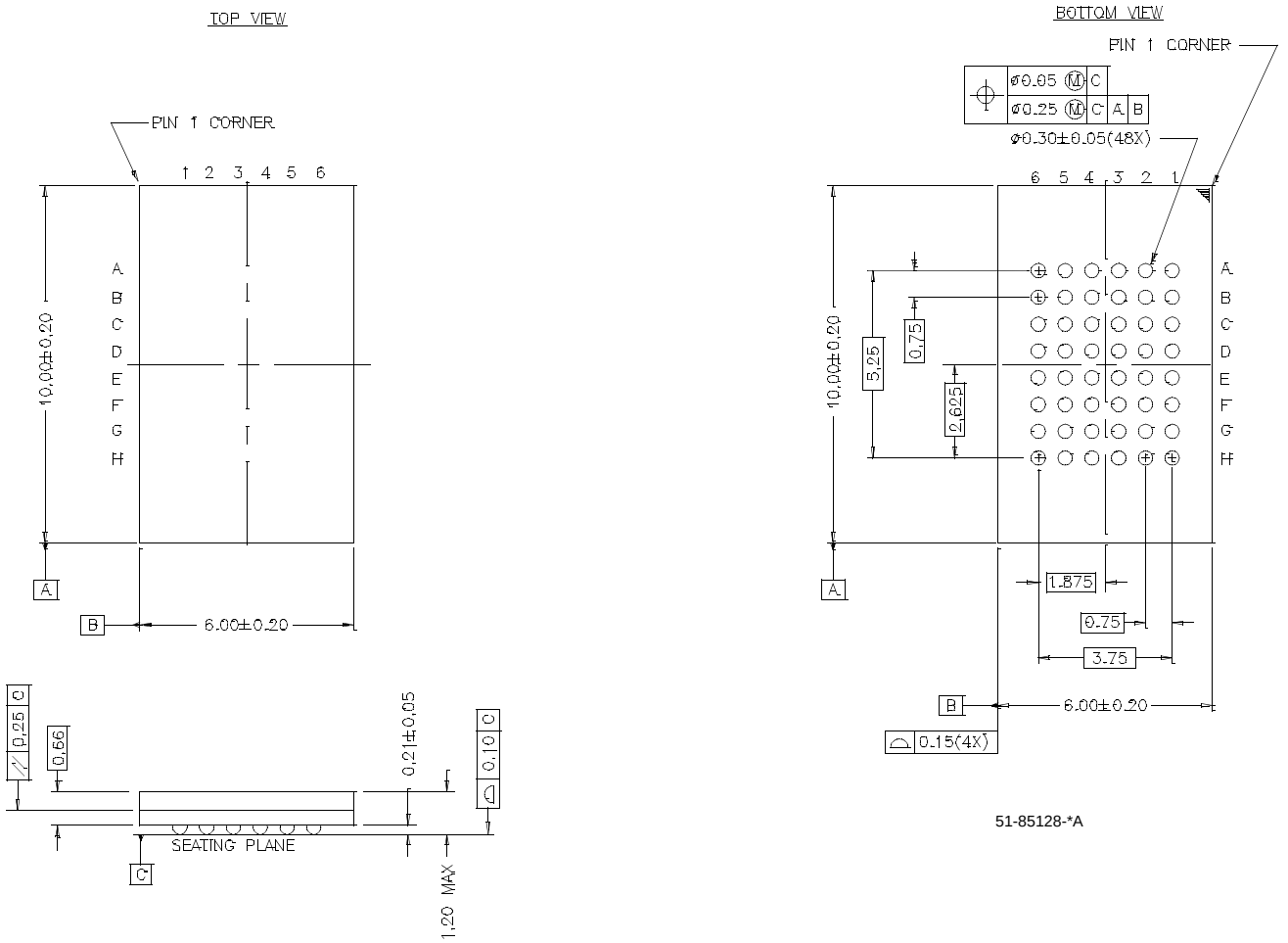
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O0–I/O15)	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O0–I/O7); High Z (I/O8–I/O15)	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O0–I/O7); Data Out (I/O8–I/O15)	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O0–I/O15)	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O0–I/O7); High Z (I/O8–I/O15)	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O0–I/O7); Data In (I/O8–I/O15)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62157CV18LL-55BAI	BA48F	48-Ball Fine Pitch BGA	Industrial
70	CY62157CV18LL-70BAI			

Package Diagram

48-Ball (6 mm x 10 mm x 1.2 mm) Fine Pitch BGA BA48F



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Document Title:CY62157CV18MoBL2 (TM) 512K x 16 Static Ram Document Number: 38-05012				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106158	04/06/01	MGN	New Data Sheet, replaces CY62157BV18
*A	107242	07/31/01	MGN	Changing from Preliminary to Final