



128K x 8 Static RAM

Features

- **High speed**
— $t_{AA} = 10, 12, 15 \text{ ns}$
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with \overline{CE} and \overline{OE} options**
- **Functionally equivalent to CY7C1019V33**

Functional Description

The CY7C1019B/10191B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

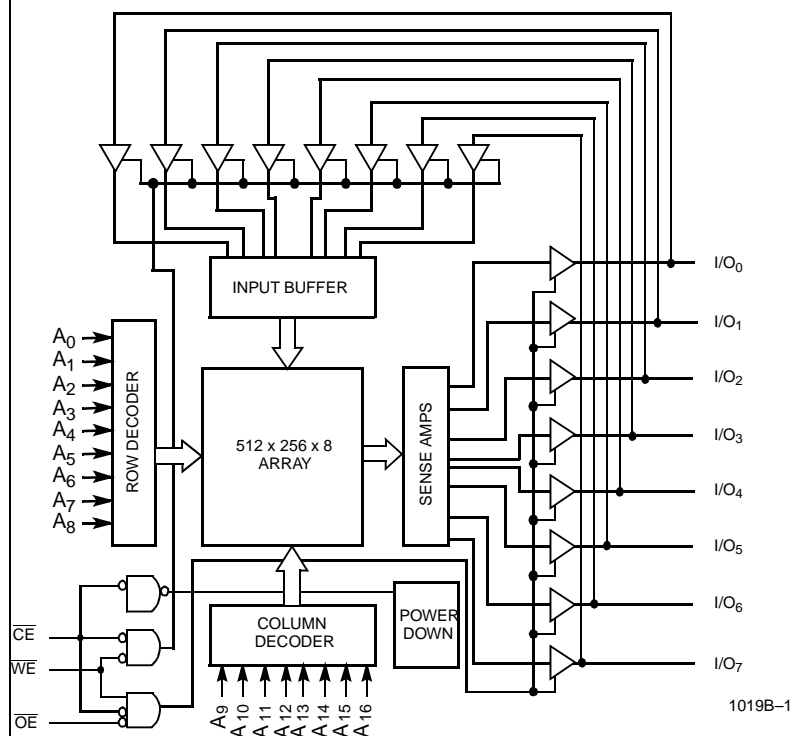
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

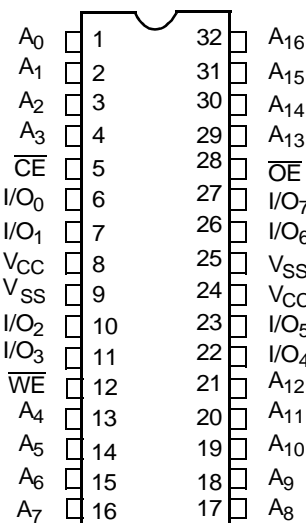
The CY7C1019B/10191B is available in standard 32-pin TSOP Type II and 400-mil-wide SOJ packages. Customers should use part number CY7C10191B when ordering parts with 10 ns t_{AA} , and CY7C1019B when ordering 12 and 15 ns t_{AA} .

Logic Block Diagram



Pin Configurations

SOJ / TSOP II Top View



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1019B-2

Selection Guide

		7C10191B-10	7C1019B-12	7C1019B-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)		150	140	130
Maximum Standby Current (mA)		10	10	10
	L	–	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with
Power Applied –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] –0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] –0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C10191B-10		7C1019B-12		7C1019B-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.},$ $I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.},$ $I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	–1	+1	–1	+1	–1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC},$ Output Disabled	–5	+5	–5	+5	–5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.},$ $I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		150		140		130	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. $V_{CC}, \overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		40		40		40	mA
			L	20		20		20	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. $V_{CC},$ $\overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V,$ or $V_{IN} \leq 0.3V, f = 0$		10		10		10	mA
			L	–		1		1	

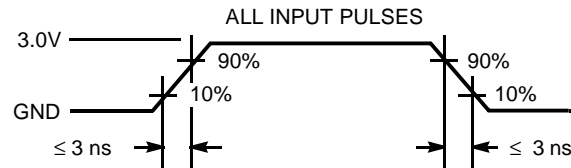
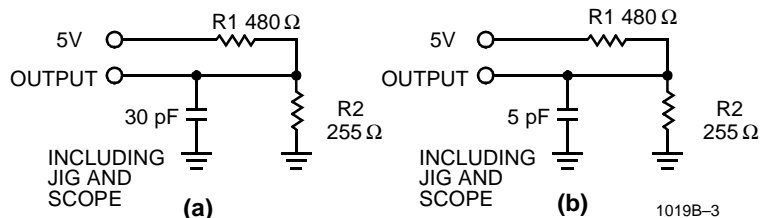
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 5.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

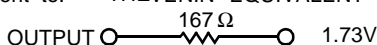
Notes:

- $V_{IL} (\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics^[4] Over the Operating Range

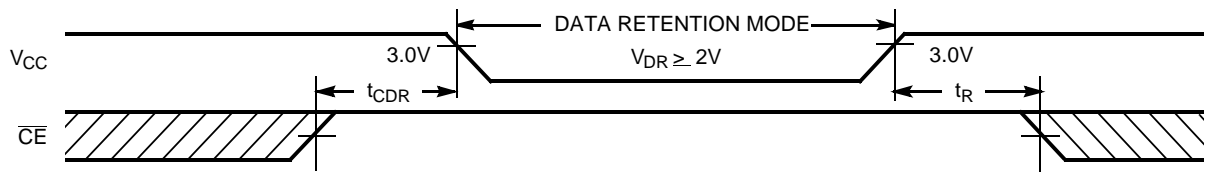
Parameter	Description	7C10191B-10		7C1019B-12		7C1019B-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	10		12		15		ns
t _{AA}	Address to Data Valid		10		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		10		12		15	ns
t _{DOE}	\overline{OE} LOW to Data Valid		5		6		7	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[5, 6]		5		6		7	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[5, 6]		5		6		7	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		10		12		15	ns
WRITE CYCLE ^[7, 8]								
t _{WC}	Write Cycle Time	10		12		15		ns
t _{SCE}	\overline{CE} LOW to Write End	8		9		10		ns
t _{AW}	Address Set-Up to Write End	7		8		10		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	7		8		10		ns
t _{SD}	Data Set-Up to Write End	5		6		8		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[5, 6]		5		6		7	ns

Notes:

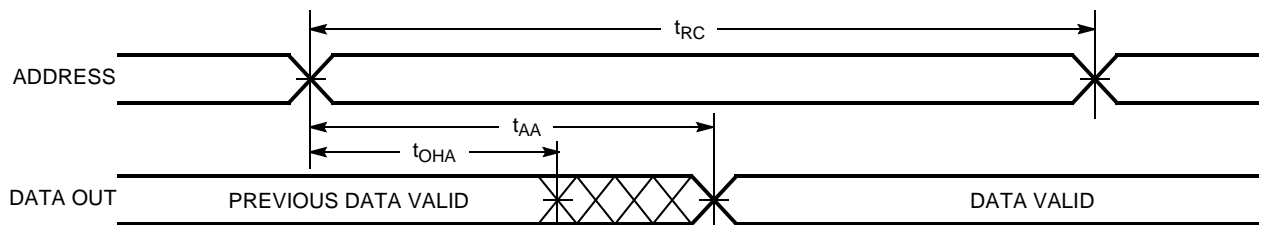
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range (L Version Only)

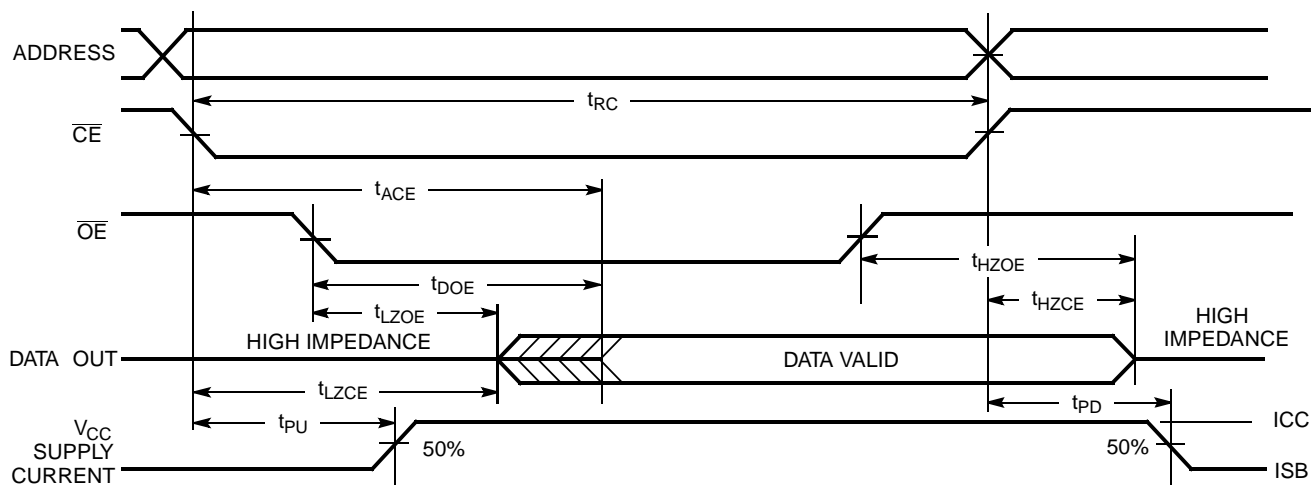
Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	No input may exceed $V_{CC} + 0.5V$	2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$,		300	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
t_R	Operation Recovery Time		200		μs

Data Retention Waveform


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Switching Waveforms
Read Cycle No. 1^[9, 10]


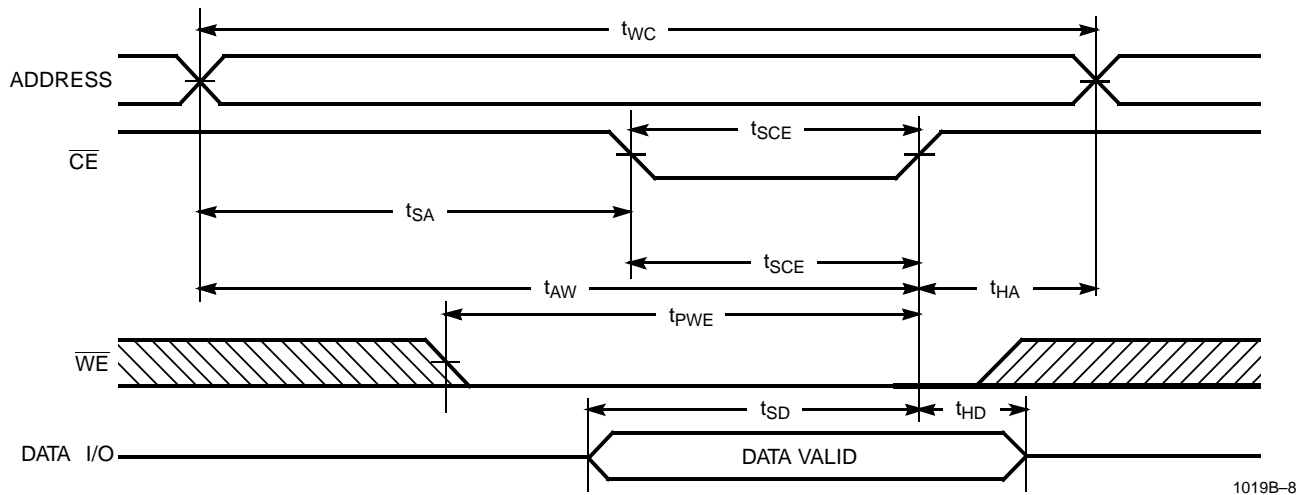
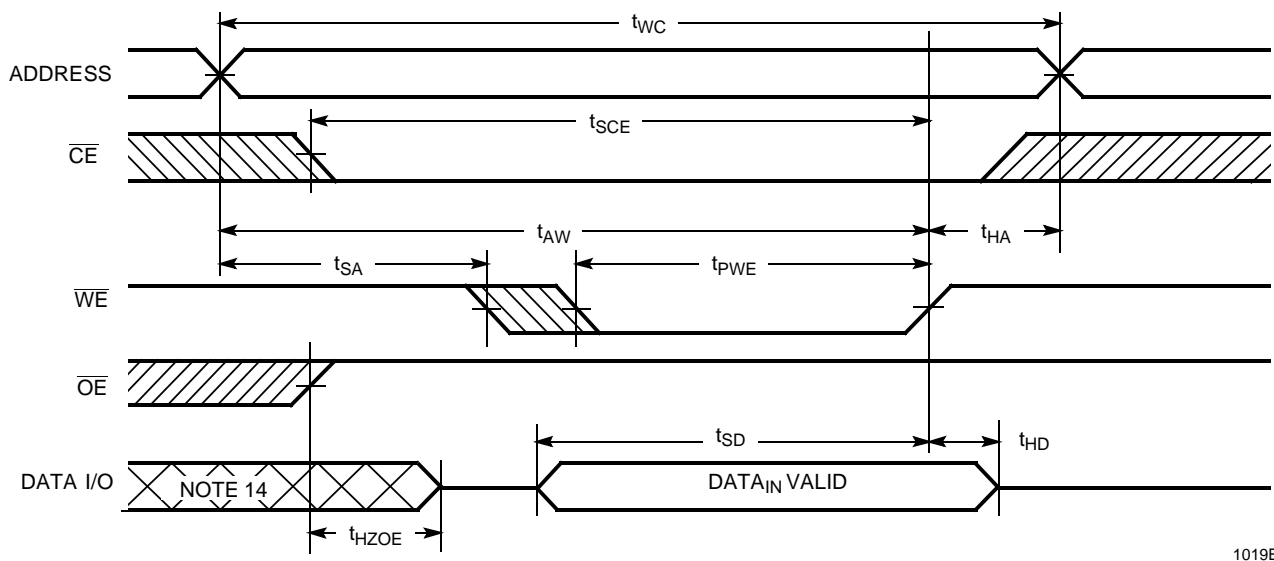
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Read Cycle No. 2 (\overline{OE} Controlled)^[10, 11]


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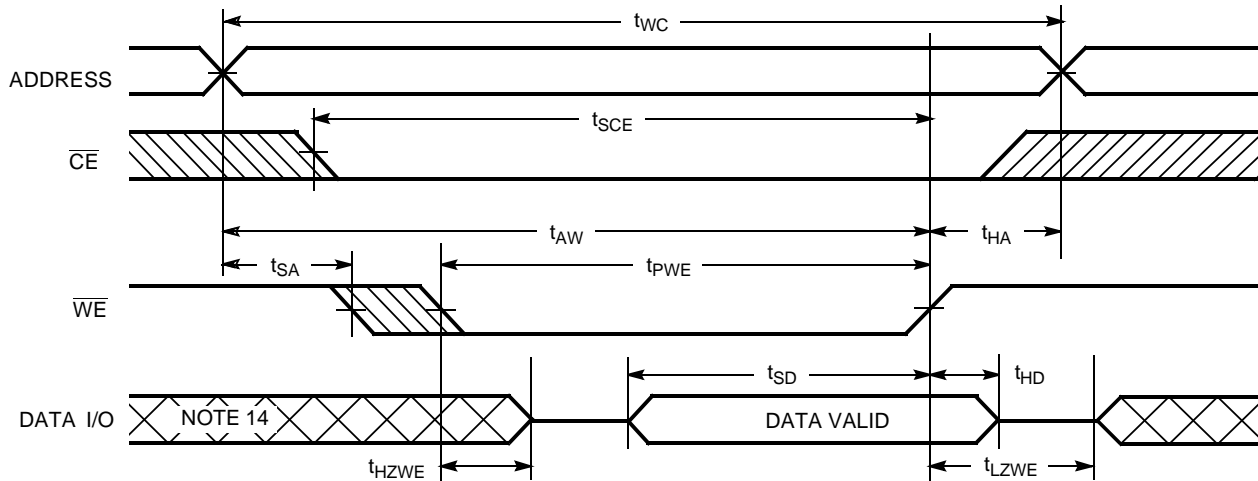
Notes:

9. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
10. \overline{WE} is HIGH for read cycle.
11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[12, 13]

Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[12, 13]

Notes:

12. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[13]


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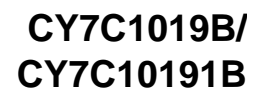
Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

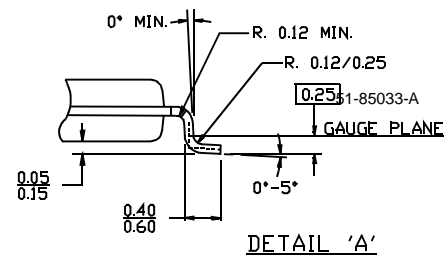
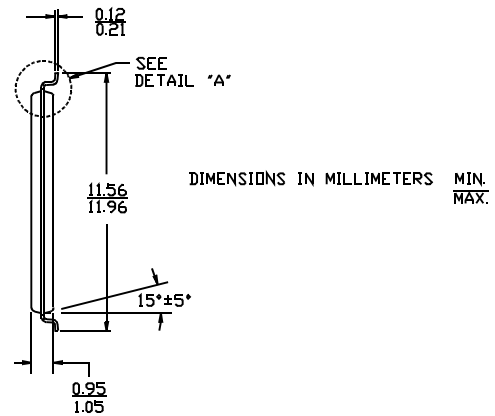
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C10191B-10VC	V33	32-Lead 400-Mil Molded SOJ	Commercial
12	CY7C1019B-12VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019B-12ZC	ZS32	32-Lead TSOP Type II	
15	CY7C1019B-15VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019B-15ZC	ZS32	32-Lead TSOP Type II	

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32-Lead (400-Mil) Molded SOJ V33



Package Diagram (continued)

32-Lead TSOP II ZS32

