



CY7C1041

256K x 16 Static RAM

Features

- **High speed**
— $t_{AA} = 15 \text{ ns}$
- **Low active power**
— 1430 mW (max.)
- **Low CMOS standby power (L version)**
— 2.75 mW (max.)
- **2.0V Data Retention (400 μW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**

Functional Description

The CY7C1041 is a high-performance CMOS static RAM organized as 262,144 words by 16 bits.

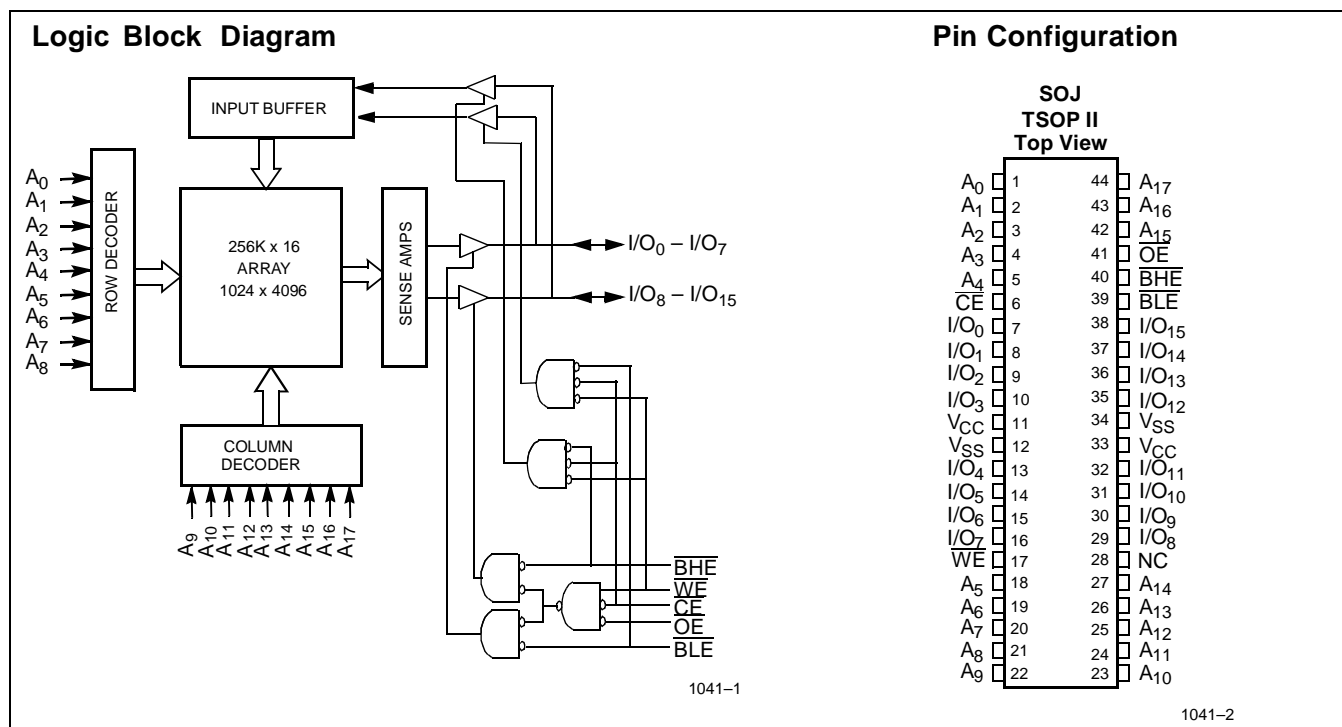
Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is

written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), the $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1041 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.



Selection Guide

| | | 7C1041-12 | 7C1041-15 | 7C1041-17 | 7C1041-20 | 7C1041-25 |
|-----------------------------------|---------|-----------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns) | | 12 | 15 | 17 | 20 | 25 |
| Maximum Operating Current (mA) | | 280 | 260 | 250 | 230 | 220 |
| Maximum CMOS Standby Current (mA) | Com'l | 3 | 3 | 3 | 3 | 3 |
| | Com'l L | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| | Ind'l | 6 | 6 | 6 | 6 | 6 |

Shaded areas contain preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Operating Range

| Range | Ambient Temperature ^[2] | V_{CC} |
|------------|------------------------------------|----------|
| Commercial | 0°C to +70°C | 5V ± 0.5 |
| Industrial | -40°C to +85°C | |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C1041-12 | | 7C1041-15 | | 7C1041-17 | | Unit |
|-----------|---|---|-----------|----------------|-----------|----------------|-----------|----------------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.5$ | 2.2 | $V_{CC} + 0.5$ | 2.2 | $V_{CC} + 0.5$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_{OUT} \leq V_{CC}$, Output Disabled | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.},$ $f = f_{MAX} = 1/t_{RC}$ | | 280 | | 260 | | 250 | mA |
| I_{SB1} | Automatic CE Power-Down Current — TTL Inputs | Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | | 40 | | 40 | | 40 | mA |
| I_{SB2} | Automatic CE Power-Down Current — CMOS Inputs | Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$ | Com'l | | | 3 | | 3 | mA |
| | | | Com'l L | | | 0.5 | | 0.5 | mA |
| | | | Ind'l | | | 6 | | 6 | mA |

Shaded areas contain preliminary information.

Notes:

- $V_{IL}(\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- T_A is the case temperature.

Electrical Characteristics Over the Operating Range (continued)

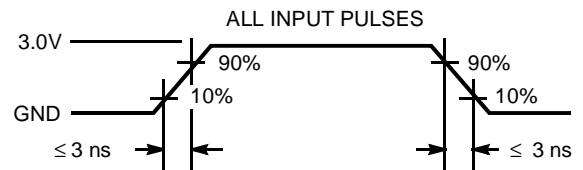
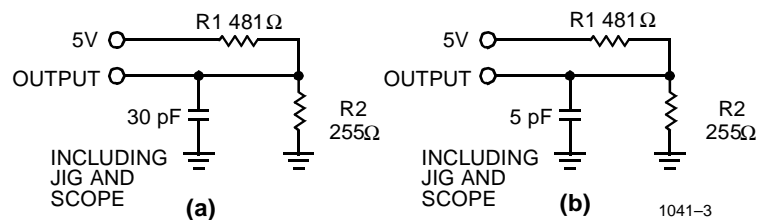
| Parameter | Description | Test Conditions | 7C1041-20 | | 7C1041-25 | | Unit |
|-----------|--|--|-----------|----------------|-----------|----------------|---------------|
| | | | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.5$ | 2.2 | $V_{CC} + 0.5$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_{OUT} \leq V_{CC}$, Output Disabled | -1 | +1 | -1 | +1 | μA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}$, $f = f_{\text{MAX}} = 1/t_{RC}$ | | 230 | | 220 | mA |
| I_{SB1} | Automatic CE Power-Down Current —TTL Inputs | Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{\text{MAX}}$ | | 40 | | 40 | mA |
| I_{SB2} | Automatic CE Power-Down Current —CMOS Inputs | Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$, or $V_{IN} \leq 0.3\text{V}$, $f = 0$ | Com'l | 3 | | 3 | mA |
| | | | Com'l L | 0.5 | | 0.5 | mA |
| | | | Ind'l | 6 | | 6 | mA |

Capacitance^[3]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|-------------------|--|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0\text{V}$ | 8 | pF |
| C_{OUT} | I/O Capacitance | | 8 | pF |

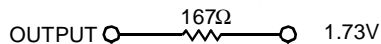
Note:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


1041-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics^[4] Over the Operating Range

| Parameter | Description | 7C1041-12 | | 7C1041-15 | | 7C1041-17 | | Unit |
|-------------------------------|--|-----------|------|-----------|------|-----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 12 | | 15 | | 17 | | ns |
| t _{AA} | Address to Data Valid | | 12 | | 15 | | 17 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 12 | | 15 | | 17 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 6 | | 7 | | 7 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z | 0 | | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[5, 6] | | 6 | | 7 | | 7 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[6] | 3 | | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[5, 6] | | 6 | | 7 | | 7 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 12 | | 15 | | 17 | ns |
| t _{DBE} | Byte Enable to Data Valid | | 6 | | 7 | | 7 | ns |
| t _{LZBE} | Byte Enable to Low Z | 0 | | 0 | | 0 | | ns |
| t _{HZBE} | Byte Disable to High Z | | 6 | | 7 | | 7 | ns |
| WRITE CYCLE ^[7, 8] | | | | | | | | |
| t _{WC} | Write Cycle Time | 12 | | 15 | | 17 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 10 | | 12 | | 14 | | ns |
| t _{AW} | Address Set-Up to Write End | 10 | | 12 | | 14 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 10 | | 12 | | 14 | | ns |
| t _{SD} | Data Set-Up to Write End | 7 | | 8 | | 8 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[6] | 3 | | 3 | | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[5, 6] | | 6 | | 7 | | 7 | ns |
| t _{BW} | Byte Enable to End of Write | 10 | | 12 | | 12 | | ns |

Shaded areas contain preliminary information.

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Characteristics^[4] Over the Operating Range (continued)

| Parameter | Description | 7C1041-20 | | 7C1041-25 | | Unit |
|-------------------------------|--|-----------|------|-----------|------|------|
| | | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | |
| t _{RC} | Read Cycle Time | 20 | | 25 | | ns |
| t _{AA} | Address to Data Valid | | 20 | | 25 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 5 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 20 | | 25 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 8 | | 10 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[5, 6] | | 8 | | 10 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[6] | 3 | | 5 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[5, 6] | | 8 | | 10 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 20 | | 25 | ns |
| t _{DBE} | Byte Enable to Data Valid | | 8 | | 10 | ns |
| t _{LZBE} | Byte Enable to Low Z | 0 | | 0 | | ns |
| t _{HZBE} | Byte Disable to High Z | | 8 | | 10 | ns |
| WRITE CYCLE ^[7, 8] | | | | | | |
| t _{WC} | Write Cycle Time | 20 | | 25 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 13 | | 15 | | ns |
| t _{AW} | Address Set-Up to Write End | 13 | | 15 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 13 | | 15 | | ns |
| t _{SD} | Data Set-Up to Write End | 9 | | 10 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[6] | 3 | | 5 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[5, 6] | | 8 | | 10 | ns |
| t _{BW} | Byte Enable to End of Write | 13 | | 15 | | ns |

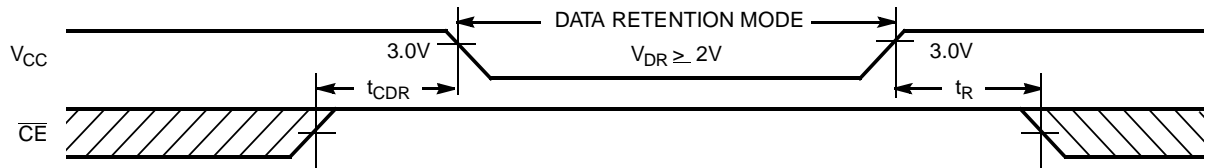
Data Retention Characteristics Over the Operating Range

| Parameter | Description | | Conditions ^[10] | Min. | Max. | Unit |
|---------------------------------|--------------------------------------|---------|---|------------|------|------|
| V _{DR} | V _{CC} for Data Retention | | | 2.0 | | V |
| I _{CCDR} | Data Retention Current | | V _{CC} = V _{DR} = 2.0V, CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V | | | μA |
| | | Com'l L | | | 200 | μA |
| | | | | | | μA |
| t _{CDR} ^[3] | Chip Deselect to Data Retention Time | | | 0 | | ns |
| t _R ^[9] | Operation Recovery Time | | | See Note 9 | | |

Notes:

9. t_r ≤ 100 μs for all speeds.
10. No input may exceed V_{CC} + 0.5V.

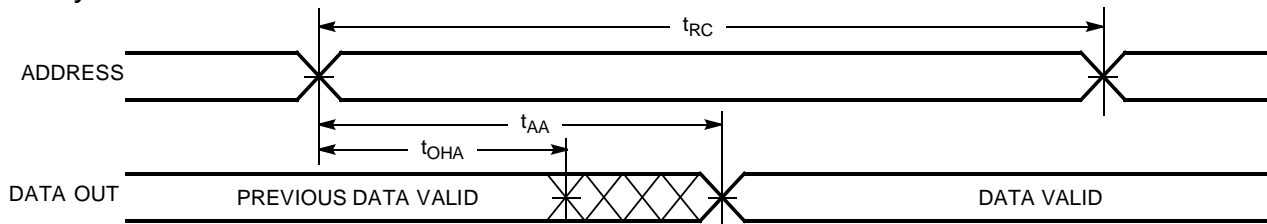
Data Retention Waveform



1041-5

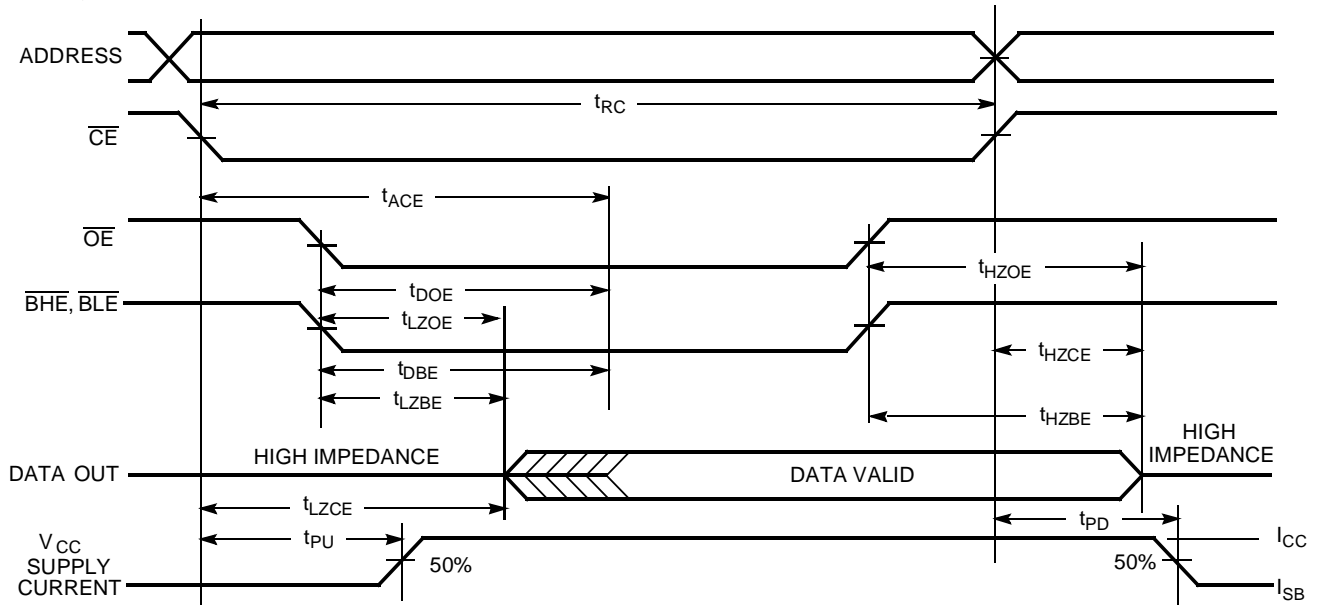
Switching Waveforms

Read Cycle No.1^[11, 12]



1041-6

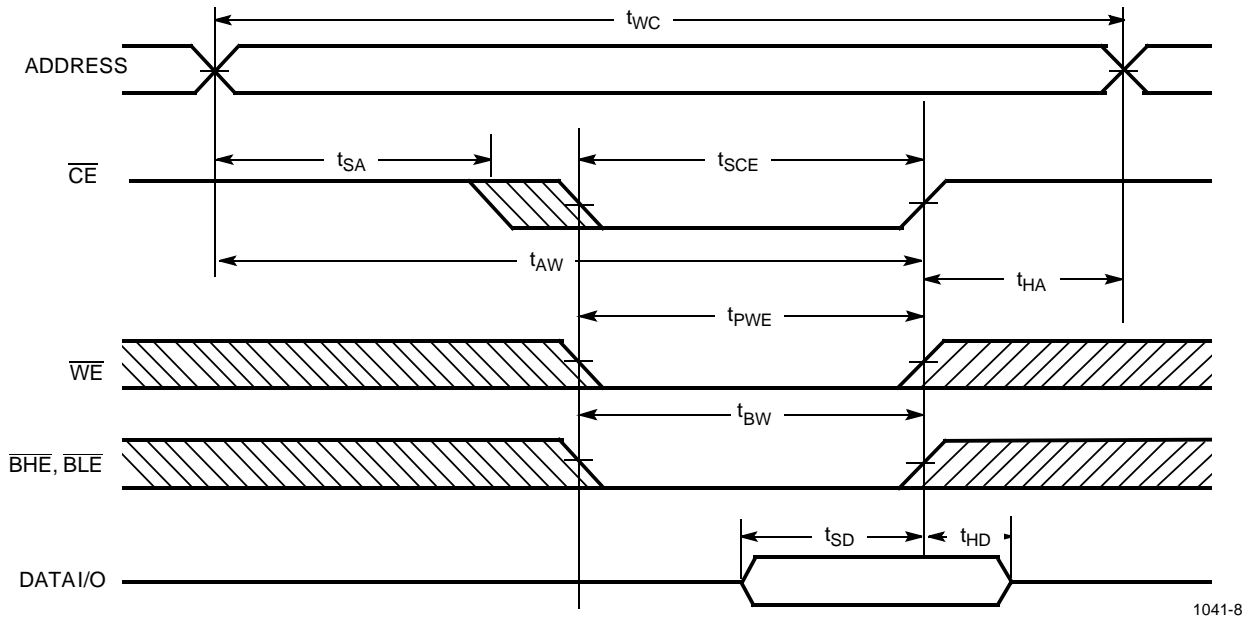
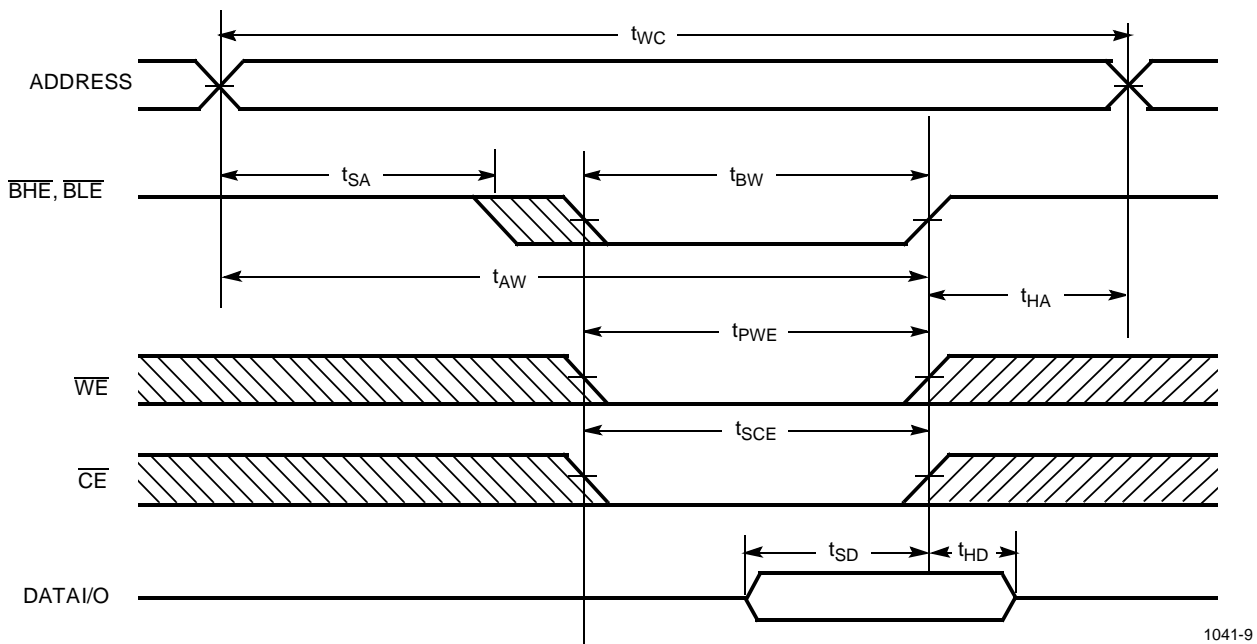
Read Cycle No.2 (\overline{OE} Controlled)^[12, 13]



1041-7

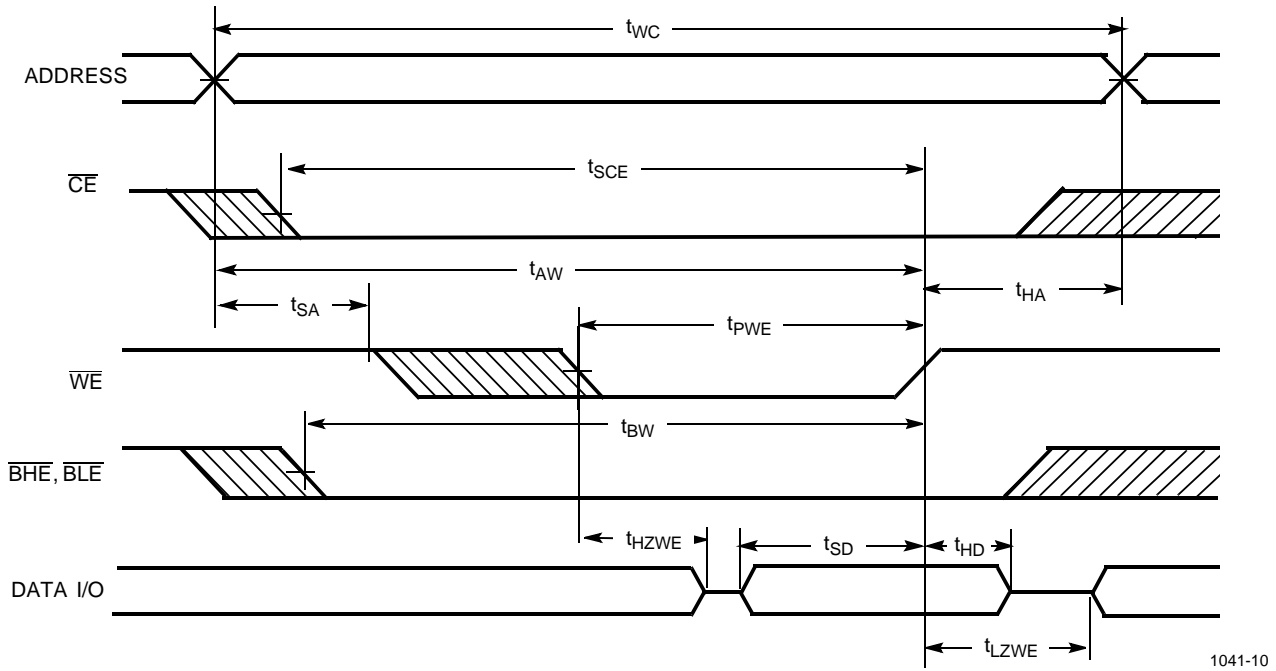
Notes:

11. Device is continuously selected. $\overline{OE}, \overline{CE}, \overline{BHE}$, and/or $\overline{BLE} = V_{IL}$.
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) ^[14, 15]

Write Cycle No. 2 ($\overline{\text{BL E}}$ or $\overline{\text{BHE}}$ Controlled)

Notes:

14. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BL E}} = V_{\text{IH}}$.
15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No.3 (\overline{WE} Controlled, LOW)

Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ –I/O ₇ | I/O ₈ –I/O ₁₅ | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------------|----------------------|
| H | X | X | X | X | High Z | High Z | Power Down | Standby (I_{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read All Bits | Active (I_{CC}) |
| L | L | H | L | H | Data Out | High Z | Read Lower Bits Only | Active (I_{CC}) |
| L | L | H | H | L | High Z | Data Out | Read Upper Bits Only | Active (I_{CC}) |
| L | X | L | L | L | Data In | Data In | Write All Bits | Active (I_{CC}) |
| L | X | L | L | H | Data In | High Z | Write Lower Bits Only | Active (I_{CC}) |
| L | X | L | H | L | High Z | Data In | Write Upper Bits Only | Active (I_{CC}) |
| L | H | H | X | X | High Z | High Z | Selected, Outputs Disabled | Active (I_{CC}) |

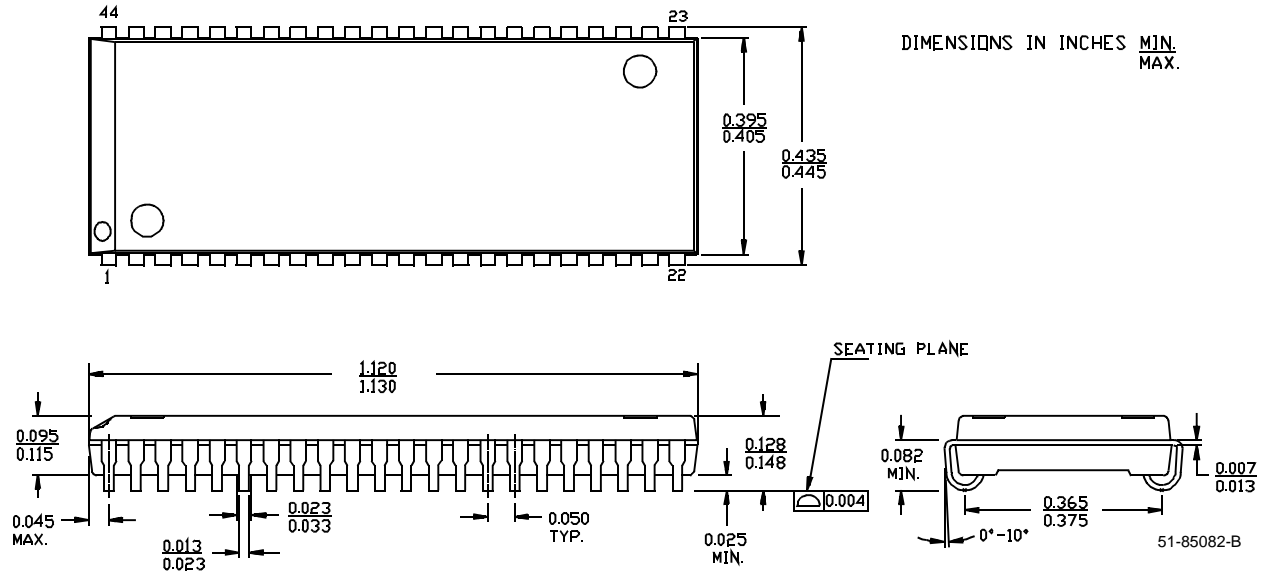
Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|----------------|--------------|------------------------------|-----------------|
| 15 | CY7C1041-15VC | V34 | 44-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1041L-15VC | V34 | 44-Lead (400-Mil) Molded SOJ | |
| | CY7C1041-15ZC | Z44 | 44-Lead TSOP Type II | |
| | CY7C1041L-15ZC | Z44 | 44-Lead TSOP Type II | |
| 17 | CY7C1041-17VC | V34 | 44-Lead (400-Mil) Molded SOJ | |
| | CY7C1041L-17VC | V34 | 44-Lead (400-Mil) Molded SOJ | |
| | CY7C1041-17ZC | Z44 | 44-Lead TSOP Type II | |
| | CY7C1041L-17ZC | Z44 | 44-Lead TSOP Type II | |
| 20 | CY7C1041-20VC | V34 | 44-Lead (400-Mil) Molded SOJ | |
| | CY7C1041L-20VC | V34 | 44-Lead (400-Mil) Molded SOJ | |
| | CY7C1041-20ZC | Z44 | 44-Lead TSOP Type II | |
| | CY7C1041L-20ZC | Z44 | 44-Lead TSOP Type II | |
| 25 | CY7C1041-25VC | V34 | 44-Lead (400-Mil) Molded SOJ | |
| | CY7C1041L-25VC | V34 | 44-Lead (400-Mil) Molded SOJ | |
| | CY7C1041-25ZC | Z44 | 44-Lead TSOP Type II | |
| | CY7C1041L-25ZC | Z44 | 44-Lead TSOP Type II | |
| 15 | CY7C1041-15ZI | Z44 | 44-Lead TSOP Type II | Industrial |
| | CY7C1041-15VI | V34 | 44-Lead (400-Mil) Molded SOJ | |
| 17 | CY7C1041-17ZI | V34 | 44-Lead TSOP Type II | |
| | CY7C1041-17VI | Z44 | 44-Lead (400-Mil) Molded SOJ | |
| 20 | CY7C1041-20ZI | Z44 | 44-Lead TSOP Type II | |
| | CY7C1041-20VI | Z44 | 44-Lead (400-Mil) Molded SOJ | |
| 25 | CY7C1041-25ZI | Z44 | 44-Lead TSOP Type II | |
| | CY7C1041-25VI | Z44 | 44-Lead (400-Mil) Molded SOJ | |

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Package Diagrams

44-Lead (400-Mil) Molded SOJ V34



44-Pin TSOP II Z44

DIMENSION IN MM (INCH)
MAX.
MIN.

