



CYPRESS

PRELIMINARY

CY7C1046BV33

1M x 4 Static RAM

## Features

- **High speed**  
—  $t_{AA} = 10 \text{ ns}$
- **Low active power for 10 ns speed**  
— 540 mW (max.)
- **Low CMOS standby power (L version)**  
— 1.8 mW (max.)
- **2.0V Data Retention (400  $\mu\text{W}$  at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**

## Functional Description

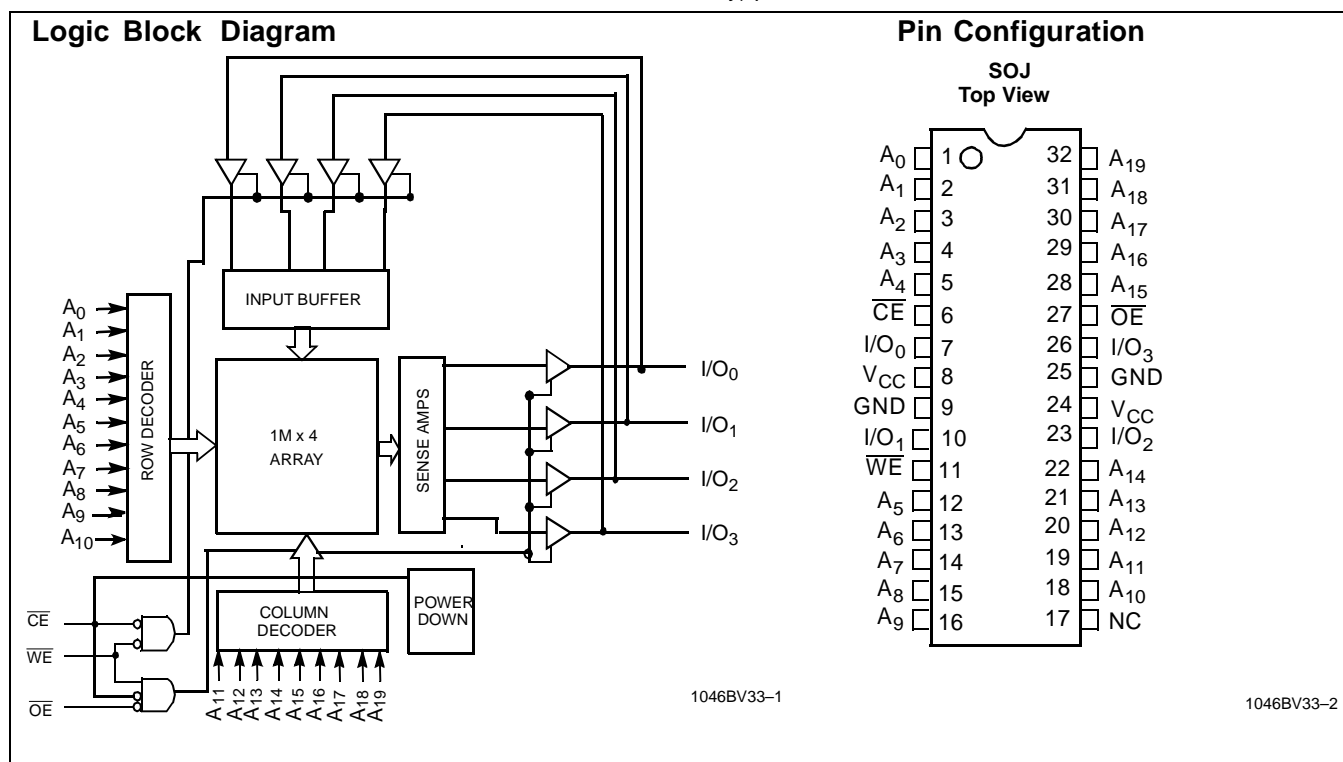
The CY7C1046BV33 is a high-performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory

expansion is provided by an active LOW Chip Enable ( $\overline{\text{CE}}$ ), an active LOW Output Enable ( $\overline{\text{OE}}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the four I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_3$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{19}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_3$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1046BV33 is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.



## Selection Guide

		7C1046BV33-10	7C1046BV33-12	7C1046BV33-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)		150	140	130
Maximum CMOS Standby Current (mA)	Com'l	8	8	8
	L version	0.5	0.5	0.5

Shaded areas contain advance information.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs  
in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	3.0V - 3.6V

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1046BV33-10		7C1046BV33-12		7C1046BV33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = −4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	2.2	V <sub>CC</sub> + 0.5	2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	−1	+1	−1	+1	−1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	−1	+1	−1	+1	−1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		150		140		130	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		20		20		20	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	8		8		8	mA
		L version		0.5		0.5		0.5	

Shaded areas contain advance information.

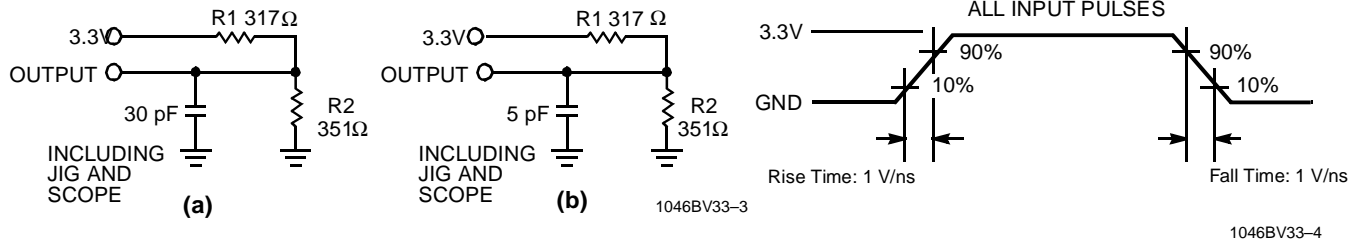
## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 3.3V$	6	pF
$C_{OUT}$	I/O Capacitance		6	pF

### Notes:

- $V_{IL} (\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

OUTPUT  $\text{---} 167\Omega \text{---} 1.73\text{V}$

## Switching Characteristics<sup>[4]</sup> Over the Operating Range

Parameter	Description	7C1046BV33-10		7C1046BV33-12		7C1046BV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t <sub>RC</sub>	Read Cycle Time	10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		4		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
WRITE CYCLE <sup>[7, 8]</sup>								
t <sub>WC</sub>	Write Cycle Time	10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	7		10		12		ns
t <sub>AW</sub>	Address Set-Up to Write End	7		10		12		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	7		10		12		ns
t <sub>SD</sub>	Data Set-Up to Write End	5		7		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		5		6		7	ns

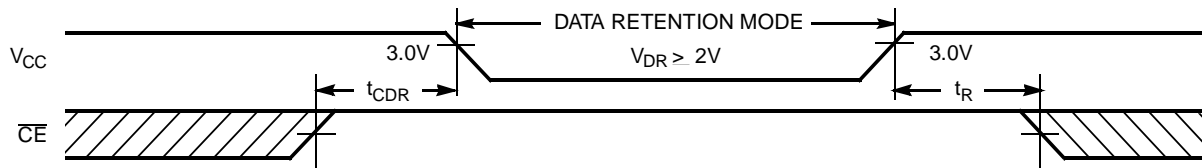
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### Notes:

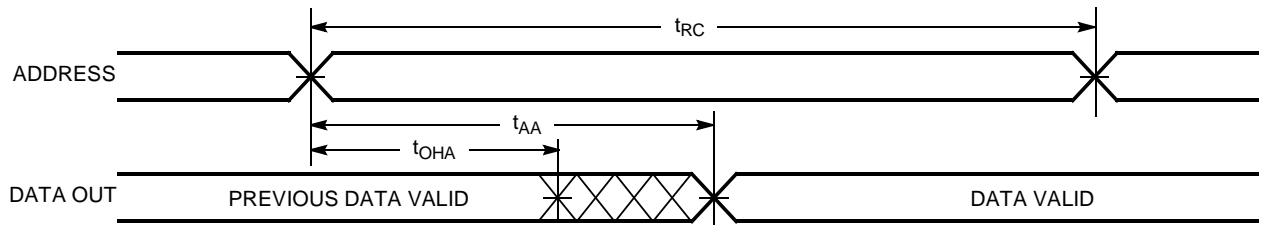
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range

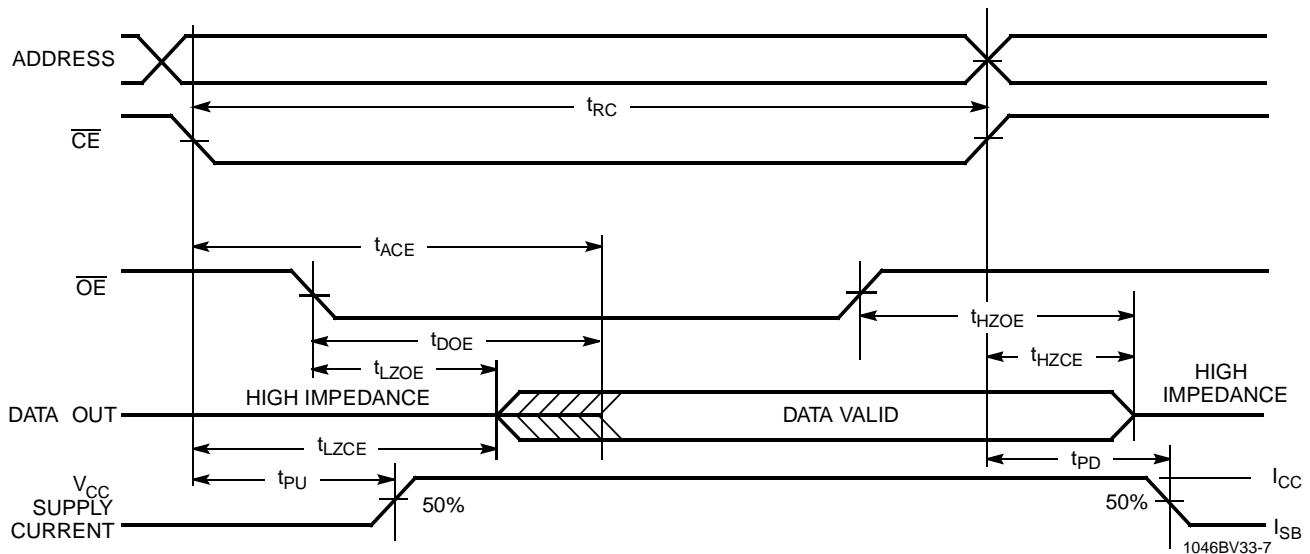
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	Com'l		200	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[9]}$	Operation Recovery Time		10		$\mu s$

**Data Retention Waveform**


1046BV33-5

**Switching Waveforms**
**Read Cycle No. 1<sup>[11, 12]</sup>**


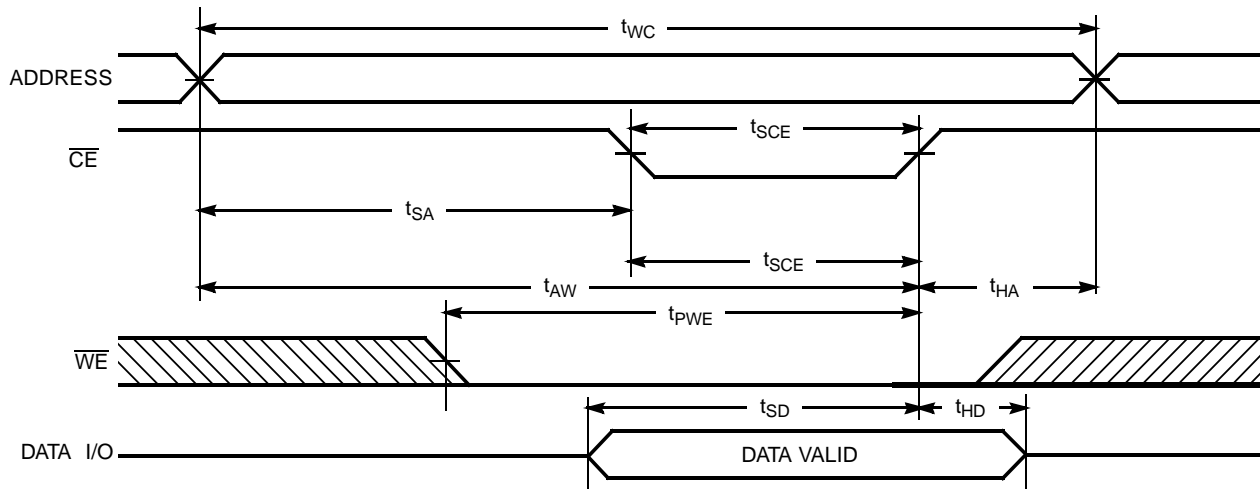
1046BV33-6

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[12, 13]</sup>**


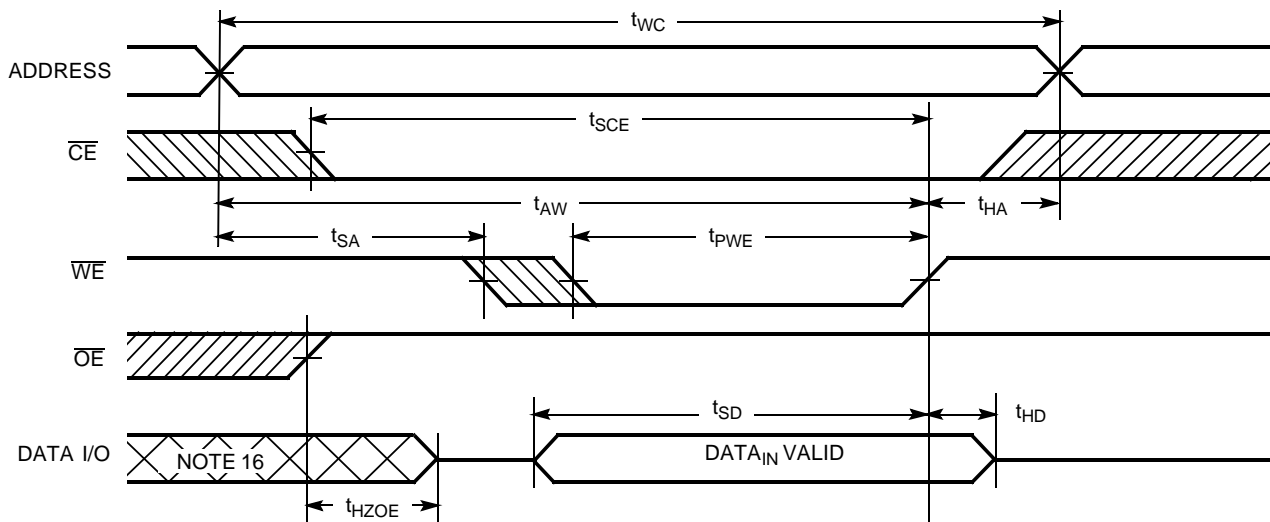
1046BV33-7

**Notes:**

9.  $t_r \leq 3$  ns for the -10, -12, and -15 speeds.
10. No input may exceed  $V_{CC} + 0.5V$ .
11. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[14, 15]</sup>**


1046BV33-8

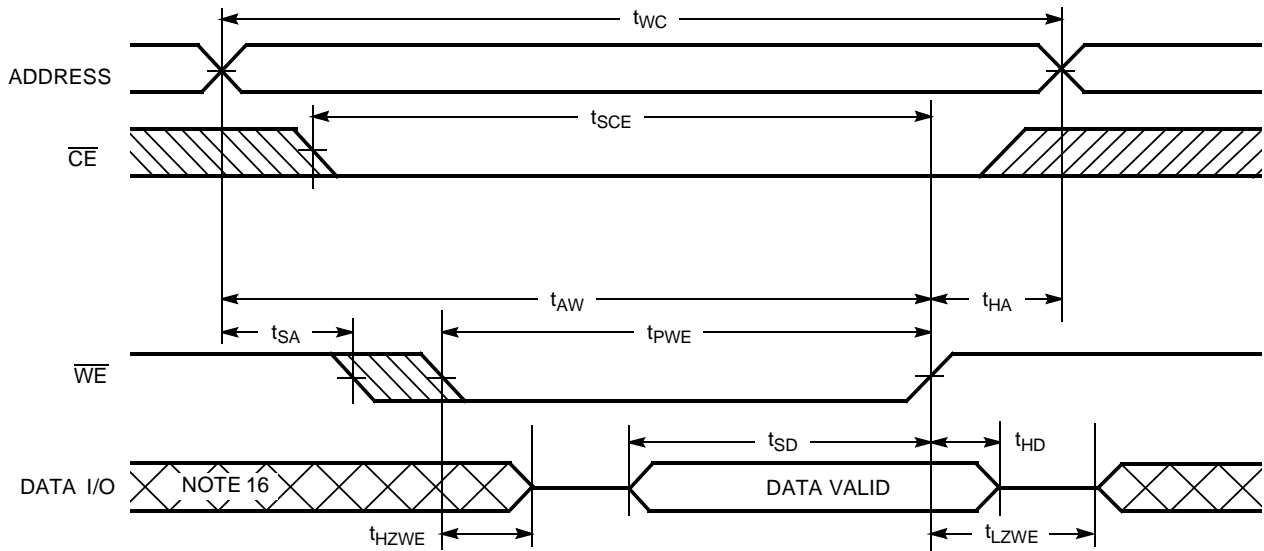
**Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write)<sup>[14, 15]</sup>**


1046BV33-9

**Notes:**

14. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[15]</sup>**


1046BV33-10

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> - I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1046BV33-10VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
12	CY7C1046BV33-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046BV33-15VC	V33	32-Lead (400-Mil) Molded SOJ	
10	CY7C1046BV33L-10VC	V33	32-Lead (400-Mil) Molded SOJ	
12	CY7C1046BV33L-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046BV33L-15VC	V33	32-Lead (400-Mil) Molded SOJ	

Shaded areas contain pre-release information.

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## Package Diagram

### 32-Lead (400-Mil) Molded SOJ V33

DIMENSIONS IN INCHES MIN. MAX.

