



CYPRESS

PRELIMINARY

CY7C1049

512K x 8 Static RAM

Features

- **High speed**
 - $t_{AA} = 15 \text{ ns}$
- **Low active power**
 - 1210 mW (max.)
- **Low CMOS standby power (Commercial L version)**
 - 2.75 mW (max.)
- **2.0V Data Retention (400 μW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**

Functional Description

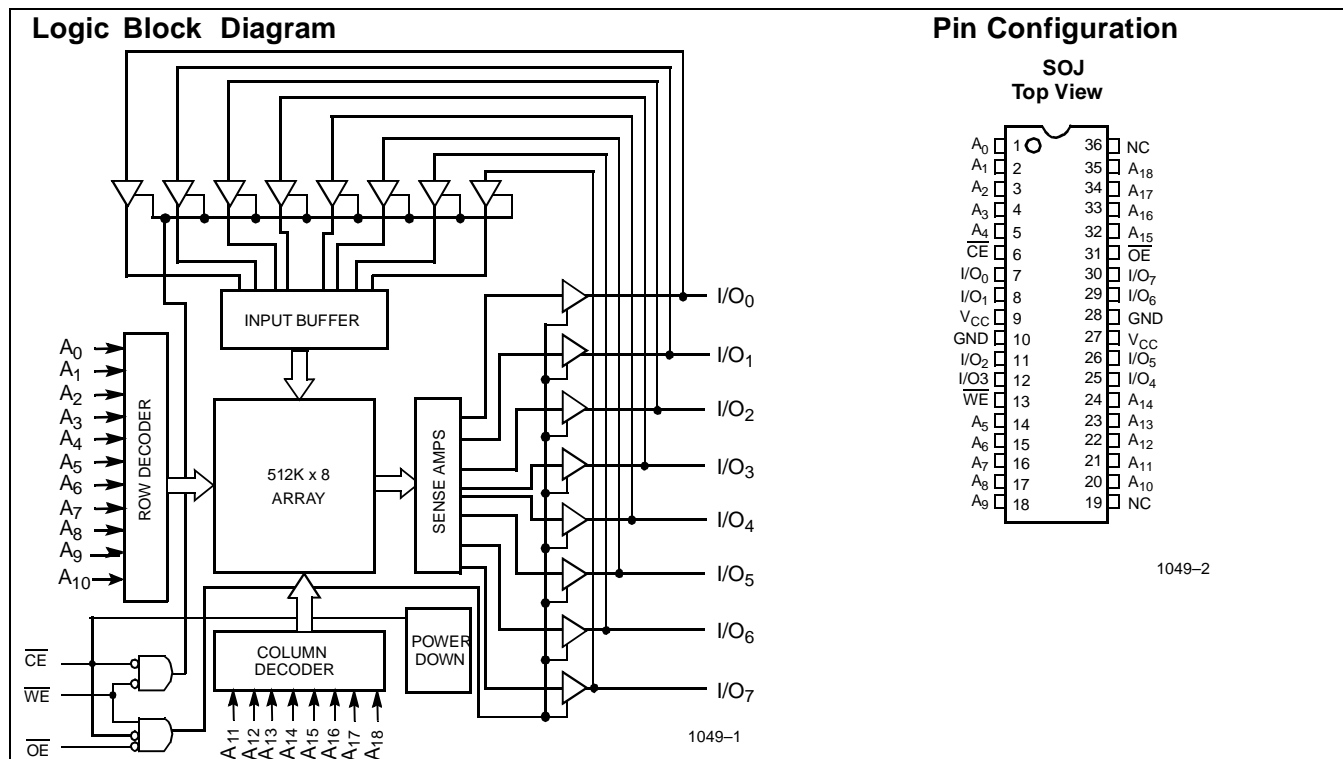
The CY7C1049 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion

is provided by an active LOW chip enable ($\overline{\text{CE}}$), an active LOW output enable ($\overline{\text{OE}}$), and three-state drivers. Writing to the device is accomplished by taking chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) LOW while forcing write enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1049 is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.



Selection Guide

| | | 7C1049-12 | 7C1049-15 | 7C1049-17 | 7C1049-20 | 7C1049-25 |
|-----------------------------------|----------|-----------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns) | | 12 | 15 | 17 | 20 | 25 |
| Maximum Operating Current (mA) | | 240 | 220 | 195 | 185 | 180 |
| Maximum CMOS Standby Current (mA) | Com'l | 8 | 8 | 8 | 8 | 8 |
| | Com'l L | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| | Ind'l | 9 | 9 | 9 | 9 | 9 |
| | Military | | | | 10 | 10 |

Shaded areas contain advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

| Range | Ambient Temperature ^[2] | V_{CC} |
|------------|------------------------------------|-----------|
| Commercial | 0°C to +70°C | 4.5V–5.5V |
| Industrial | -40°C to +85°C | |
| Military | -55°C to +125°C | |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C1049-12 | | 7C1049-15 | | 7C1049-17 | | Unit |
|-----------|---|---|-----------|----------------|-----------|----------------|-----------|----------------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3$ | 2.2 | $V_{CC} + 0.3$ | 2.2 | $V_{CC} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.3 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_{OUT} \leq V_{CC}$, Output Disabled | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}$ $f = f_{MAX} = 1/t_{RC}$ | | 240 | | 220 | | 195 | mA |
| I_{SB1} | Automatic CE Power-Down Current — TTL Inputs | Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | | 40 | | 40 | | 40 | mA |
| I_{SB2} | Automatic CE Power-Down Current — CMOS Inputs | Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f=0$ | Com'l | | | 8 | | 8 | mA |
| | | | Com'l L | | | 0.5 | | 0.5 | mA |
| | | | Ind'l | | | 9 | | 9 | mA |
| | | | Military | | | 10 | | 10 | mA |

Shaded areas contain advance information.

Notes:

- $V_{IL}(\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range (continued)

| Parameter | Description | Test Conditions | 7C1049-20 | | 7C1049-25 | | Unit |
|-----------|--|---|-----------|----------------|-----------|----------------|---------------|
| | | | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3$ | 2.2 | $V_{CC} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_{OUT} \leq V_{CC}$, Output Disabled | -1 | +1 | -1 | +1 | μA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}$, $f = f_{MAX} = 1/t_{RC}$ | | 185 | | 180 | mA |
| I_{SB1} | Automatic CE Power-Down Current —TTL Inputs | Max. V_{CC} , $CE \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | | 40 | | 40 | mA |
| I_{SB2} | Automatic CE Power-Down Current —CMOS Inputs | Max. V_{CC} , $CE \geq V_{CC} - 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$, or $V_{IN} \leq 0.3\text{V}$, $f=0$ | Com'l | | | 8 | mA |
| | | | Com'l L | | | 0.5 | mA |
| | | | Ind'l | | | 9 | mA |
| | | | Military | | | 10 | mA |

Capacitance^[3]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|-------------------|--|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0\text{V}$ | 8 | pF |
| C_{OUT} | I/O Capacitance | | 8 | pF |

Note:

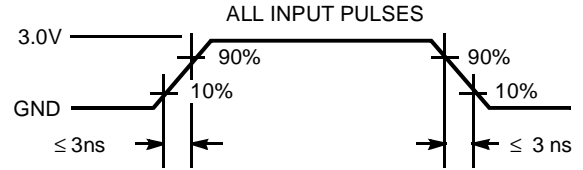
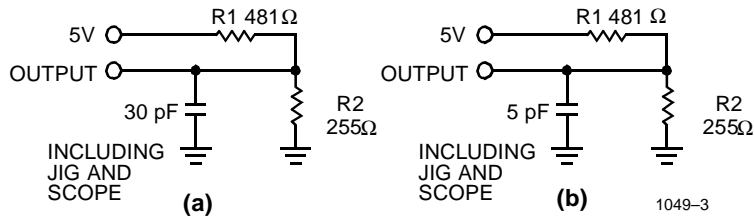
3. Tested initially and after any design or process changes that may affect these parameters.



PRELIMINARY

CY7C1049

AC Test Loads and Waveforms



1049-4

Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT $\text{---} \frac{167\Omega}{\text{---}} \text{---} 1.73\text{V}$

Switching Characteristics^[4] Over the Operating Range

| Parameter | Description | 7C1049-12 | | 7C1049-15 | | 7C1049-17 | | Unit |
|------------------------------|--|-----------|------|-----------|------|-----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 12 | | 15 | | 17 | | ns |
| t _{AA} | Address to Data Valid | | 12 | | 15 | | 17 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 12 | | 15 | | 17 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 6 | | 7 | | 8 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[6] | 0 | | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[5, 6] | | 6 | | 7 | | 7 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[6] | 3 | | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[5, 6] | | 6 | | 7 | | 7 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 12 | | 15 | | 17 | ns |
| WRITE CYCLE ^[7,8] | | | | | | | | |
| t _{WC} | Write Cycle Time | 12 | | 15 | | 17 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 10 | | 12 | | 12 | | ns |
| t _{AW} | Address Set-Up to Write End | 10 | | 12 | | 12 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 10 | | 12 | | 12 | | ns |
| t _{SD} | Data Set-Up to Write End | 7 | | 8 | | 8 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[6] | 3 | | 3 | | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[5, 6] | | 6 | | 7 | | 8 | ns |

Shaded areas contain advance information.

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Characteristics^[4] Over the Operating Range (continued)

| Parameter | Description | 7C1049-20 | | 7C1049-25 | | Unit |
|----------------------------|--|-----------|------|-----------|------|------|
| | | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | |
| t _{RC} | Read Cycle Time | 20 | | 25 | | ns |
| t _{AA} | Address to Data Valid | | 20 | | 25 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 5 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 20 | | 25 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 8 | | 10 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[6] | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[5, 6] | | 8 | | 10 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[6] | 3 | | 5 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[5, 6] | | 8 | | 10 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 20 | | 25 | ns |
| WRITE CYCLE ^[7] | | | | | | |
| t _{WC} | Write Cycle Time | 20 | | 25 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 13 | | 15 | | ns |
| t _{AW} | Address Set-Up to Write End | 13 | | 15 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 13 | | 15 | | ns |
| t _{SD} | Data Set-Up to Write End | 9 | | 10 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[6] | 3 | | 5 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[5, 6] | | 8 | | 10 | ns |

Data Retention Characteristics Over the Operating Range

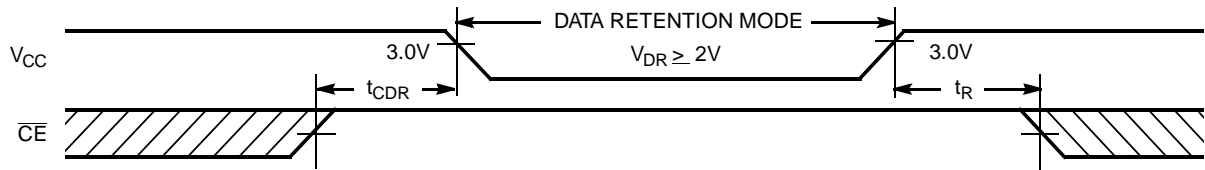
| Parameter | Description | | | Conditions ^[10] | Min. | Max | Unit |
|---------------------------------|--------------------------------------|----------|---|--|-----------------|-----|------|
| V _{DR} | V _{CC} for Data Retention | | | | 2.0 | | V |
| I _{CCDR} | Data Retention Current | Com'l | L | V _{CC} = V _{DR} = 3.0V, CE ≥ V _{CC} − 0.3V V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V | | 200 | μA |
| | | Ind'l | | | | 1 | mA |
| | | Military | | | | 2 | mA |
| t _{CDR} ^[3] | Chip Deselect to Data Retention Time | | | | 0 | | ns |
| t _R ^[9] | Operation Recovery Time | | | | t _{RC} | | ns |

Notes:

9. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 ns and slower speeds.

10. No input may exceed $V_{CC} + 0.5V$.

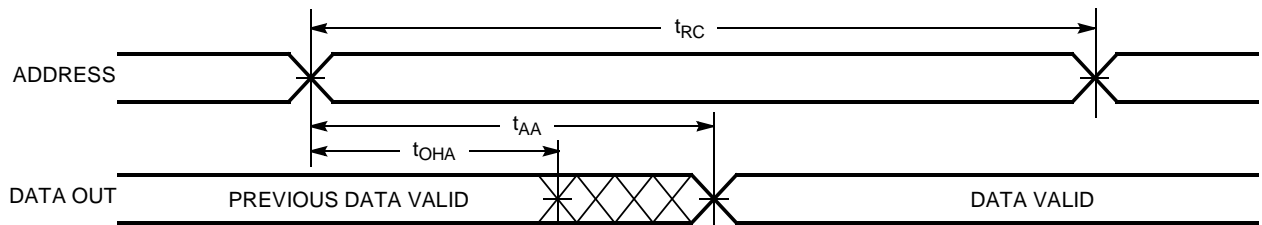
Data Retention Waveform



1049-5

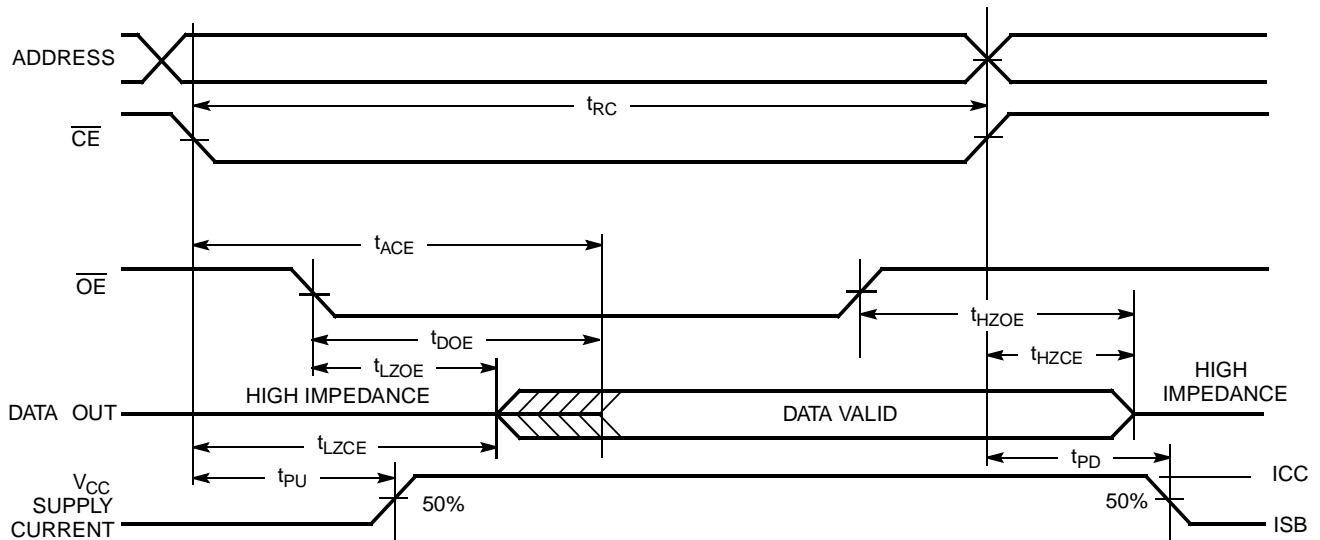
Switching Waveforms

Read Cycle No. 1^[11, 12]



1049-6

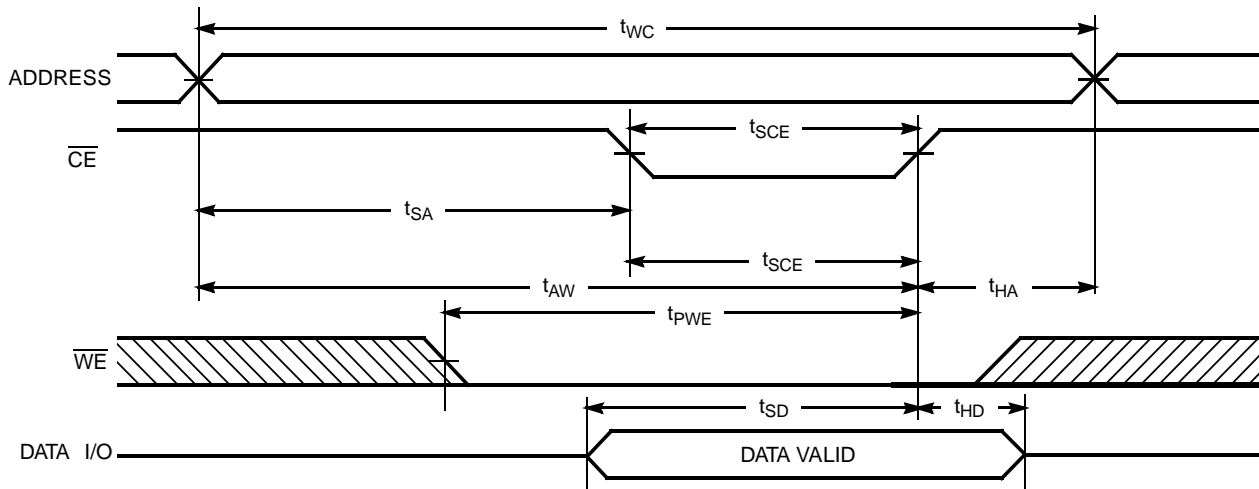
Read Cycle No. 2 (\overline{OE} Controlled)^[12, 13]



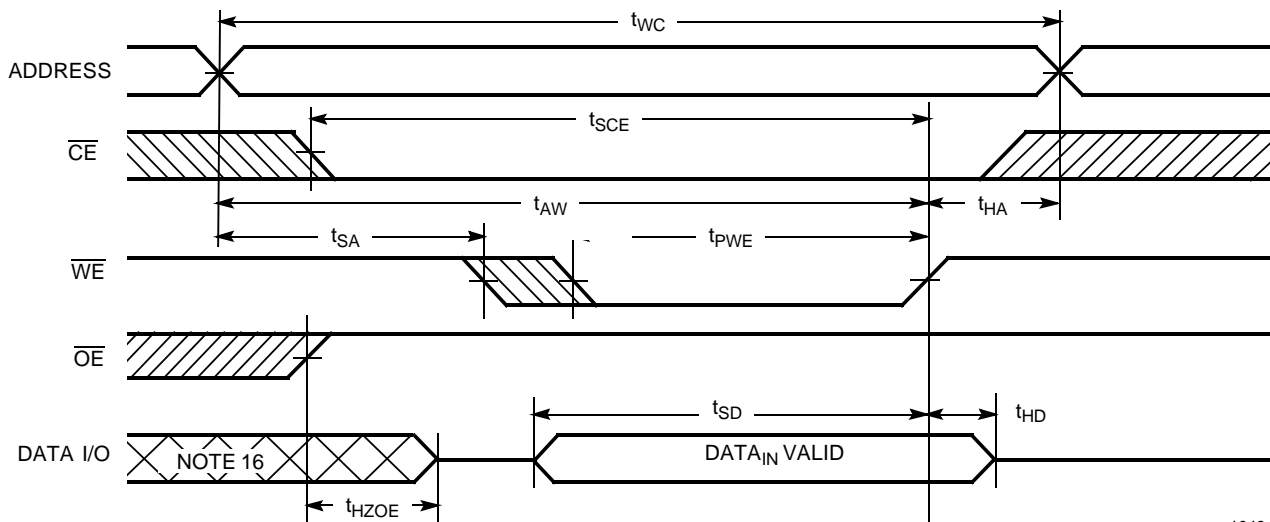
1049-7

Notes:

11. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[14, 15]


1049-8

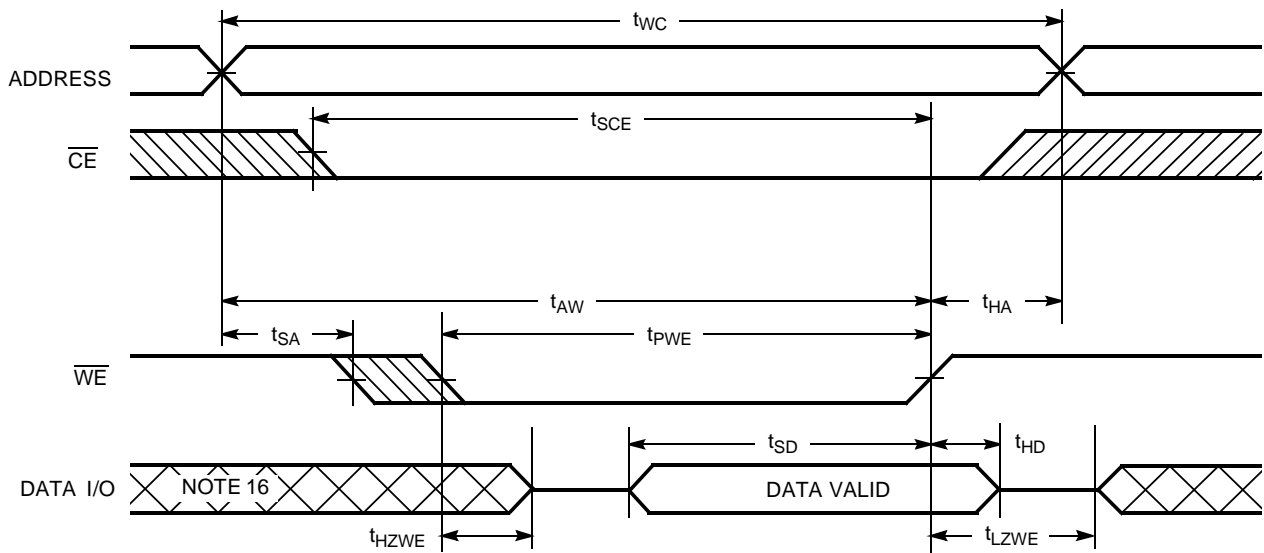
Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[14, 15]


1049-9

Notes:

14. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15]


1049-10

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|----------------|--------------|------------------------------|-----------------|
| 15 | CY7C1049-15VC | V36 | 36-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1049L-15VC | V36 | 36-Lead (400-Mil) Molded SOJ | |
| 17 | CY7C1049-17VC | V36 | 36-Lead (400-Mil) Molded SOJ | |
| | CY7C1049L-17VC | V36 | 36-Lead (400-Mil) Molded SOJ | |
| 20 | CY7C1049-20VC | V36 | 36-Lead (400-Mil) Molded SOJ | Industrial |
| | CY7C1049L-20VC | V36 | 36-Lead (400-Mil) Molded SOJ | |
| | CY7C1049-20VI | V36 | 36-Lead (400-Mil) Molded SOJ | |
| | CY7C1049L-20VI | V36 | 36-Lead (400-Mil) Molded SOJ | |
| | CY7C1049-20VM | V36 | 36-Lead (400-Mil) Molded SOJ | Military |
| | CY7C1049L-20VM | V36 | 36-Lead (400-Mil) Molded SOJ | |
| 25 | CY7C1049-25VC | V36 | 36-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1049L-25VC | V36 | 36-Lead (400-Mil) Molded SOJ | |
| | CY7C1049-25VI | V36 | 36-Lead (400-Mil) Molded SOJ | Industrial |
| | CY7C1049L-25VI | V36 | 36-Lead (400-Mil) Molded SOJ | |
| | CY7C1049-25VM | V36 | 36-Lead (400-Mil) Molded SOJ | Military |
| | CY7C1049L-25VM | V36 | 36-Lead (400-Mil) Molded SOJ | |

Shaded areas contain advance information.

Document #: 38-00563-B

Package Diagram

36-Lead (400-Mil) Molded SOJ V36

