



PRELIMINARY

CY7C1199

32K x 8 Static RAM

Features

- **High speed**
— 15 ns t_{AA}
- **Single 5V power supply with 3.3V-compatible I/Os**
— V_{OH} max. of 3.435V
- **Fast t_{DOE}**

Functional Description

The CY7C1199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. The device operates with a single 5V power supply but internally clamps the output voltage level to a maximum of 3.435V. The internal clamps allow the CY7C1199 to interface to 3.3V processors (such as the Pentium™ processor) without buffers or level translators.

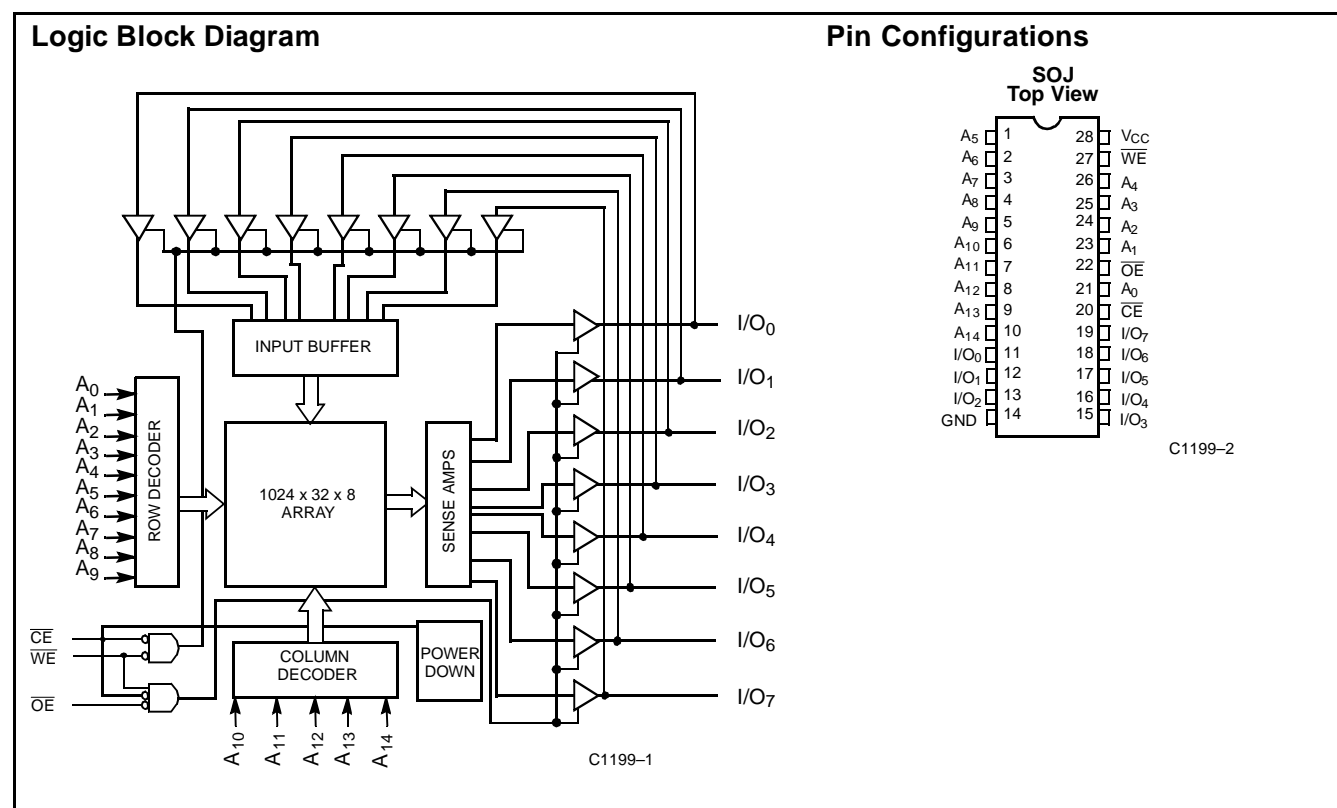
Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and

three-state drivers. This device has an automatic power-down feature, that reduces the power consumption significantly when deselected.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

The CY7C1199 is available in standard 300-mil-wide SOJ packages.



Selection Guide

		7C1199-15	7C1199-20
Maximum Access Time (ns)		15	20
Maximum Operating Current (mA)	Com'l	130	125
Maximum Standby Current (mA)	Com'l	30	30

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14) -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	7C1199-15		7C1199-20		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$-100 \mu A \leq I_{OH} \leq -4.0 \text{ mA}$	2.4	3.435	2.4	3.435	V
V_{OL}	Output LOW Voltage	$I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.}$, $V_{OUT} = GND$		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$	Com'l	130		125	mA
I_{SB1}	Automatic CE Power-Down Current— TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	Com'l	30		30	mA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$	Com'l	10		10	mA

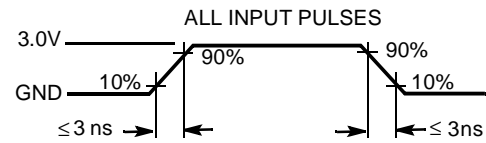
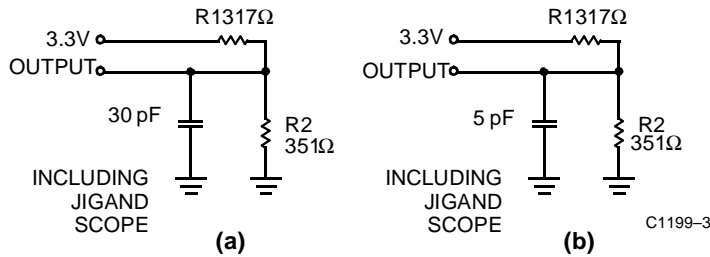
Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

- $V_{IL}(\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[5]



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Equivalent to: THÉVENIN EQUIVALENT

OUTPUT — 167Ω — 1.73V

Switching Characteristics Over the Operating Range^[2, 5]

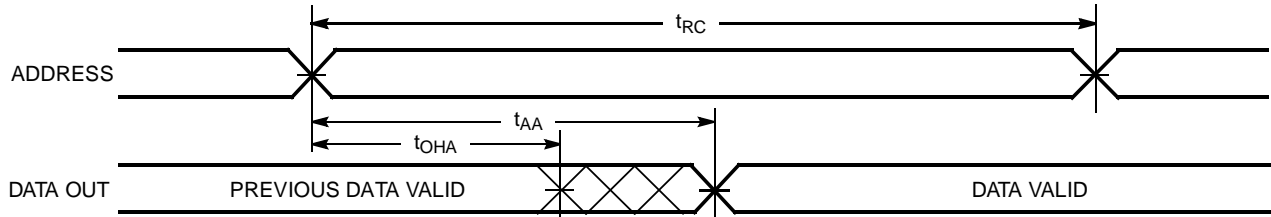
Parameter	Description	7C1199-15		7C1199-20		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	15		20		ns
t _{AA}	Address to Data Valid		15		20	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		15		20	ns
t _{DOE}	\overline{OE} LOW to Data Valid		5		6	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[6]	0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		7		9	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		7		9	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		15		20	ns
WRITE CYCLE ^[8, 9]						
t _{WC}	Write Cycle Time	15		20		ns
t _{SCE}	\overline{CE} LOW to Write End	10		15		ns
t _{AW}	Address Set-Up to Write End	10		15		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	9		15		ns
t _{SD}	Data Set-Up to Write End	8		9		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[7]		7		10	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		ns

Notes:

- Test conditions assume timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

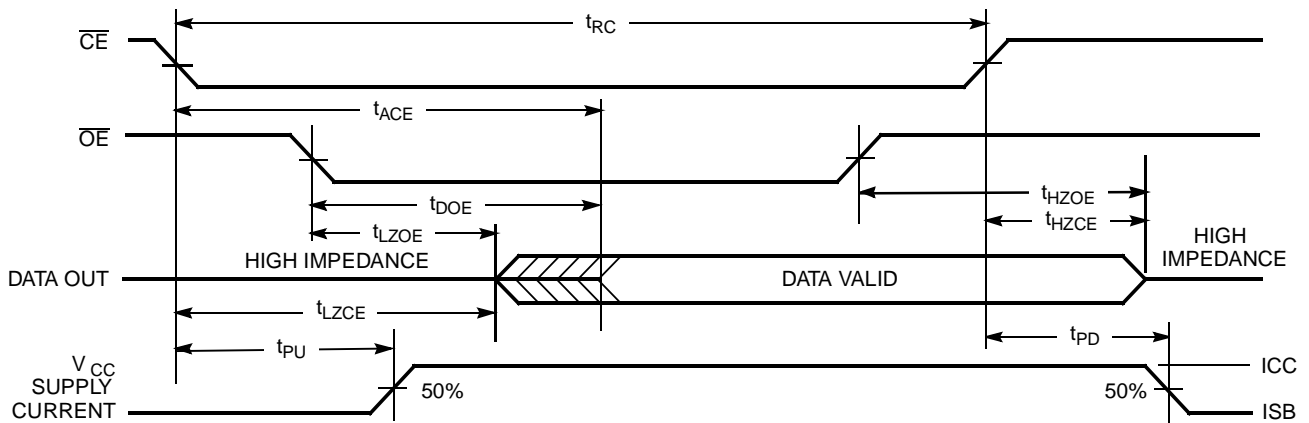
Switching Waveforms

Read Cycle No. 1^[10, 11]



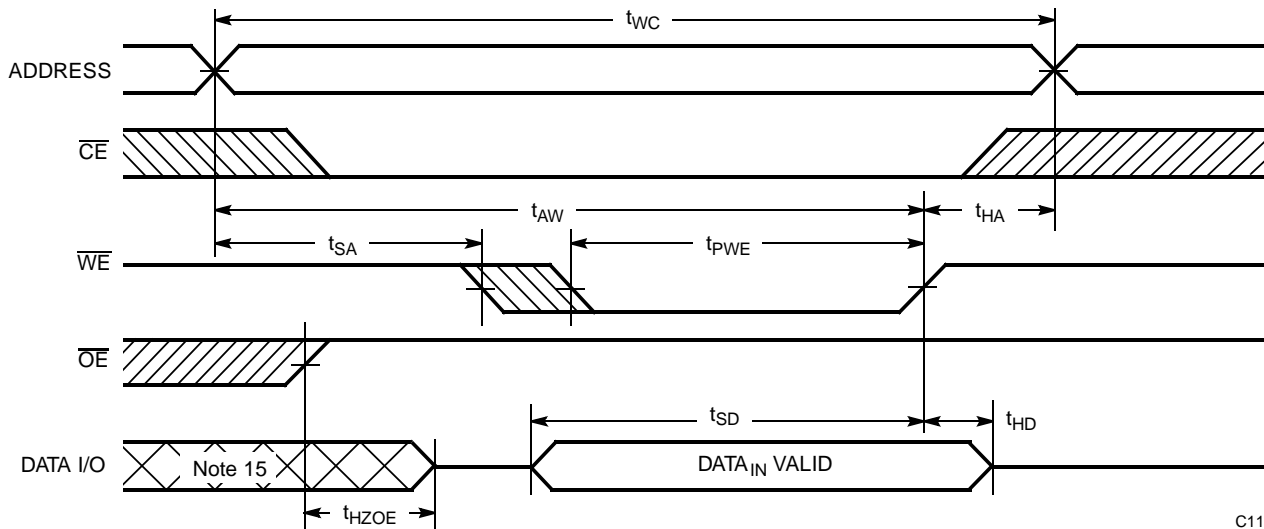
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Read Cycle No. 2^[11, 12]



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Write Cycle No. 1 (\overline{WE} Controlled)^[8, 13, 14]



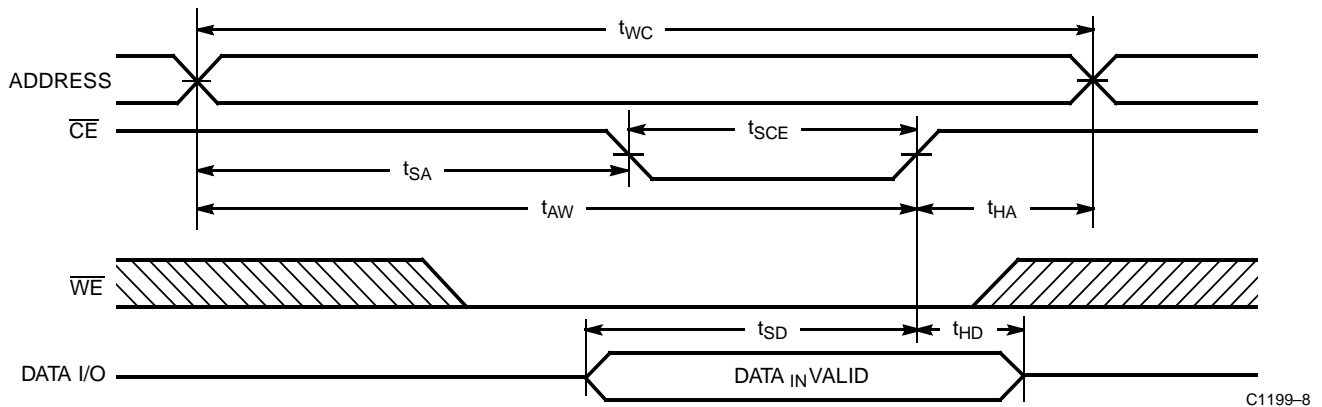
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Switching Waveforms (continued)

Notes:

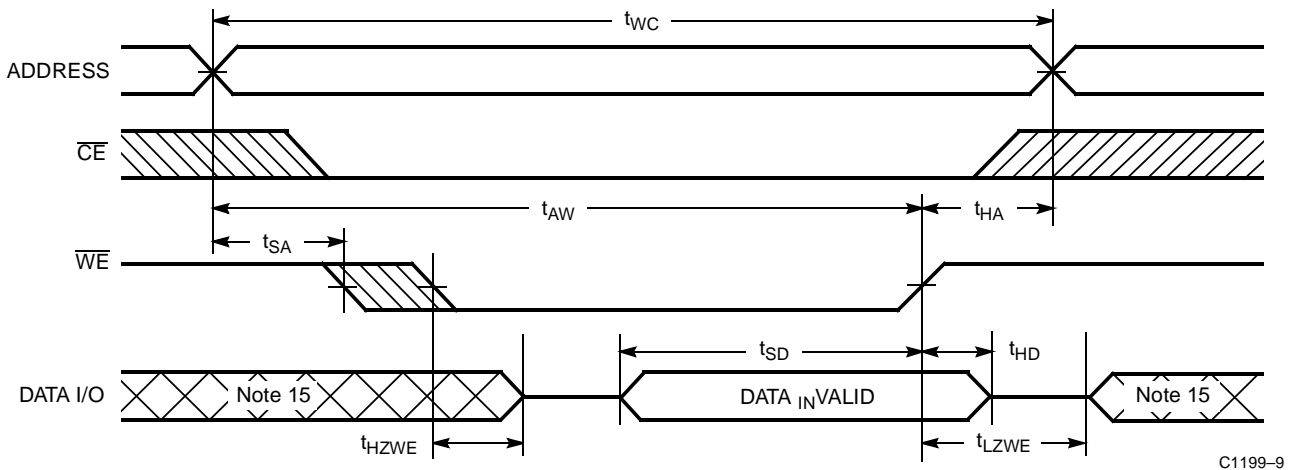
10. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
11. \overline{WE} is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in the output state and input signals should not be applied.

Write Cycle No. 2 (\overline{CE} Controlled)^[8, 13, 14]



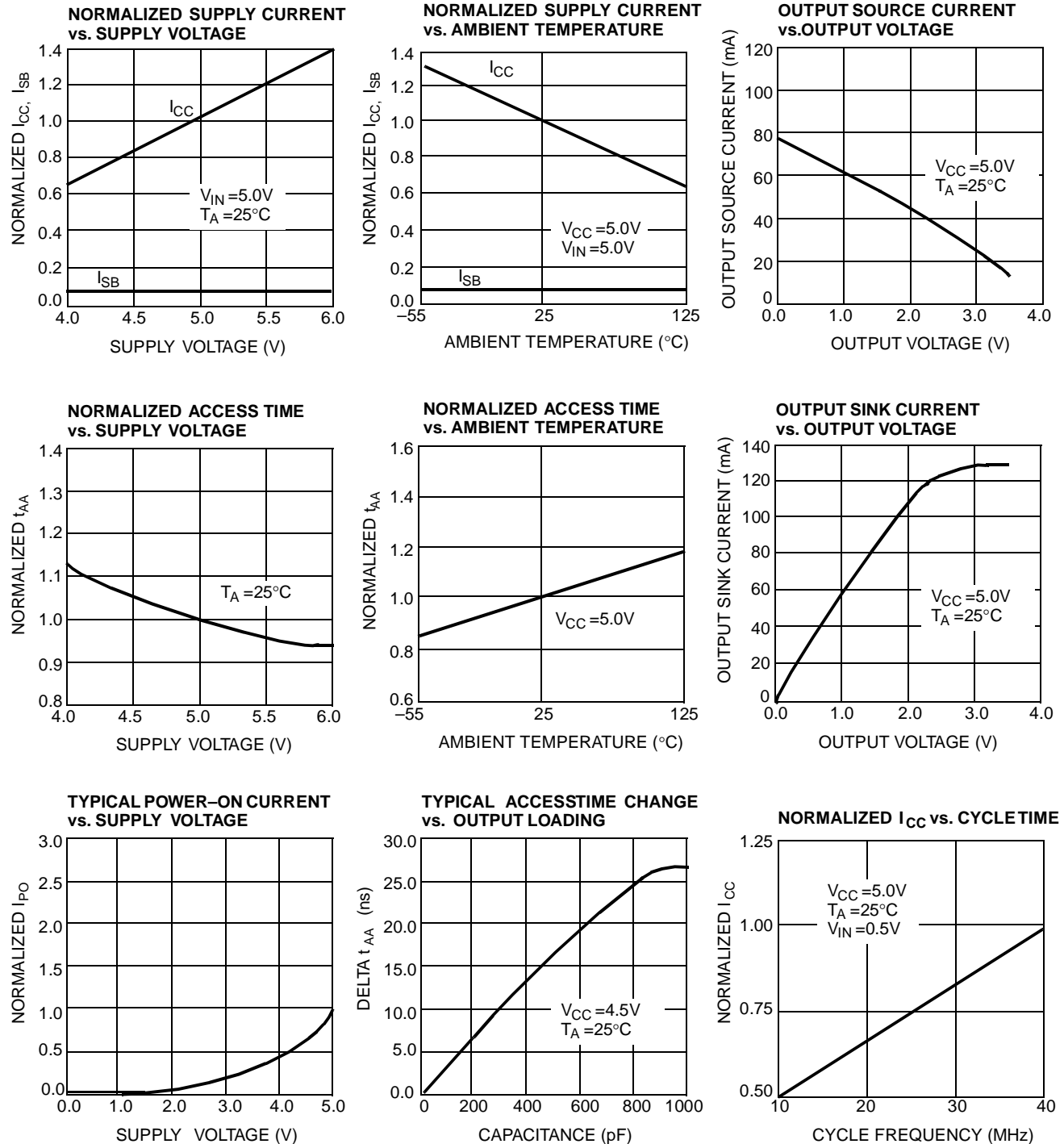
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Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[9, 14]



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Typical DC and AC Characteristics



Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1199-15VC	V21	28-Lead Molded SOJ	Commercial
20	CY7C1199-20VC	V21	28-Lead Molded SOJ	Commercial

Document #: 38-00460

Package Diagram
28-Lead (300-Mil) Molded SOJ V21
