



CYPRESS

PRELIMINARY

CY7C1300A

128K X 36 Dual I/O Dual Address Synchronous SRAM

Features

- Fast clock speed: 133, 100, and 83 MHz
- Fast Access Times: 4.0/5.0/6.0 ns Max.
- Single Clock Operation
- Single 3.3V -5% and +5% power supply V_{CC}
- Separate V_{CCQ} for output buffer
- Two chip enables for simple depth expansion
- Address, Data Input, $\overline{CE1X}$, $\overline{CE2X}$, $\overline{CE1Y}$, $\overline{CE2Y}$, \overline{PTX} , \overline{PTY} , \overline{WEX} , \overline{WEY} , and Data Output Registers On-Chip
- Concurrent Reads and Writes
- Two Bidirectional Data Buses
- Can be configured as separate I/O
- Pass-Through feature
- Asynchronous Output Enables ($\overline{OEX\#}$, $\overline{OEY\#}$)
- LVTTL Compatible I/O
- Self-Timed Write
- Automatic power-down
- 176-Pin TQFP Package

Functional Description

The CY7C1300A SRAM integrates 131,072 x 36 SRAM cells with advanced synchronous peripheral circuitry. It employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1300A allows the user to concurrently perform reads, writes, or pass-through cycles in combination on the two data ports. The two address ports (\overline{AX} , \overline{AY}) determine the read or write locations for their respective data ports (\overline{DQX} , \overline{DQY}).

All input pins except output enable pins (\overline{OEX} , \overline{OEY}) are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion chip enables ($\overline{CE1X}$, $\overline{CE2X}$, $\overline{CE1Y}$ and $\overline{CE2Y}$), pass-through controls (\overline{PTX} and \overline{PTY}), and read-write control (\overline{WEX} and \overline{WEY}).

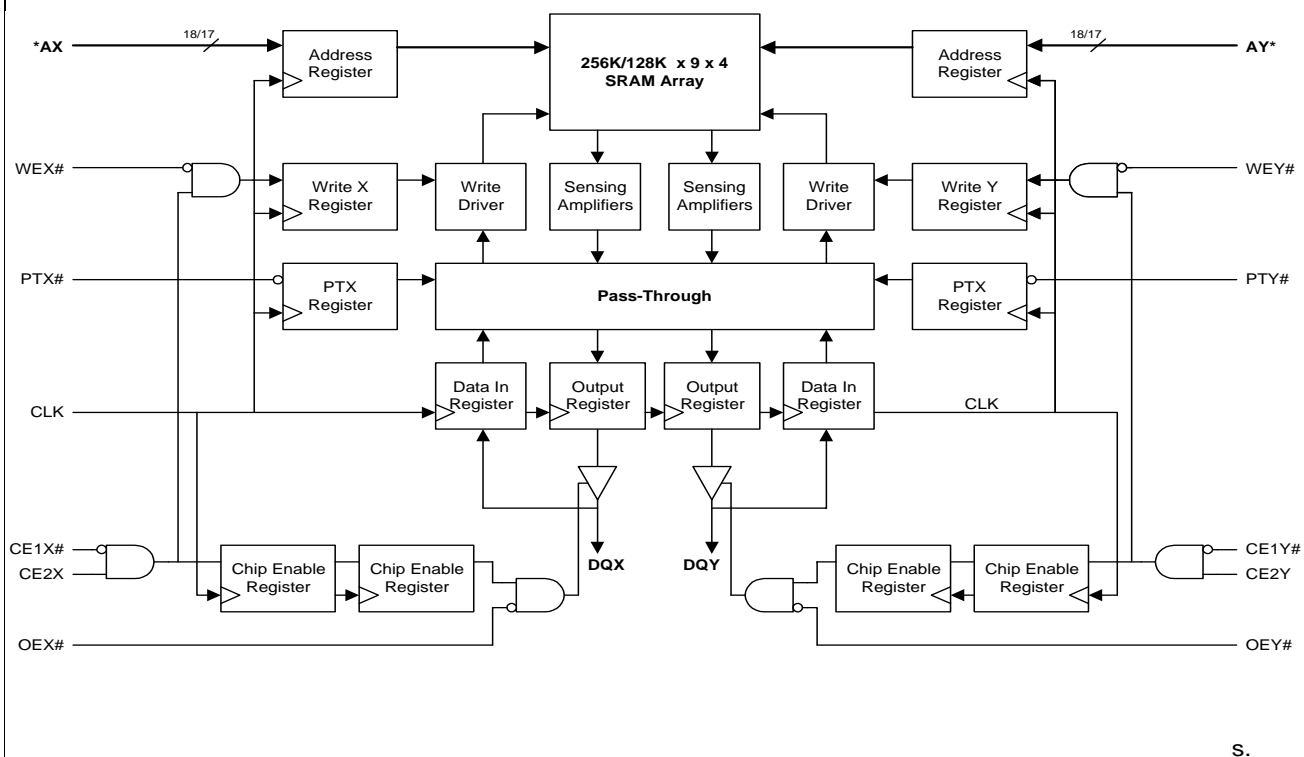
The pass-through feature allows data to be passed from one port to the other, in either direction. The $\overline{PTX\#}$ input must be asserted to pass data from port X to port Y. The $\overline{PTY\#}$ will likewise pass data from port Y to port X. A pass-through operation takes precedence over a read operation.

For the case when \overline{AX} and \overline{AY} are the same, certain protocols are followed. If both ports are read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on \overline{DQY} will be written to the array.

The CY7C1300A operates from a +3.3V power supply. All inputs and outputs are LVTTL compatible. These dual I/O, dual address synchronous SRAMs are well suited for ATM, Ethernet switches, routers, cell/frame buffers, SNA switches and shared memory applications.

The CY7C1300A needs one extra cycle after power for proper power-on reset. The extra cycle is needed after V_{CC} is stable on the device.

This device is available in a 176-pin TQFP package.

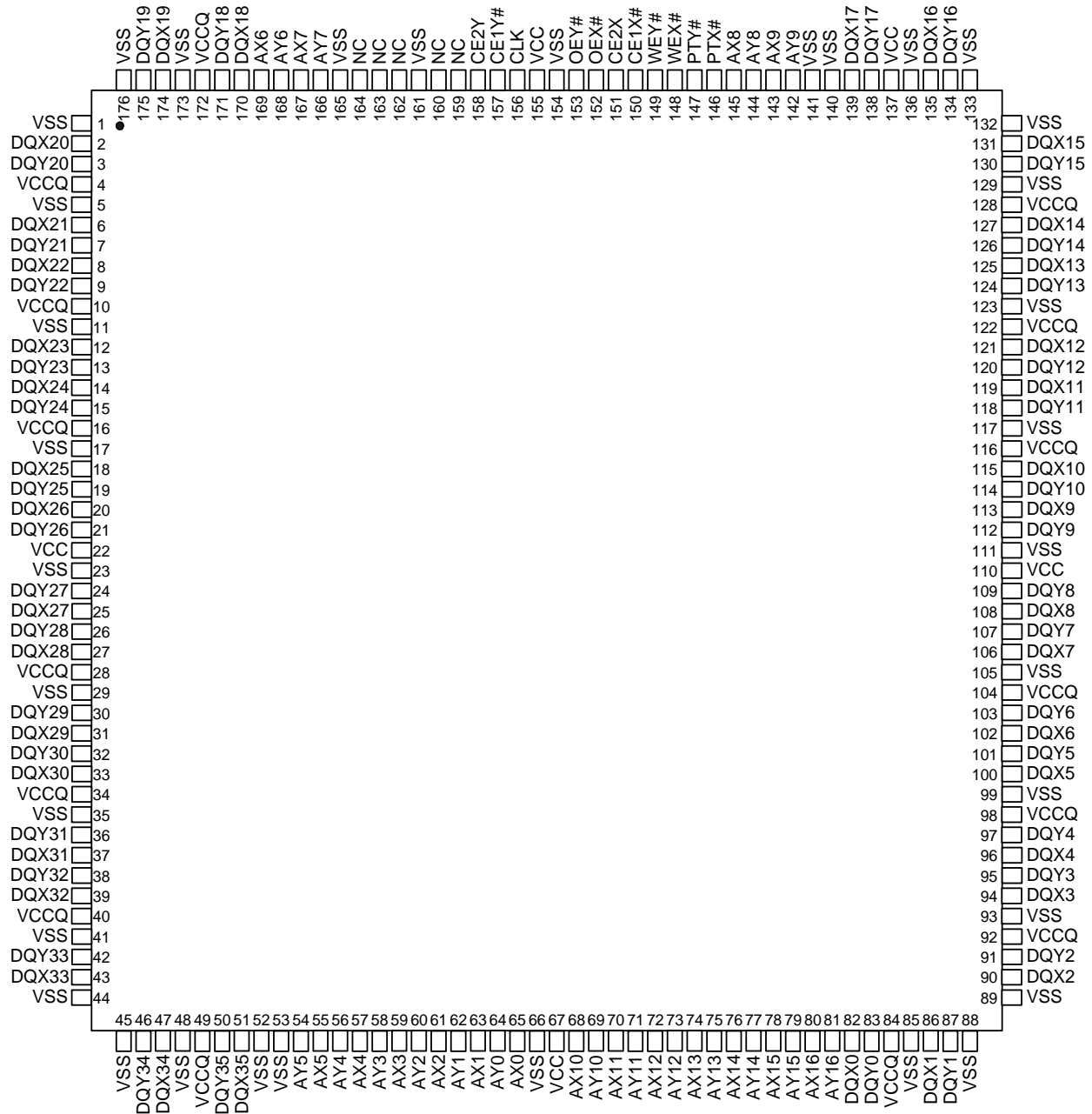
Logic Block Diagram

Selection Guide

	-133	-100	-83
Maximum Access Time (ns)	4.0	5.0	6.0
Maximum Operating Current (mA)	400	350	300
Maximum CMOS Standby Current (mA)	100	100	100

Shaded areas contain advance information.

Note:

- For 128K x 36 devices, AX and AY are 17-bit wide buses.

Pin Configuration
176-Pin TQFP


Pin Definitions (176-pin TQFP)

Name	I/O	Description
AX0–AX16	Input-Synchronous	Synchronous Address Inputs of Port X: Do not allow address pins to float.
AY0–AY16	Input-Synchronous	Synchronous Address Inputs of Port Y: Do not allow address pins to float.
\overline{WEX}	Input-Synchronous	Read Write of Port X: \overline{WEX} signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
\overline{WEY}	Input-Synchronous	Read Write of Port Y: \overline{WEY} signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
\overline{PTX}	Input-Synchronous	Pass-Through of Port X: \overline{PTX} signal is a synchronous input that enables passing Port X input to Port Y output.
\overline{PTY}	Input-Synchronous	Pass-Through of Port Y: \overline{PTY} signal is a synchronous input that enables passing Port Y input to Port X output.
\overline{OEX}	Input	Asynchronous Output Enable of Port X: \overline{OEX} must be LOW to read data. When \overline{OEX} is HIGH, the DQXx pins are in high-impedance state.
\overline{OEY}	Input	Asynchronous Output Enable of Port Y: \overline{OEY} must be LOW to read data. When \overline{OEY} is HIGH, the DQYx pins are in high-impedance state.
DQX0–DQX35	Input/Output	Data Inputs/Outputs of Port X: Both the data input path and data output path are registered and triggered by the rising edge of CLK.
DQY0 – DQY35	Input/Output	Data Inputs/Outputs of Port Y: Both the data input path and data output path are registered and triggered by the rising edge of CLK.
CLK	Input-Synchronous	Clock: This is the clock input to this device. Except for \overline{OEX} and \overline{OEY} , all timing references of the address, data in, and all control signals for the device are made with respect to the rising edge of CLK.
$\overline{CE1X}$	Input-Synchronous	Synchronous Active LOW Chip Enable Port X: $\overline{CE1X}$ is used with CE2X to enable Port X of this device. CE1X sampled HIGH at the rising edge of clock initiates a deselect cycle for Port X.
CE2X	input-Synchronous	Synchronous Active HIGH Chip Enable Port X: CE2X is used with $\overline{CE1X}$ to enable Port X of this device. CE2X sampled LOW at the rising edge of clock initiates a deselect cycle for Port X.
$\overline{CE1Y}$	Input-Synchronous	Synchronous Active LOW Chip Enable Port Y: $\overline{CE1Y}$ is used with CE2Y to enable Port Y of this device. CE1Y sampled HIGH at the rising edge of clock initiates a deselect cycle for Port Y.
CE2Y	input-Synchronous	Synchronous Active HIGH Chip Enable Port Y: CE2Y is used with $\overline{CE1Y}$ to enable Port Y of this device. CE2Y sampled LOW at the rising edge of clock initiates a deselect cycle for Port Y.
VCC	Supply	Power Supply: +3.3V –5% and +5%.
VSS	Ground	Ground: GND.
VSS	Ground	Ground: GND. No chip current flows through these pins. However, user needs to connect GND to these pins.
VCCQ	I/O Supply	Output Buffer Supply: +3.3V -5% and +5%.
NC	-	No Connect: These signals are not internally connected. User can connect them to V_{CC} , V_{SS} , or any signal lines or simply leave them floating.

Cycle Description Truth Table^[2, 3, 4, 5, 6, 7, 8, 9]

Operation	CE1X#	CE2X	CE1Y#	CE2Y	WEX#	WEY#	PTX#	PTY#
DESELECT CYCLE	H	X	H	X	X	X	X	X
DESELECT CYCLE	X	L	X	L	X	X	X	X
WRITE PORT X	L	H	X	X	0	X	X	X
WRITE PORT Y	X	X	L	H	X	0	X	X
PASS-THROUGH from X to Y	L	H	L	H	X	X	0	X
PASS-THROUGH from Y to X	L	H	L	H	X	X	X	0
READ PORT X	L	H	X	X	1	X	1	1
READ PORT Y	X	X	L	H	X	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C

Ambient Temperature with

Power Applied..... -10°C to +85°C

Supply Voltage on V_{DD} Relative to GND..... -0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State^[10]..... -0.5V to V_{CCQ} + 0.5V

DC Input Voltage^[10]..... -0.5V to V_{CCQ} + 0.5V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA.

Operating Range

Range	Ambient Temperature ^[11]	V _{DD} /V _{DDQ}
Com'l	0°C to +70°C	3.3V ± 5%

Notes:

- X means "Don't Care." H means logic HIGH. L means logic LOW.
- All inputs except OEX and OEY must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
- OEX and OEY must be asserted to avoid bus contention during Write and Pass-Through cycles. For a Write and Pass-Through operation following a Read operation, OEX/OEY must be HIGH before the input data required setup time plus High-Z time for OEX/OEY and staying HIGH throughout the input data hold time.
- Operation number 3 – 6 can be used in any combination.
- Operation number 4 and 7, 3 and 8, 7 and 8 can be combined.
- Operation number 5 can not be combined with operation number 7 or 8 because Pass-Through operation has higher priority over a READ operation.
- Operation number 6 can not be combined with operation number 7 or 8 because Pass-Through operation has higher priority over a READ operation.
- This device contains circuitry that will ensure the outputs will be in High-Z during power-up
- Minimum voltage equals -2.0V for pulse duration less than 20 ns.
- T_A is the case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.465	V
V_{DDQ}	I/O Supply Voltage			3.135	3.465	V
V_{OH}	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$		2.4		V
V_{OL}	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage ^[12]			2.0	$V_{CC} + 0.5V$	V
V_{IL}	Input LOW Voltage ^[13]			-0.5	0.8	V
I_X	Input Load Current	$GND \leq V_{IN} \leq V_{DDQ}$		-5	5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{IN} \leq V_{DDQ}$, Output Disabled		-5	5	μA
I_{CC}	V_{DD} Operating Supply	$V_{DD} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{CYC}$	7.0-ns cycle, 133 MHz		400	mA
			7.5-ns cycle, 100 MHz		350	mA
			10.0-ns cycle, 83MHz		300	mA
I_{SB}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD} , Device Deselected ^[14] , $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$, $f = 0$		All speed grades		100 mA

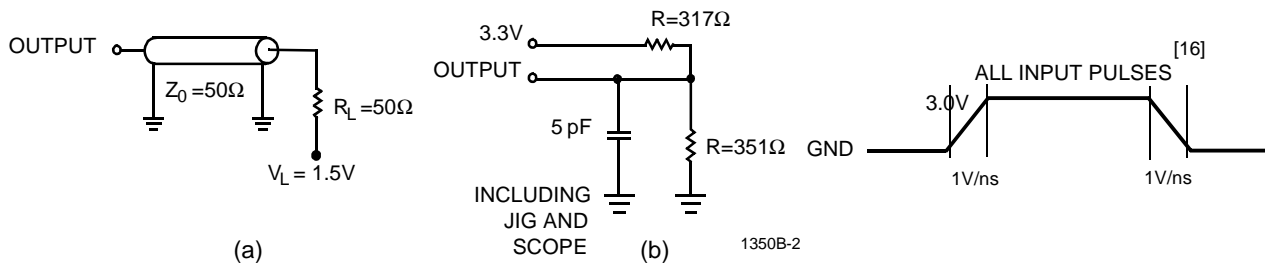
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Note:

12. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq t_{KC}/2$
13. Undershoot: $V_{IL} \leq -2.0V$ for $t \leq t_{KC}/2$.
14. "Device Deselected" means the device is in Power -Down mode as defined in the truth table.

Capacitance^[15]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{V}$, $V_{CCQ} = 3.3\text{V}$	6	pF
C_{CLK}	Clock Input Capacitance		6	pF
$C_{I/O}$	Input/Output Capacitance		8	pF

AC Test Loads and Waveforms^[16]

Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Units	Notes
Thermal Resistance (Junction to Ambient)	(@200lfm) Single-layer printed circuit board	Θ_{JA}	40	$^\circ\text{C/W}$	15
Thermal Resistance (Junction to Ambient)	(@200lfm) Four-layer printed circuit board	Θ_{JC}	35	$^\circ\text{C/W}$	15
Thermal Resistance (Junction to Board)	Bottom	Θ_{JA}	23	$^\circ\text{C/W}$	15
Thermal Resistance (Junction to Case)	Top	Θ_{JC}	9	$^\circ\text{C/W}$	15

Notes:

15. Tested initially and after any design or process change that may affect these parameters.
 16. AC test conditions assume signal transition time of 1 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading shown in part (a) of AC Test Loads.

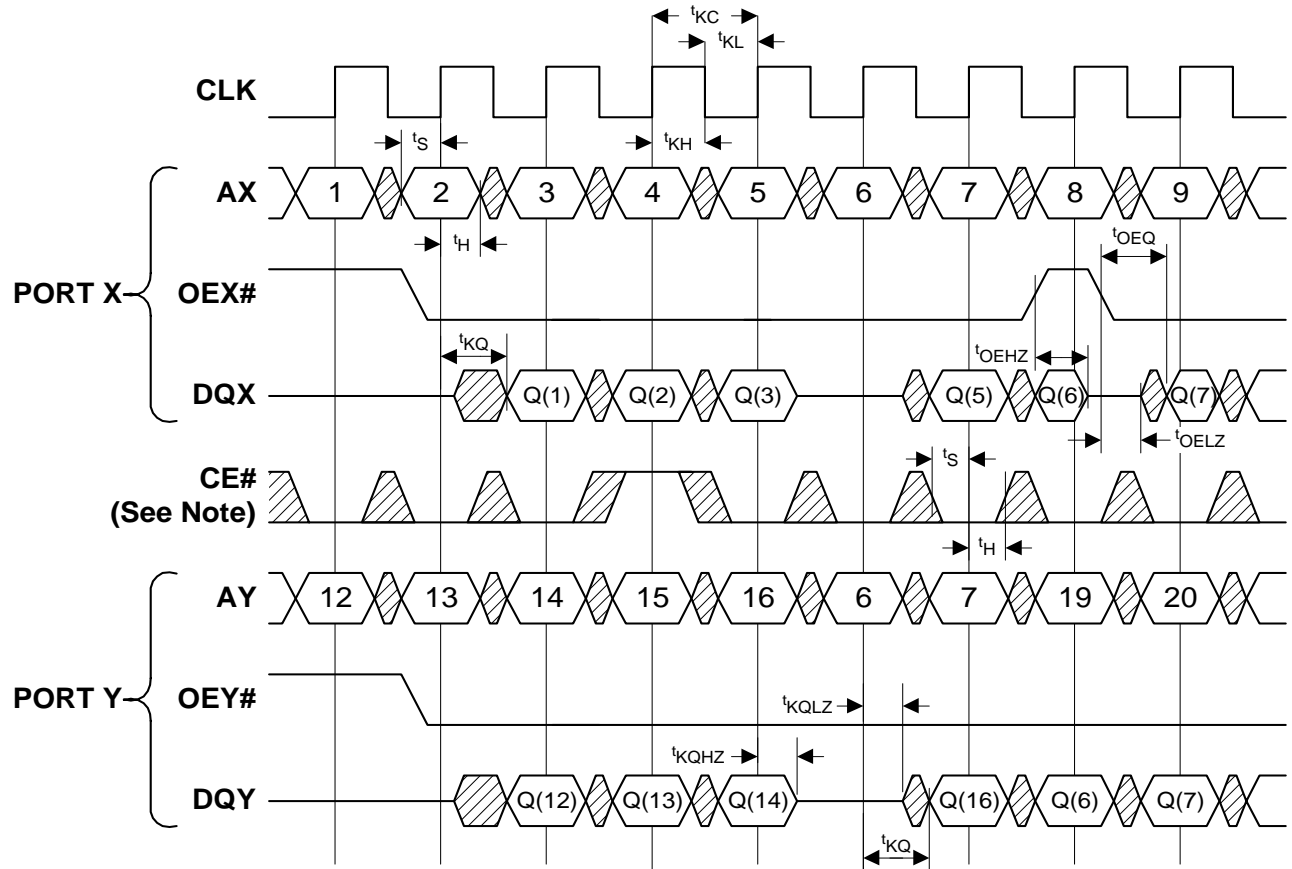
Switching Characteristics Over the Operating Range^[16, 17, 18]

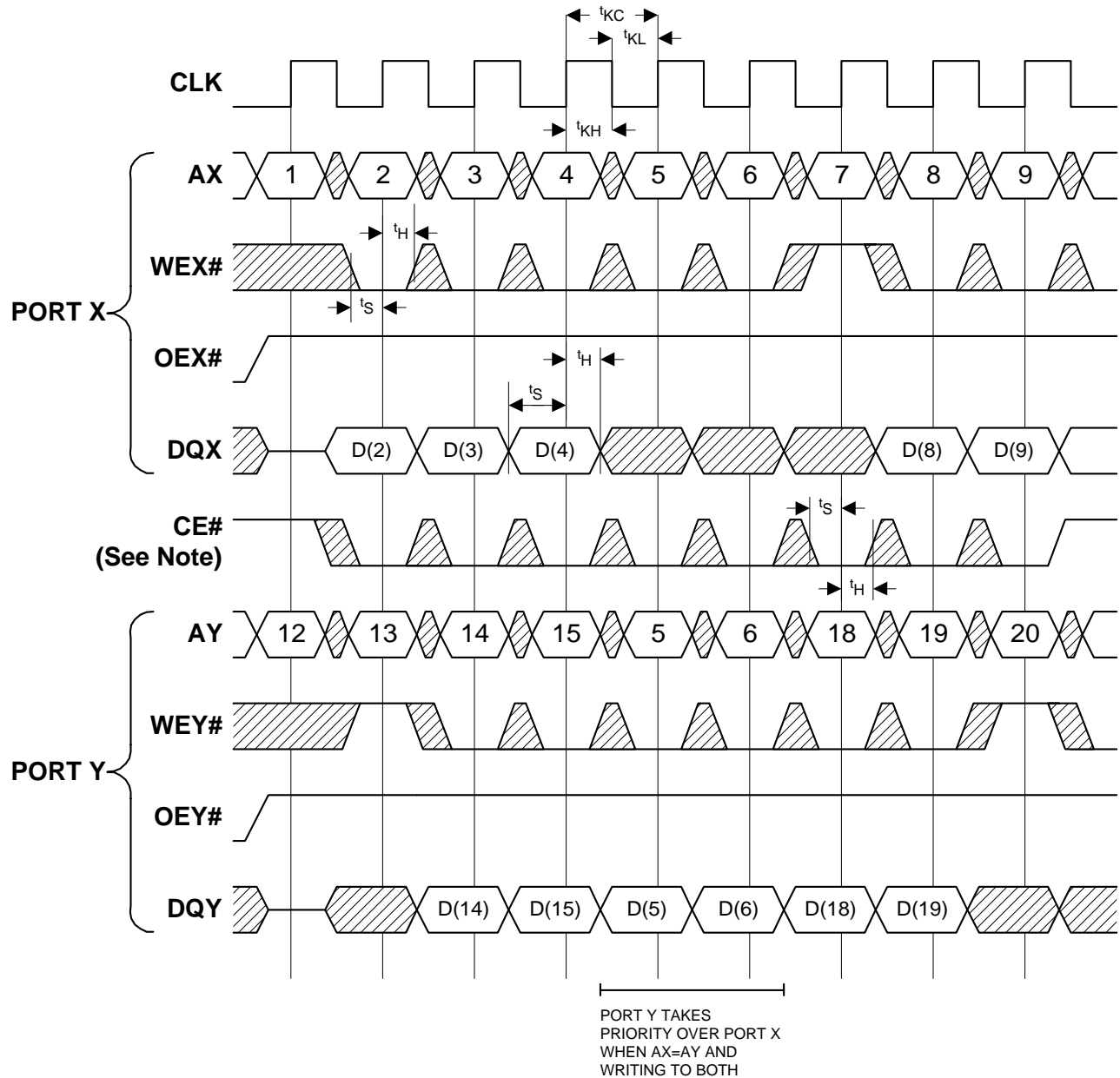
Parameter	Description	-133		-100		-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock								
t _{KC}	Clock cycle time	7.5		10		12		ns
t _{KH}	Clock HIGH time	3.0		3.5		4.0		ns
t _{KL}	Clock LOW time	3.0		3.5		4.0		ns
Output times								
t _{KQ}	Clock to output valid		4.0		5.0		6.0	ns
t _{KQX}	Clock to output invalid	1.5		1.5		1.5		ns
t _{KQLZ}	Clock to output in Low-Z ^[19]	0		0		0		ns
t _{KQHZ}	Clock to output in High-Z ^[19]		3.0		3.0		3.0	ns
t _{OEQ}	$\overline{OEX}/\overline{OEY}$ to output valid		4.0		5.0		6.0	ns
t _{OELZ}	$\overline{OEX}/\overline{OEY}$ to output in Low-Z ^[19]	0		0		0		ns
t _{OEHZ}	$\overline{OEX}/\overline{OEY}$ to output in High-Z ^[19]		3.0		3.0		3.0	ns
Setup times								
t _S	Addresses, Controls and Data In	1.5		1.5		2.0		ns
Hold times								
t _H	Addresses, Controls and Data In	0.5		0.5		0.5		ns

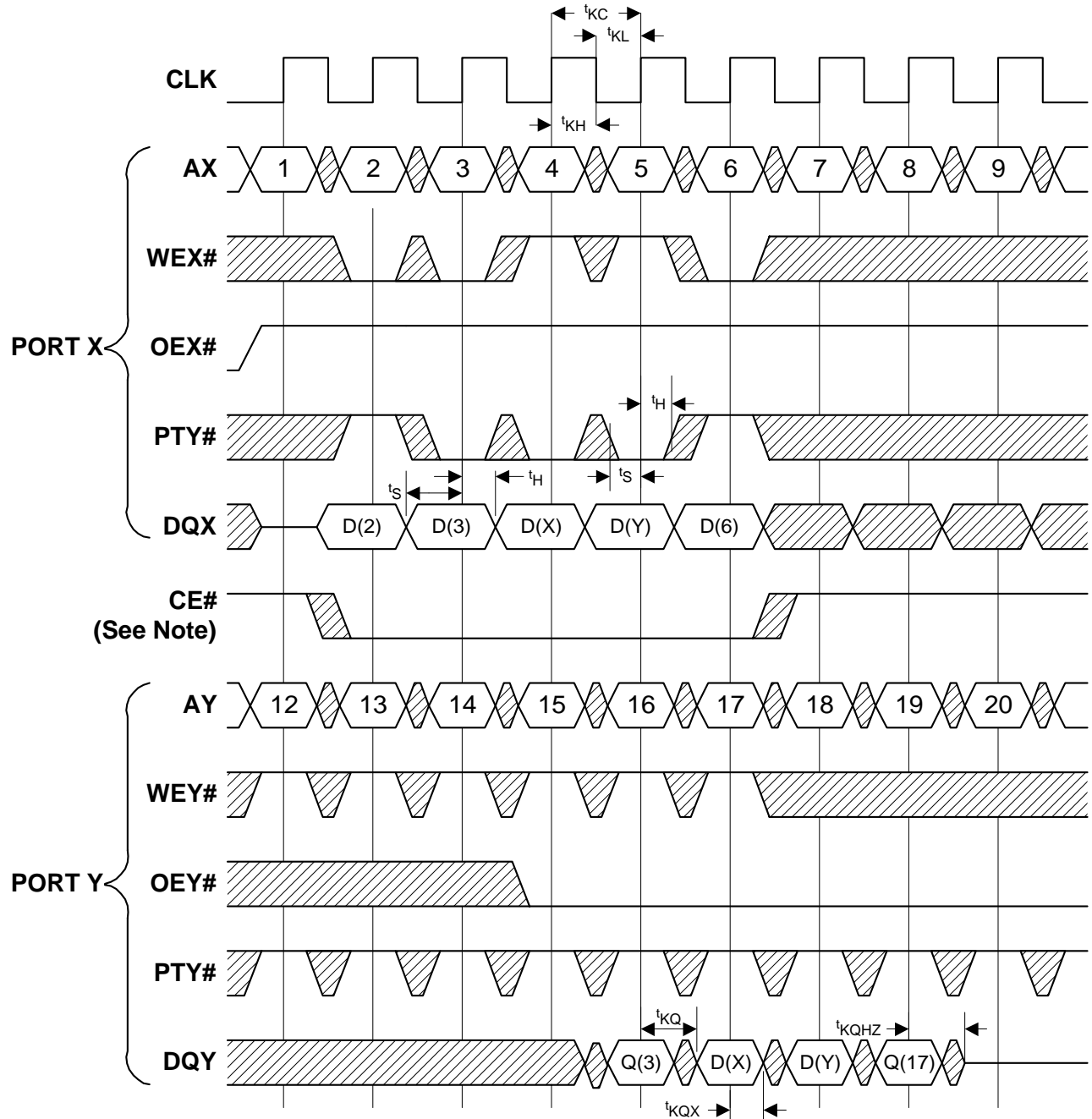
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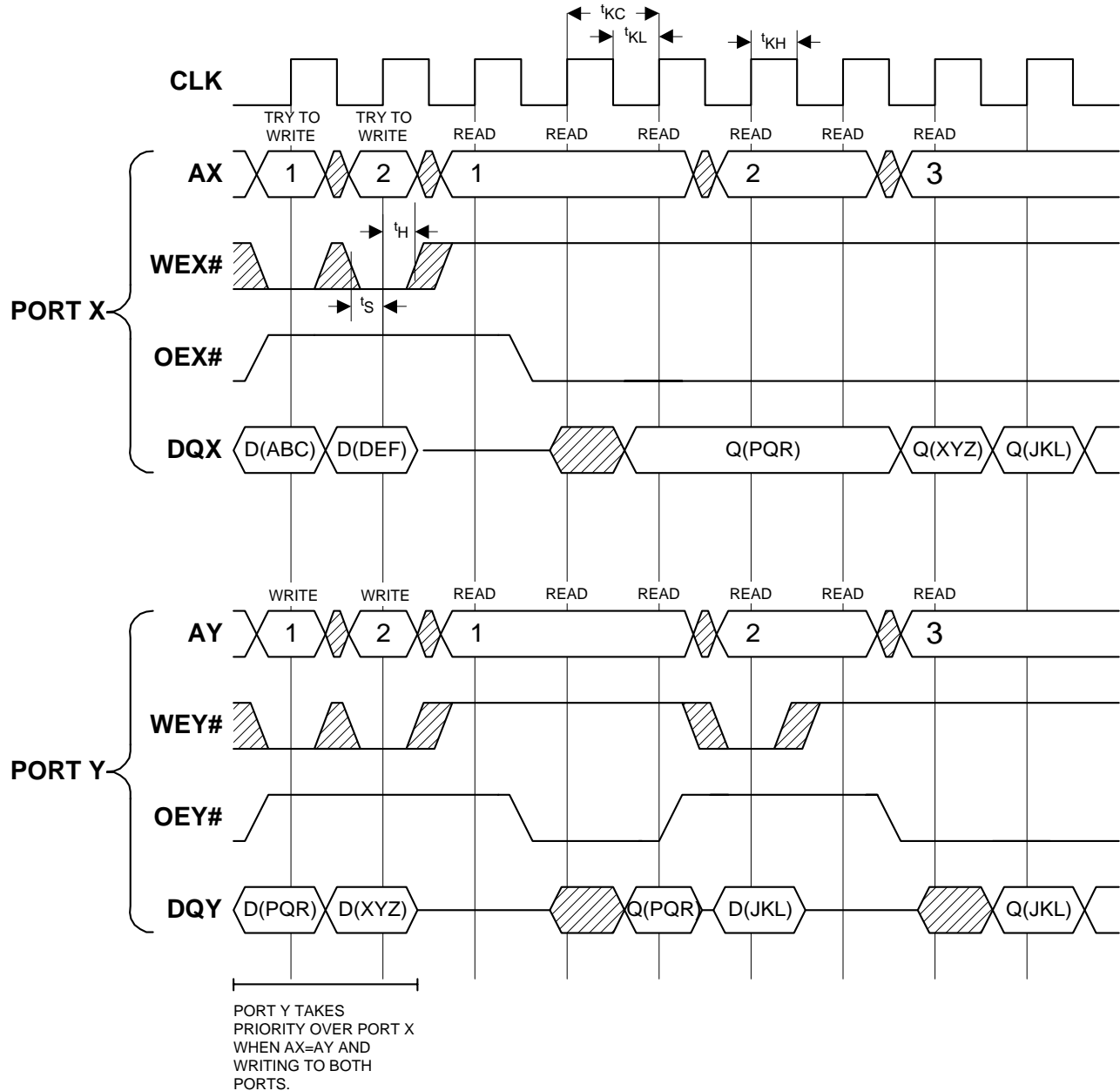
Notes:

17. t_{CHZ} , t_{CLZ} , t_{OEZ} , t_{EOLZ} , and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
19. This parameter is sampled and not 100% tested.
20. CE LOW means (CE1X and CE1Y) equals LOW and (CE2X and CE2Y) equals HIGH. \overline{CE} HIGH means ($\overline{CE1X}$ and $\overline{CE1Y}$) equals HIGH or (CE2X and CE2Y) equals LOW.

Switching Waveforms ^[20]
READ CYCLE TIMING FROM BOTH PORTS (WEX, WEY, PTX, PTY HIGH)^[19]


Switching Waveforms (continued)^[20]
WRITE CYCLE TIMING TO BOTH PORTS (\overline{PTX} , \overline{PTY} HIGH)^[19]


Switching Waveforms (continued)^[20]
WRITE TO PORT X AND PASS-THROUGH TO PORT Y^[19]


Switching Waveforms (continued)^[20]
COMBINATION READ/WRITE WITH SAME ADDRESS ON EACH PORT


PTX# = PTY# = HIGH
D(Value) = Value is the input of the data port.
Q(Value) = Value is the output of the data port.

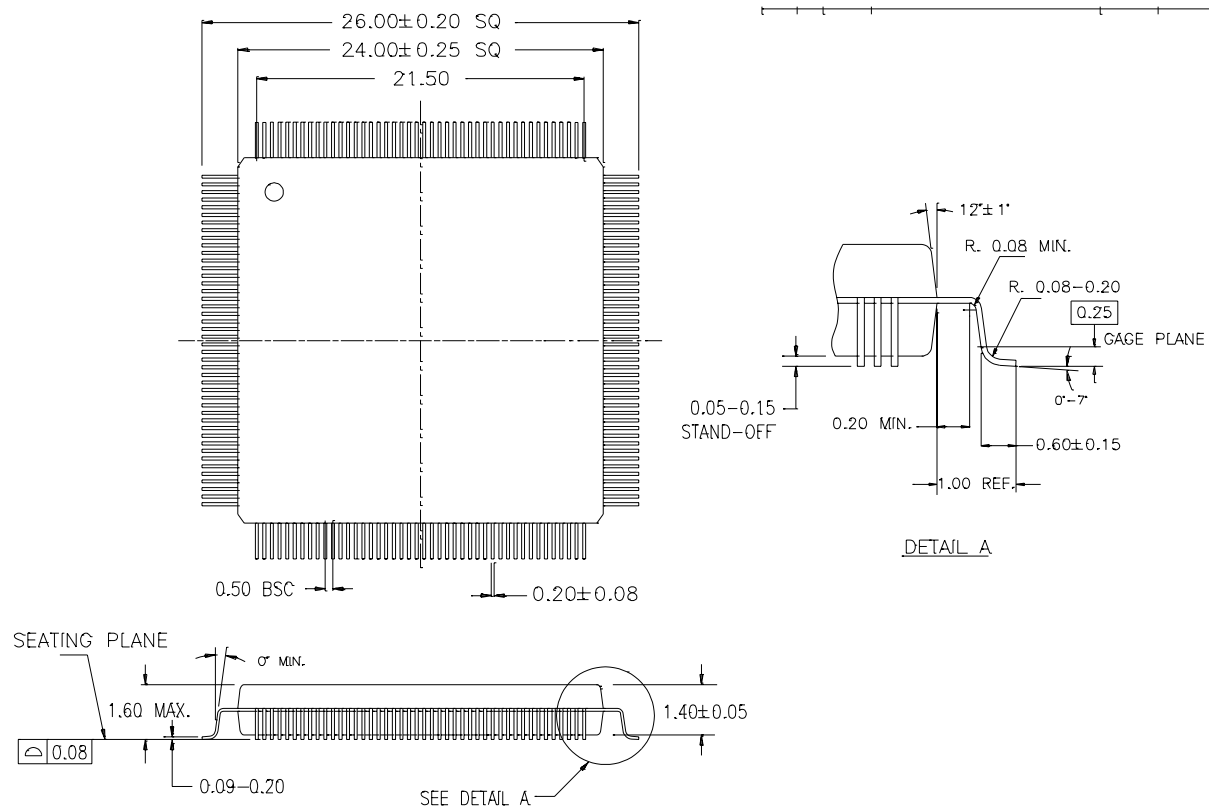


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C1300A-133AC	ACx	176 Pin TQFP	Commercial
100	CY7C1300A-100AC			
83	CY7C1300A-83BGC			
Shaded areas contain advance information				

Package Diagram

176-Lead Thin Quad Flat Pack (24x24x1.4 mm) A176





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Document Title: CY7C1300A - 128K x 36 Dual I/O Dual Address Synchronous SRAM
Document Number: 38-05075

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107304	06/08/01	NSL	New Data Sheet