



# CYPRESS

## CY7C185A

### 8K x 8 Static RAM

#### Features

- **High speed**  
— 20 ns
- **CMOS for optimum speed/power**
- **Low active power**  
— 743 mW
- **Low standby Power**  
— 220 mW
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**

#### Functional Description

The CY7C185A is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active LOW Output Enable ( $\overline{OE}$ ), and

three-state drivers. The device has an automatic power-down feature ( $\overline{CE}_1$ ), reducing the power consumption by over 70% when deselected. The CY7C185A is in the standard 300-mil-wide DIP package and leadless chip carrier.

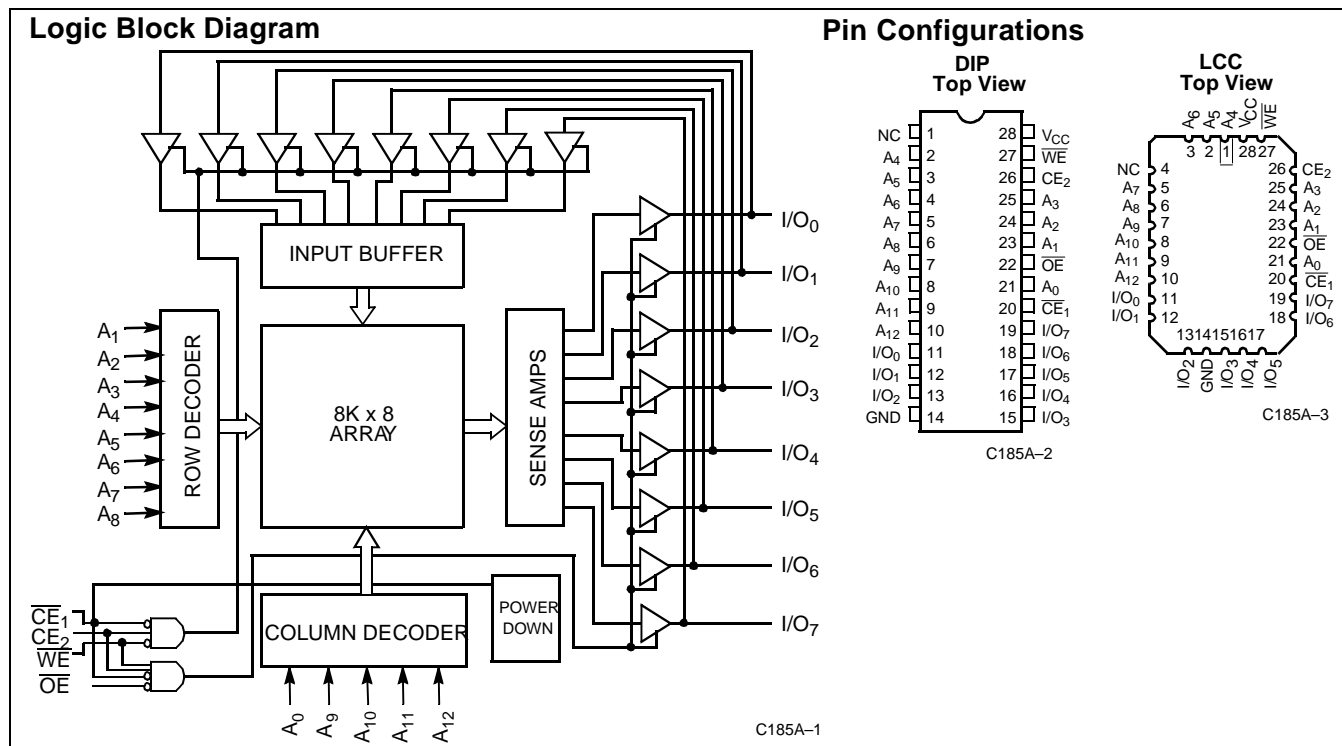
Writing to the device is accomplished when the Chip Enable one ( $\overline{CE}_1$ ) and Write Enable ( $WE$ ) inputs are both LOW, and the Chip Enable two ( $CE_2$ ) input is HIGH.

Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{12}$ ).

Reading the device is accomplished by taking Chip Enable one ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW, while taking Write Enable ( $WE$ ) and Chip Enable two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in a high-impedance state when Chip Enable one ( $\overline{CE}_1$ ) or Output Enable ( $\overline{OE}$ ) is HIGH, or Write Enable ( $WE$ ) or Chip Enable two ( $CE_2$ ) is LOW.

A die coat is used to ensure alpha immunity.



#### Selection Guide<sup>[1]</sup>

		7C185A-20	7C185A-25	7C185A-35	7C185A-45
Maximum Access Time (ns)		20	25	35	45
Maximum Operating Current (mA)	Military	135	125	125	125
Maximum Standby Current (mA)	Military	40/20	40/20	30/20	30/20

#### Note:

1. For commercial specifications, see the CY7C185 data sheet.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	–65°C to +150°C
Ambient Temperature with Power Applied .....	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14) .....	–0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State <sup>[2]</sup> .....	–0.5V to +7.0V

DC Input Voltage <sup>[2]</sup> .....	–0.5V to +7.0V
Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current .....	>200 mA

## Operating Range

Range	Ambient Temperature <sup>[3]</sup>	V <sub>CC</sub>
Military <sup>[4]</sup>	–55°C to +125°C	5V ± 10%

## Electrical Characteristics Over the Operating Range<sup>[4]</sup>

Parameter	Description	Test Conditions	7C185A–20		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = –4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		–0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	–10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	–10	+10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[5]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		–300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		135	mA
I <sub>SB1</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , Min. Duty Cycle = 100%		40	mA
I <sub>SB2</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.3V or V <sub>IN</sub> ≥ 0.3V		20	mA

## Electrical Characteristics Over the Operating Range<sup>[4]</sup> (continued)

Parameter	Description	Test Conditions	7C185A–25		7C185A–35, 45		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = –4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		–0.5	0.8	–0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	–10	+10	–10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	–10	+10	–10	+10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[5]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		–300		–300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		125		125	mA
I <sub>SB1</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , Min. Duty Cycle = 100%		40		30	mA
I <sub>SB2</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.3V or V <sub>IN</sub> ≥ 0.3V		20		20	mA

### Notes:

- V<sub>IL</sub> (min.) = –3.0V for pulse durations less than 30 ns.
- T<sub>A</sub> is the case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

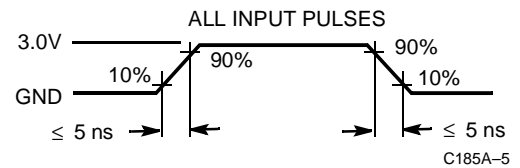
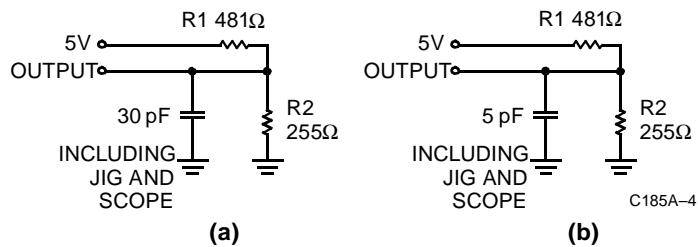
## Capacitance<sup>[6]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	10	pF
$C_{OUT}$	Output Capacitance		10	pF

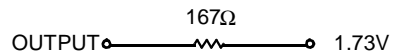
**Note:**

6. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



**Switching Characteristics** Over the Operating Range<sup>[7]</sup>

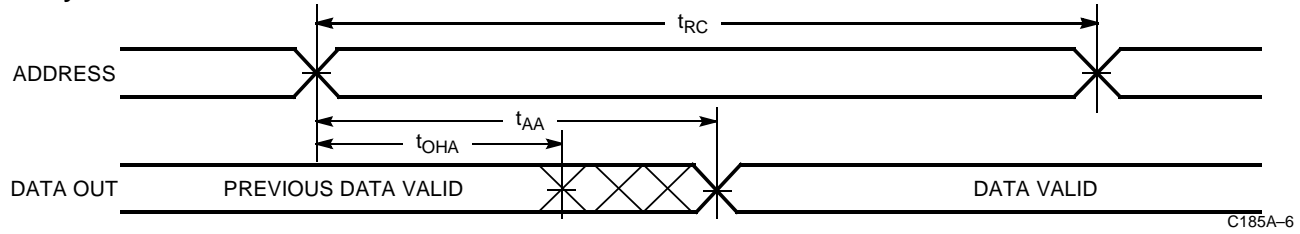
Parameter	Description	7C185A-20		7C185A-25		7C185A-35		7C185A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t <sub>RC</sub>	Read Cycle Time	20		25		35		45		ns
t <sub>AA</sub>	Address to Data Valid		20		25		35		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE1</sub>	$\overline{CE}_1$ LOW to Data Valid		20		25		35		45	ns
t <sub>ACE2</sub>	CE <sub>2</sub> HIGH to Data Valid		20		25		35		30	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		10		12		15		20	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[8]</sup>		8		10		12		15	ns
t <sub>LZCE1</sub>	$\overline{CE}_1$ LOW to Low Z <sup>[9]</sup>	5		5		5		5		ns
t <sub>LZCE2</sub>	CE <sub>2</sub> HIGH to Low Z	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH to High Z <sup>[8, 9]</sup> CE <sub>2</sub> LOW to High Z		8		10		15		15	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH to Power-Down		20		20		20		25	ns
WRITE CYCLE <sup>[10]</sup>										
t <sub>WC</sub>	Write Cycle Time	20		20		25		40		ns
t <sub>SCE1</sub>	$\overline{CE}_1$ LOW to Write End	15		20		25		30		ns
t <sub>SCE2</sub>	CE <sub>2</sub> HIGH to Write End	15		20		25		30		ns
t <sub>AW</sub>	Address Set-Up to Write End	15		20		25		30		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	15		15		20		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		10		15		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z	3		5		5		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[8]</sup>		7		7		10		15	ns

**Notes:**

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
8. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
10. Device is continuously selected.  $\overline{OE}$ , CE = V<sub>IL</sub>. CE<sub>2</sub> = V<sub>IH</sub>.

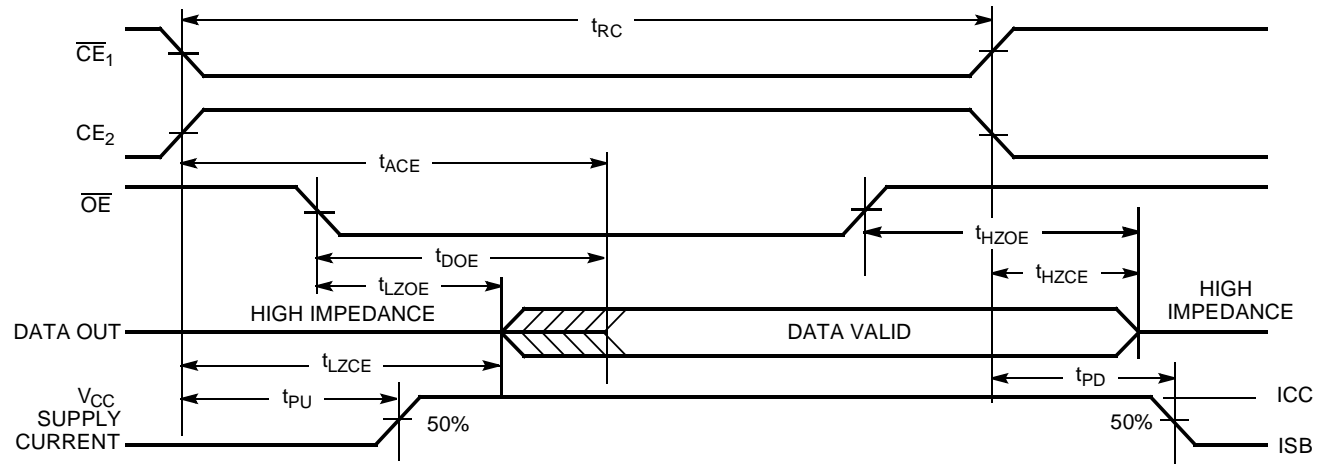
## Switching Waveforms

### Read Cycle No. 1<sup>[10, 11]</sup>



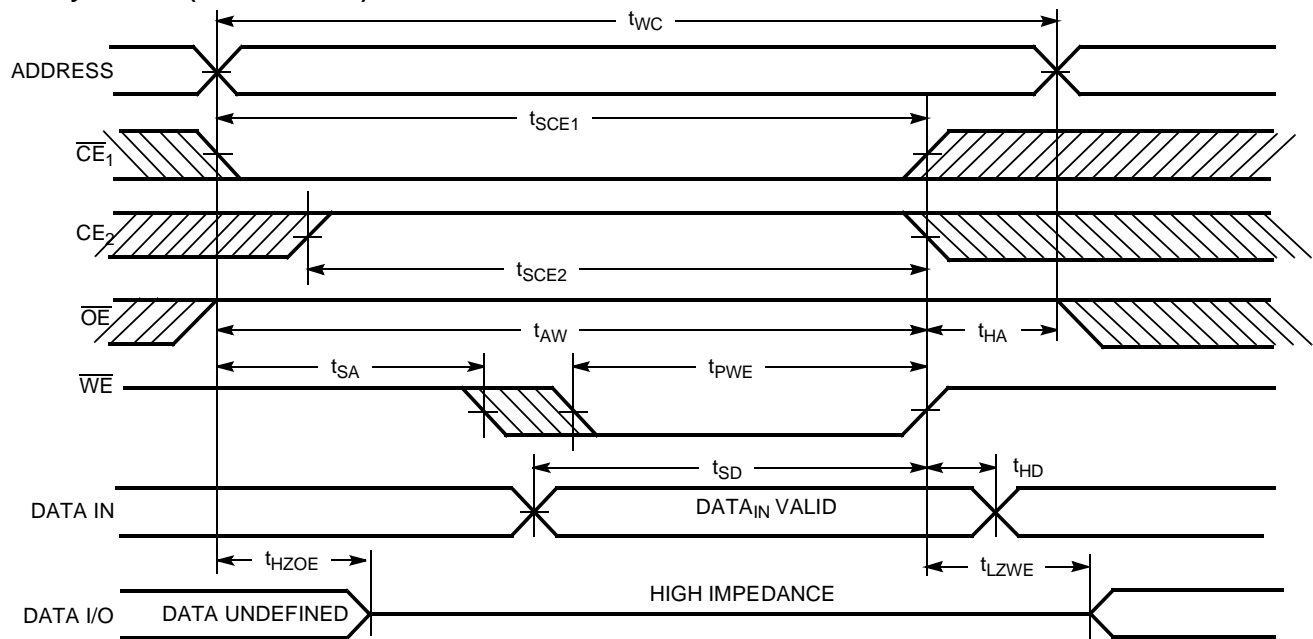
C185A-6

### Read Cycle No. 2<sup>[11, 12]</sup>



C185A-7

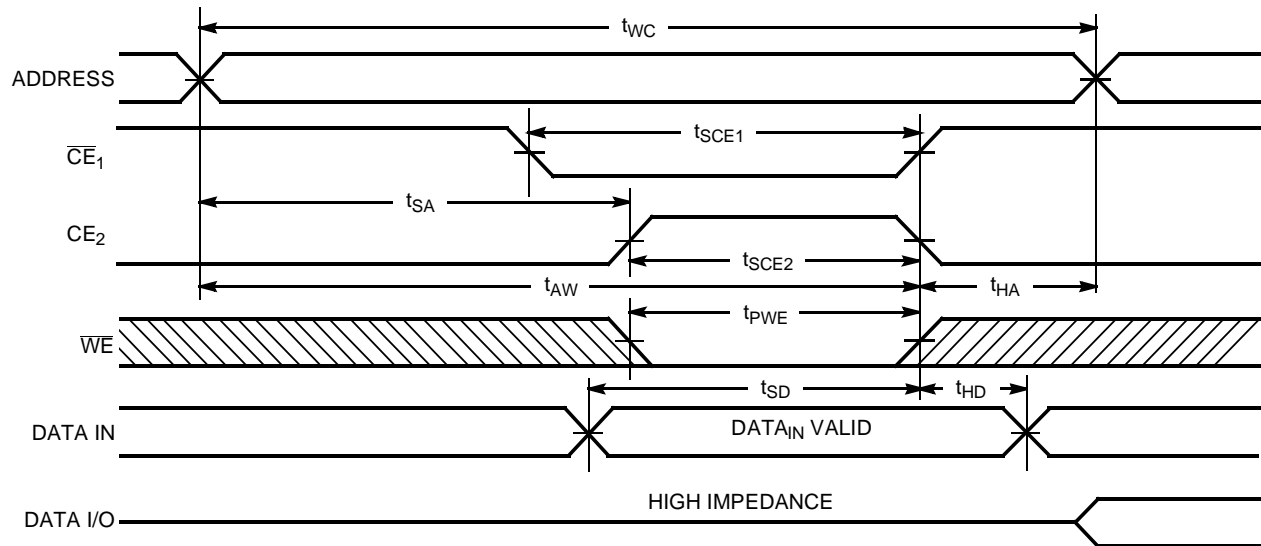
### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[13, 14]</sup>



C185A-8

#### Notes:

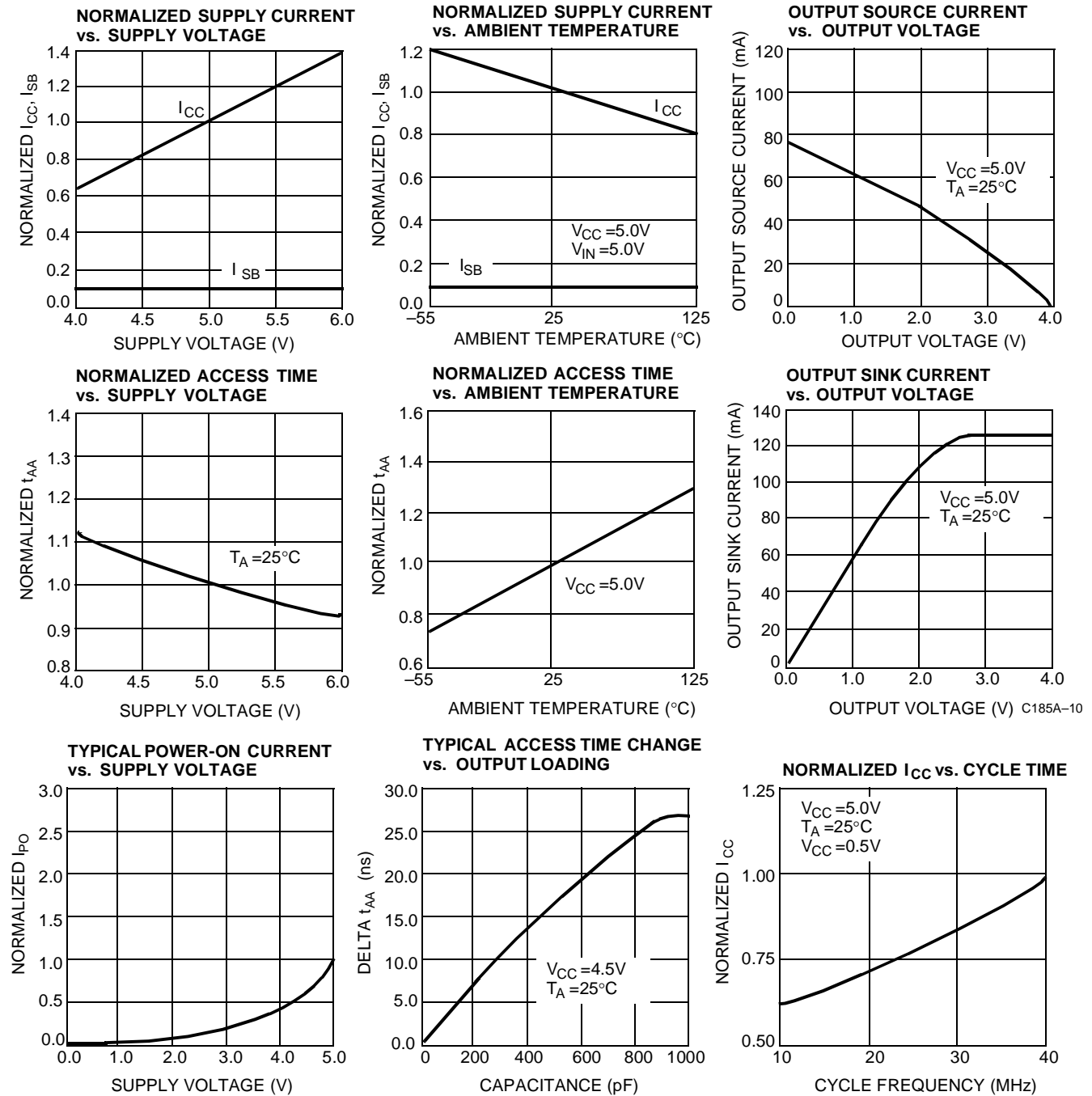
11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
12.  $\overline{WE}$  is HIGH for read cycle.
13. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. Data I/O is high impedance if  $OE = V_{IH}$ .

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[13, 14, 15]</sup>**


C185A-9

**Note:**

15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Typical DC and AC Characteristics**


C185A-11

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/ Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

**Address Designators**

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C185A-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C185A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
35	CY7C185A-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
45	CY7C185A-45DMB	D22	28-Lead (300-Mil) CerDIP	Military



**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL}$ Max.	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{OS}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB1}$	1, 2, 3
$I_{SB2}$	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
$t_{RC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{OHA}$	7, 8, 9, 10, 11
$t_{ACE1}$	7, 8, 9, 10, 11
$t_{ACE2}$	7, 8, 9, 10, 11
$t_{DOE}$	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
$t_{WC}$	7, 8, 9, 10, 11
$t_{SCE1}$	7, 8, 9, 10, 11
$t_{SCE2}$	7, 8, 9, 10, 11
$t_{AW}$	7, 8, 9, 10, 11
$t_{HA}$	7, 8, 9, 10, 11
$t_{SA}$	7, 8, 9, 10, 11
$t_{PWE}$	7, 8, 9, 10, 11
$t_{SD}$	7, 8, 9, 10, 11
$t_{HD}$	7, 8, 9, 10, 11

Document #: 38-00114-C

## Package Diagram

### 28-Lead (300-Mil) CerDIP D22

MIL-STD-1835 D-15 Config. A

