



CYPRESS

CY7C187

64K x 1 Static RAM

Features

- **High speed**
— 15 ns
- **CMOS for optimum speed/power**
- **Low active power**
— 495 mW
- **Low standby power**
— 220 mW
- **TTL compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C187 is a high-performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is pro-

vided by an active LOW Chip Enable (\overline{CE}) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 56% when deselected.

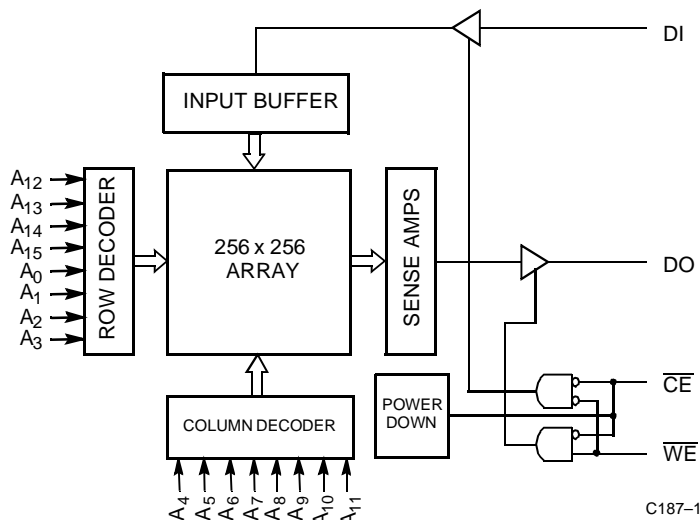
Writing to the device is accomplished when the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the Chip Enable (\overline{CE}) LOW, while Write Enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pin will appear on the data output (D_{OUT}) pin.

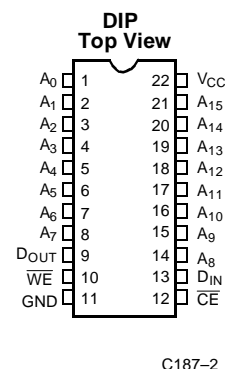
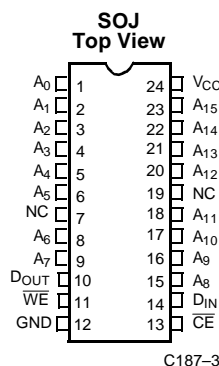
The output pin stays in high-impedance state when Chip Enable (\overline{CE}) is HIGH or Write Enable (\overline{WE}) is LOW.

The CY7C187 utilizes a die coat to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide^[1]

	7C187-15	7C187-20	7C187-25	7C187-35
Maximum Access Time (ns)	15	20	25	35
Maximum Operating Current (mA)	90	80	70	70
Maximum Standby Current (mA)	40/20	40/20	20/20	20/20

Note:

1. For military specifications, see the CY7C187A datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage to Ground Potential
(Pin 22 to Pin 11) -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[2] -0.5V to +7.0V

DC Input Voltage^[2] -0.5V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C187-15		7C187-20		7C187-25, 35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		90		80		70	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$		40		40		20	mA
I _{SB2}	Automatic \overline{CE} Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

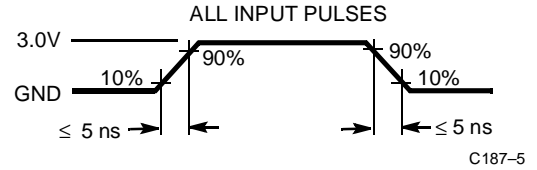
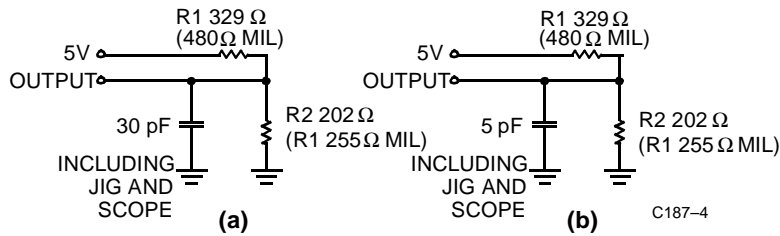
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[6]

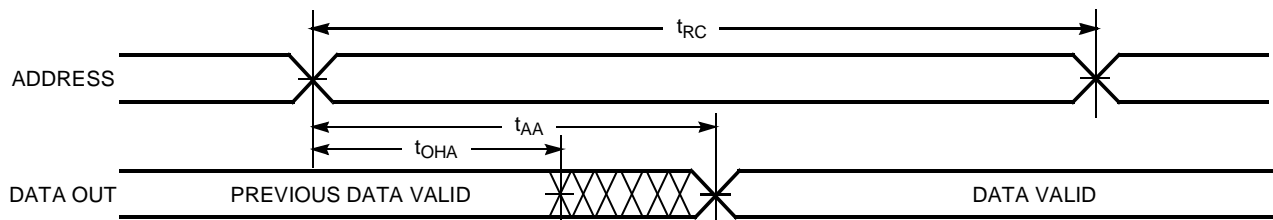
Parameter	Description	7C187-15		7C187-20		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	15		20		ns
t _{AA}	Address to Data Valid		15		20	ns
t _{OHA}	Output Hold from Address Change	3		5		ns
t _{ACE}	\overline{CE} LOW to Data Valid		15		20	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		8		8	ns
t _{PU}	\overline{CE} LOW to Power Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power Down		15		20	ns
WRITE CYCLE ^[9]						
t _{WC}	Write Cycle Time	15		20		ns
t _{SCE}	\overline{CE} LOW to Write End	12		15		ns
t _{AW}	Address Set-Up to Write End	12		15		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	12		15		ns
t _{SD}	Data Set-Up to Write End	10		10		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z	5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[8]		7		7	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range^[6] (continued)

Parameters	Description	7C187-25		7C187-35		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	25		35		ns
t _{AA}	Address to Data Valid		25		35	ns
t _{OHA}	Output Hold from Address Change	5		5		ns
t _{ACE}	\overline{CE} LOW to Data Valid		25		35	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		10		15	ns
t _{PU}	\overline{CE} LOW to Power Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power Down		20		20	ns
WRITE CYCLE ^[9]						
t _{WC}	Write Cycle Time	20		25		ns
t _{SCE}	\overline{CE} LOW to Write End	20		25		ns
t _{AW}	Address Set-Up to Write End	20		25		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	15		20		ns
t _{SD}	Data Set-Up to Write End	10		15		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low	5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[8]		7		10	ns

Switching Waveforms
Read Cycle No. 1^[10, 11]


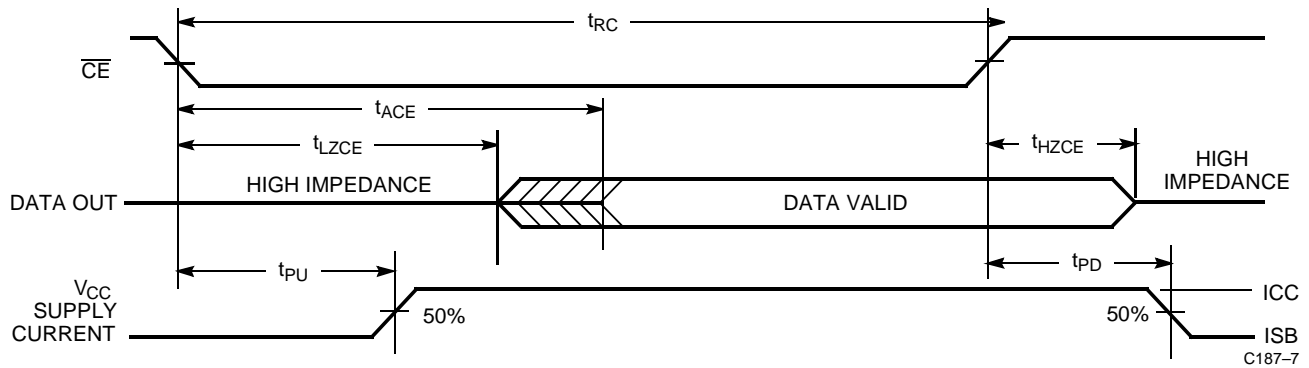
C187-6

Notes:

10. \overline{WE} is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.

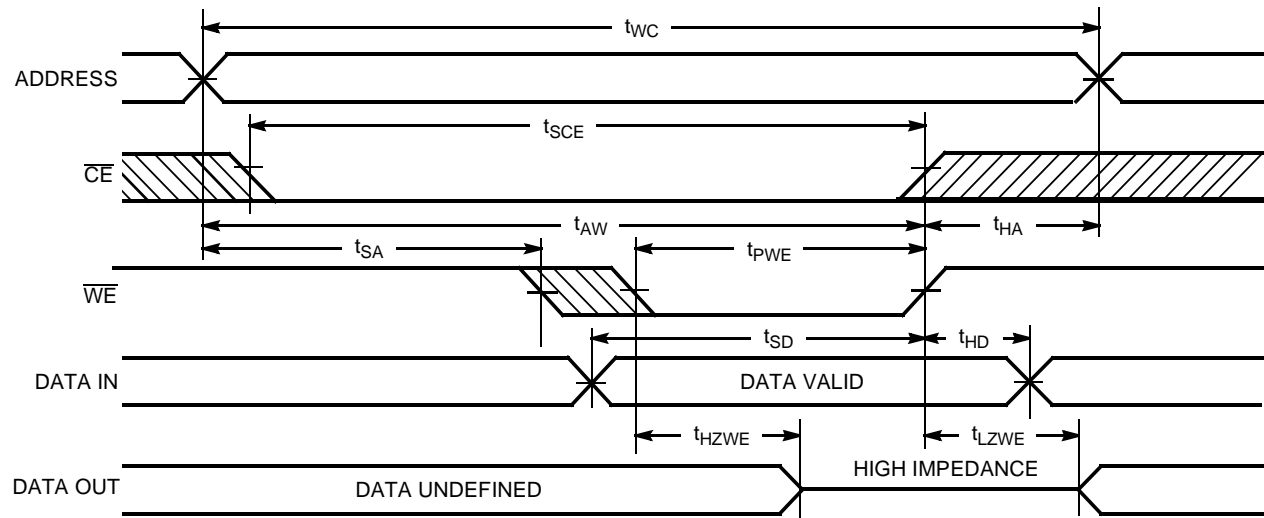
Switching Waveforms

Read Cycle No. 2^[10, 12]



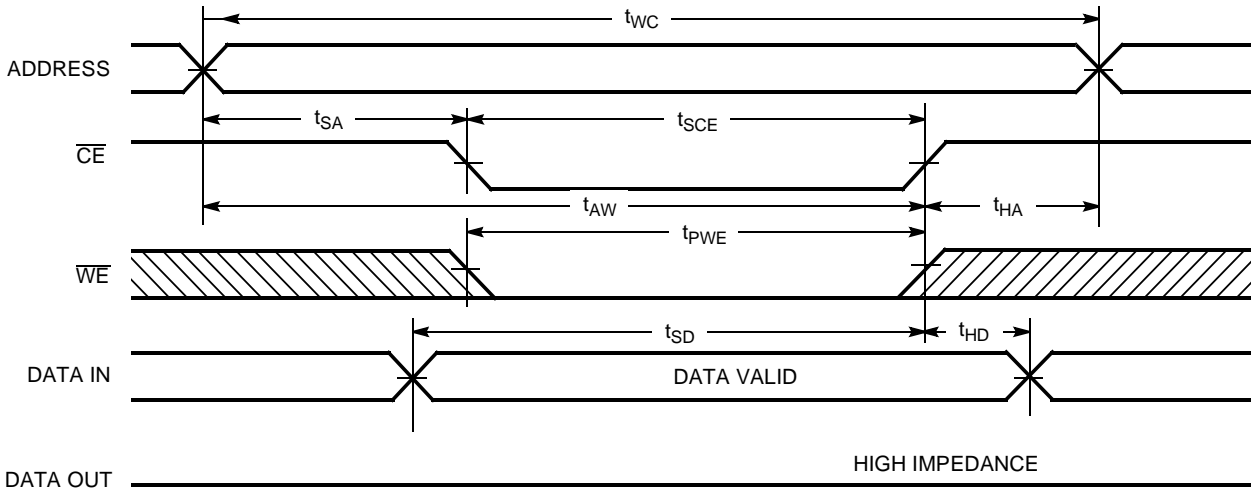
C187-7

Write Cycle No. 1 (\overline{WE} Controlled)^[11]



C187-8

Write Cycle No. 2 (\overline{CE} Controlled)^[11, 13]

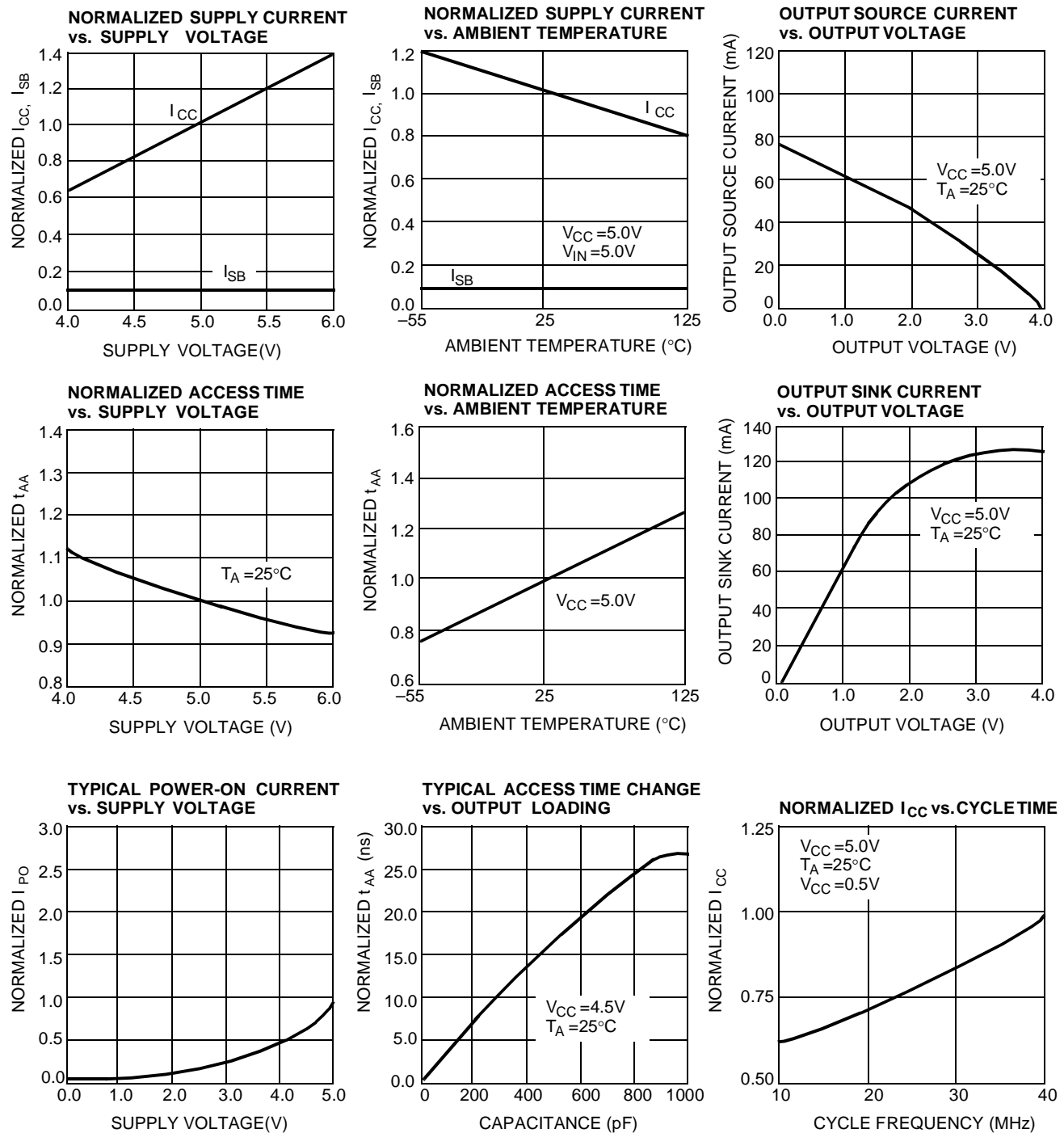


C187-9

Notes:

12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

\overline{CE}	\overline{WE}	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information^[14]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C187-15PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-15VC	V13	24-Lead Molded SOJ	
20	CY7C187-20PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-20VC	V13	24-Lead Molded SOJ	
25	CY7C187-25PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-25VC	V13	24-Lead Molded SOJ	
35	CY7C187-35PC	P9	22-Lead (300-Mil) Molded DIP	Commercial
	CY7C187-35VC	V13	24-Lead Molded SOJ	

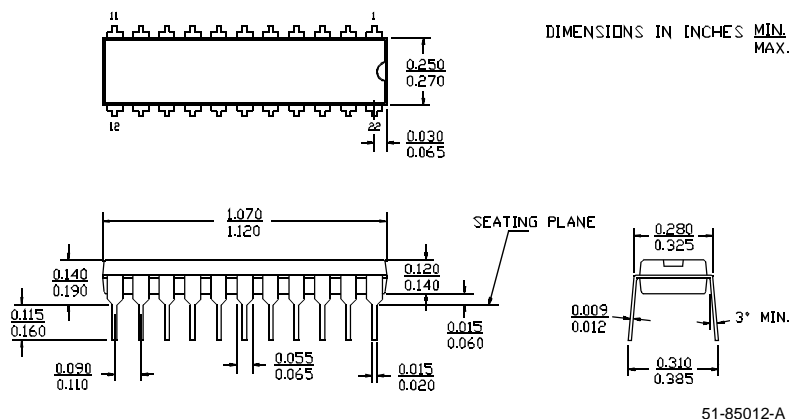
Note:

14. For military variations, see the CY7C187A datasheet.

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Package Diagrams

22-Lead (300-Mil) Molded DIP P9



24-Lead (300-Mil) Molded SOJ V13

