



CYPRESS

ADVANCE INFORMATION

CY62148CV25/30/33

MoBL™

## 512K x 8 MoBL Static RAM

### Features

- Low voltage range:
  - CY62148CV25: 2.2V–2.7V
  - CY62148CV30: 2.7V–3.3V
  - CY62148CV33: 3.0V–3.6V
- Ultra low active power
- Low standby power
- Automatic power-down when deselected
- CMOS for optimum speed/power

### Functional Description

The CY62148CV25/30/33 are high-performance CMOS static RAMs organized as 524,288 words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses

are not toggling. The device can be put into standby mode when deselected ( $\overline{CE}$  HIGH).

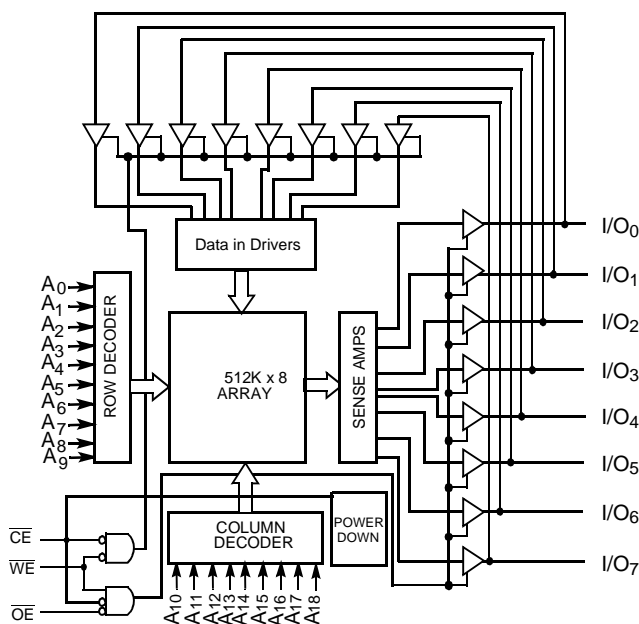
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

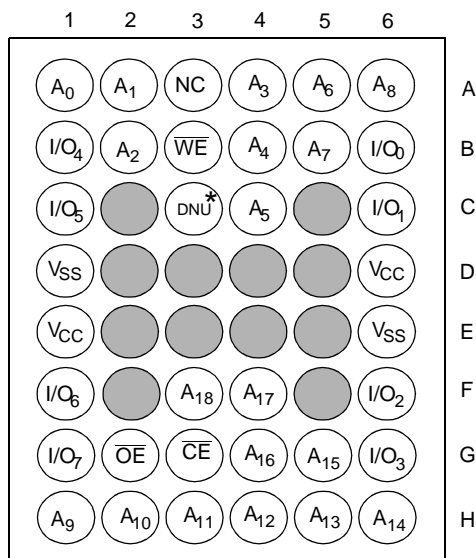
The CY62148CV25/30/33 are available in a 36-ball FBGA package. DNU\* on ball C3 is "Do Not Use" pin, connecting to Vss will not affect performance.

### Logic Block Diagram



MoBL and More Battery Life are trademarks of Cypress Semiconductor Corporation.

## Pin Configurations

**FBGA (Top View)**


\*=DNU, Do not use, connecting to  $V_{SS}$  will not affect performance

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature with  
Power Applied  $55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential  $-0.5\text{V}$  to  $+4.6\text{V}$

DC Voltage Applied to Outputs

in High Z State<sup>[1]</sup>  $-0.5\text{V}$  to  $V_{CC} + 0.5\text{V}$

DC Input Voltage<sup>[1]</sup>  $-0.5\text{V}$  to  $V_{CC} + 0.5\text{V}$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage  $>2001\text{V}$   
(per MIL-STD-883, Method 3015)

Latch-Up Current  $>200\text{ mA}$

## Operating Range

Product	Range	Ambient Temperature	$V_{CC}$
CY62148CV25	Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	2.2V to 2.7V
CY62148CV30			2.7V to 3.3V
CY62148CV33			3.0V to 3.6V

## Product Portfolio

Product	$V_{CC}$ Range			Speed	Power Dissipation (Industrial)					
					Operating ( $I_{CC}$ )				Standby ( $I_{SB2}$ )	
					55 ns		70 ns		Typ. <sup>[2]</sup>	Max.
	Min.	Typ. <sup>[2]</sup>	Max.		Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.		
CY62148CV25	2.2V	2.5V	2.7V	55,70 ns	12 mA	25 mA	7 mA	15 mA	5 $\mu\text{A}$	15 $\mu\text{A}$
CY62148CV30	2.7V	3.0V	3.3V	55,70 ns	12 mA	25 mA	7 mA	15 mA	7 $\mu\text{A}$	15 $\mu\text{A}$
CY62148CV33	3.0V	3.3V	3.6V	55,70 ns	12 mA	25 mA	7 mA	15 mA	8 $\mu\text{A}$	20 $\mu\text{A}$

### Notes:

1.  $V_{IL(\min.)} = -2.0\text{V}$  for pulse durations less than 20 ns.

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ.})}$ ,  $T_A = 25^{\circ}\text{C}$ .

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62148CV25-55			CY62148CV25-70			Unit
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA    V <sub>CC</sub> = Min.	2.0			2.0			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA    V <sub>CC</sub> = MinV			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.8		V <sub>CC</sub> +0.3V	1.8		V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.6	-0.3		0.6	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, (f = f <sub>MAX</sub> = 1/t <sub>RC</sub> ) CMOS Levels    V <sub>CC</sub> = 3.6V		12	25		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz CMOS Levels					1	2	
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE)		5	15		5	15	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0							

Parameter	Description	Test Conditions	CY62148CV30-55			CY62148CV30-70			Unit
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA    V <sub>CC</sub> = Min.	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA    V <sub>CC</sub> = MinV			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> +0.5V	2.2		V <sub>CC</sub> +0.5V	V
V <sub>IL</sub>	Input LOW Voltage		-0.3			-0.3		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, (f = f <sub>MAX</sub> = 1/t <sub>RC</sub> ) CMOS Levels    V <sub>CC</sub> = 3.6V		12	25		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz CMOS Levels		1	2		1	2	
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE)		7	15		7	15	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0							

Parameter	Description	Test Conditions		CY62148CV33-55			CY62148CV33-70			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = Min.	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = MinV			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> +0.5V	2.2		V <sub>CC</sub> +0.5V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, (f = f <sub>MAX</sub> = 1/t <sub>RC</sub> ) CMOS Levels	V <sub>CC</sub> = 3.6V		12	25		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz CMOS Levels			1	2		1	2	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			8	20		8	20	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$	LL							

### Capacitance<sup>3</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

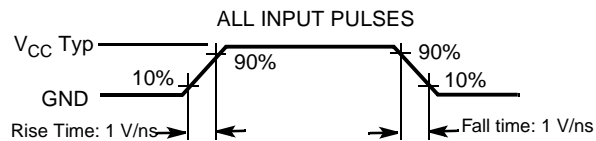
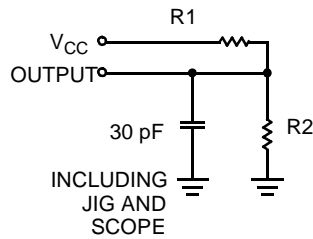
### Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance <sup>[3]</sup> (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance <sup>[3]</sup> (Junction to Case)		Θ <sub>JC</sub>	16	°C/W

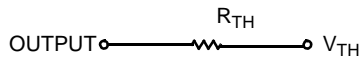
**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

#### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

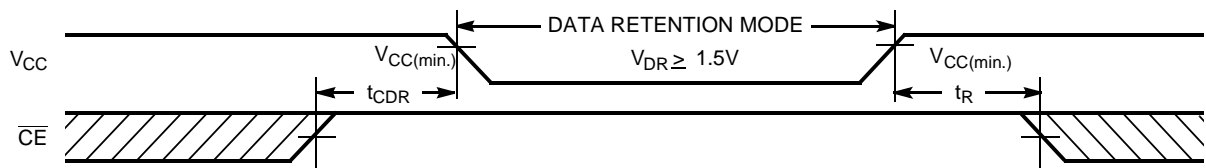


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.105	K $\Omega$
R2	15.4	1.550	1.550	K $\Omega$
$R_{TH}$	8	0.645	0.645	K $\Omega$
$V_{TH}$	1.20	1.75	1.75	V

#### Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5		$V_{CCmax}$	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5V$ $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed $V_{CC} + 0.3V$	LL	3	10	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[4]}$	Operation Recovery Time		70			ns

#### Data Retention Waveform



#### Note:

- Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$ .

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

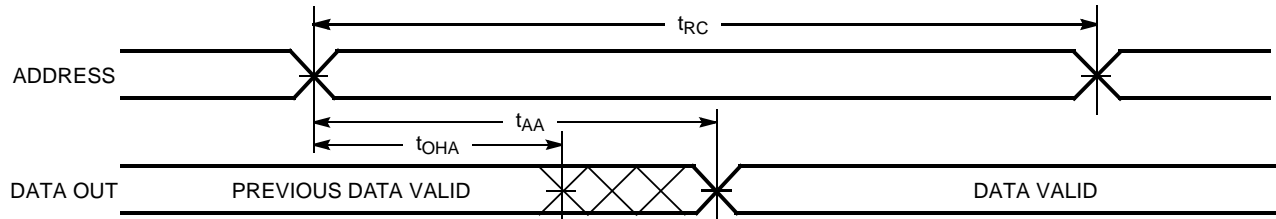
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		55		70	ns
WRITE CYCLE <sup>[8, 9]</sup>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	45		50		ns
t <sub>SD</sub>	Data Set-Up to Write End	30		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	5		10		ns

**Notes:**

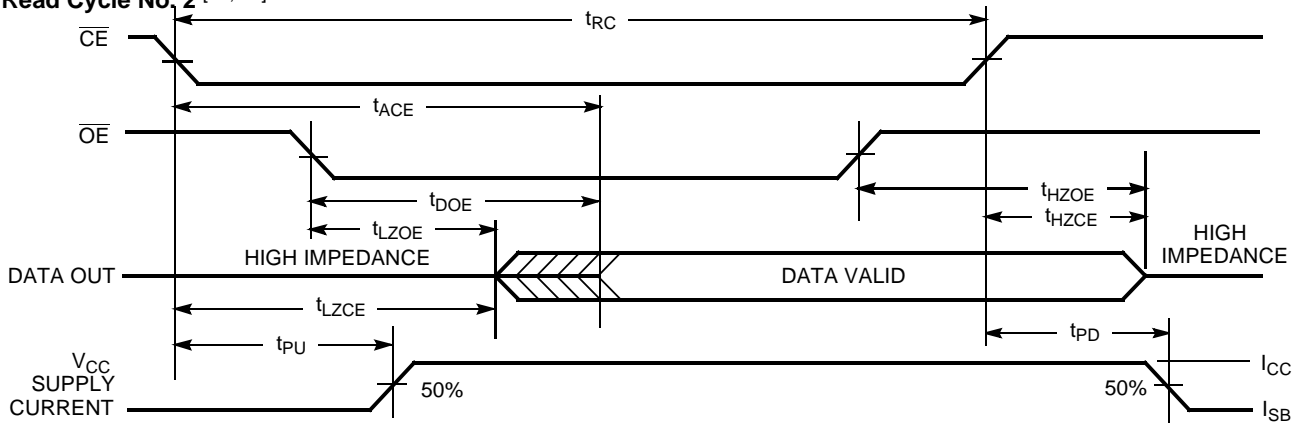
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

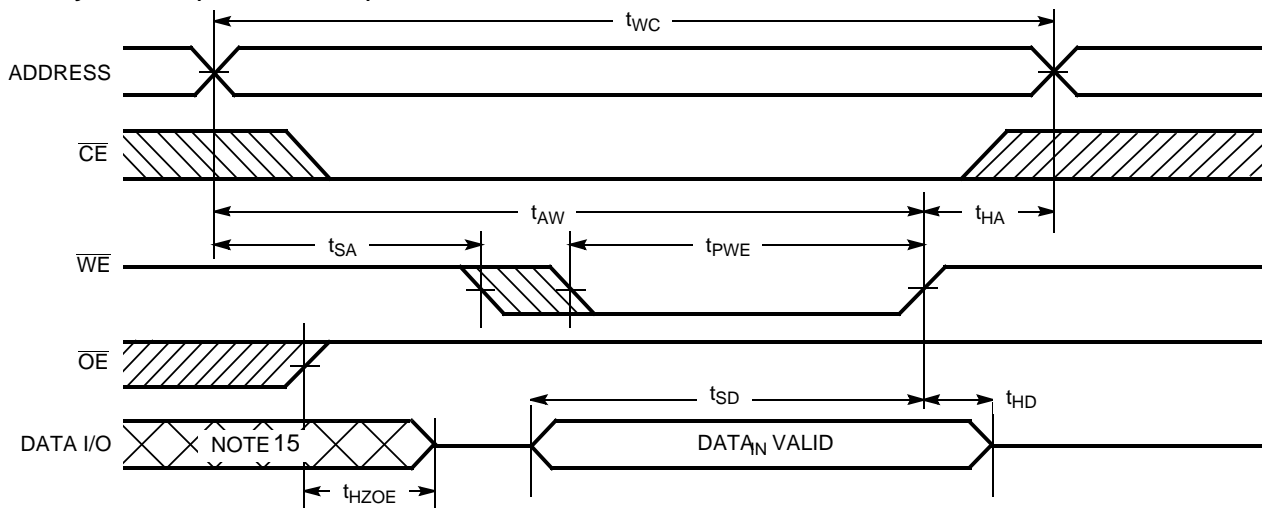
### Read Cycle No. 1<sup>[10, 11]</sup>



### Read Cycle No. 2<sup>[11, 12]</sup>

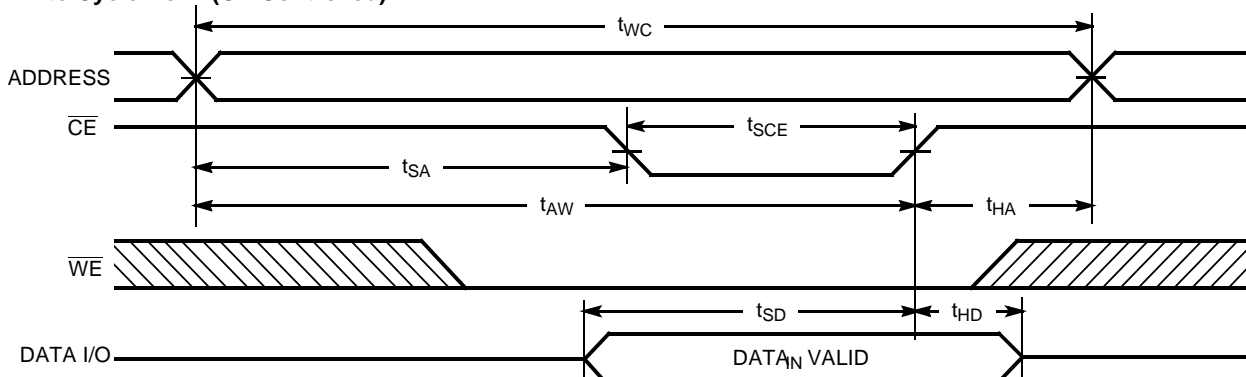
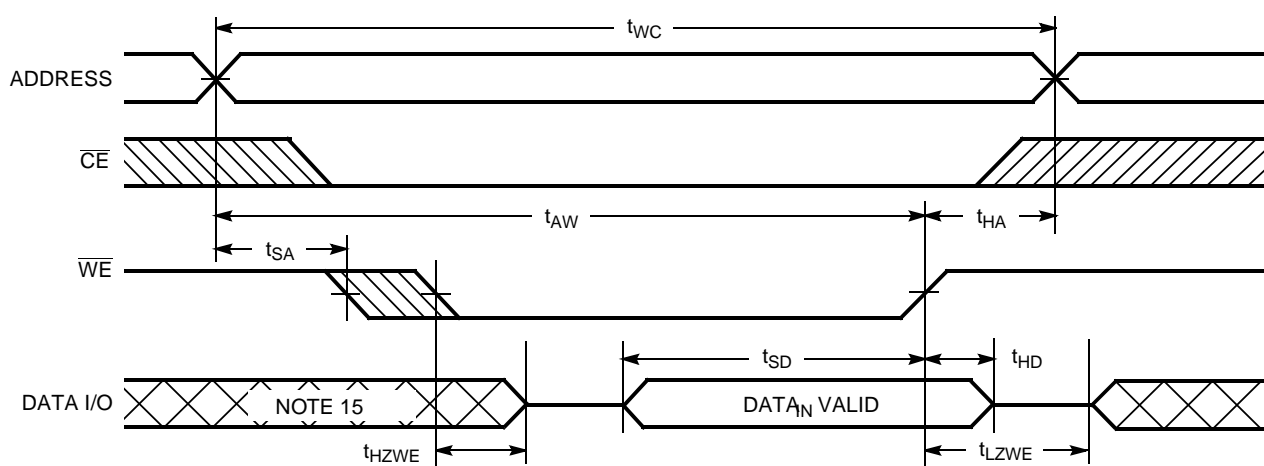


### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[8, 13, 14]</sup>



#### Notes:

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [8, 13, 14]

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [9, 14]

**Truth Table**

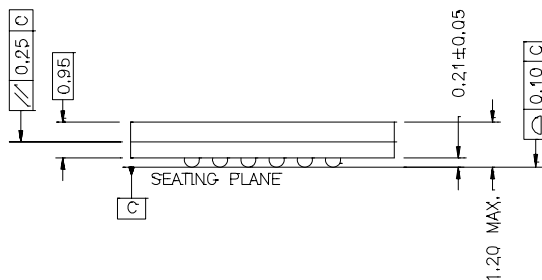
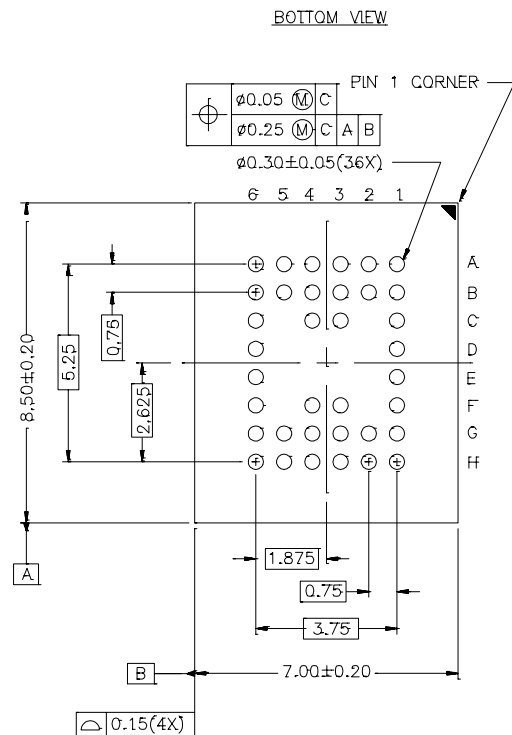
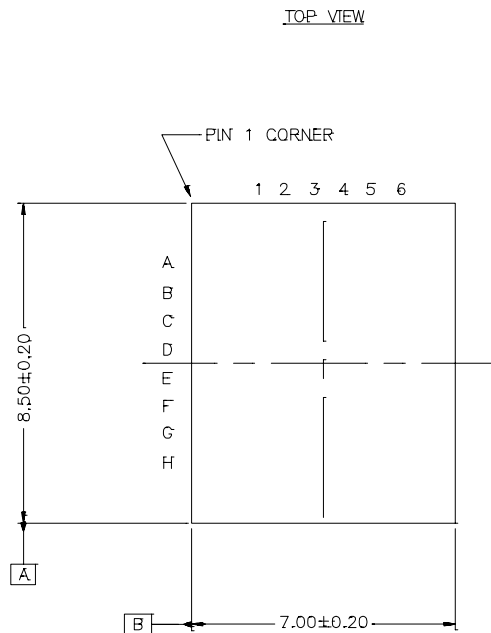
$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data Out	Read	Active ( $I_{\text{CC}}$ )
L	L	X	Data In	Write	Active ( $I_{\text{CC}}$ )
L	H	H	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )



**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148CV25LL-70BAI	BA36B	36-Ball Fine Pitch BGA	Industrial
	CY62148CV30LL-70BAI			
	CY62148CV33LL-70BAI			
55	CY62148CV25LL-55BAI			
	CY62148CV30LL-55BAI			
	CY62148CV33LL-55BAI			

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**Package Diagrams**
**36-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA36B**


51-85105-°C