

64K x 16 Static RAM

Features

- 2.7V–3.6V operation
- CMOS for optimum speed/power
- Low active power (70 ns, LL version)
— 54 mW (max.) (15 mA)
- Low standby power (70 ns, LL version)
— 54 μ W (max.) (15 μ A)
- Automatic power-down when deselected
— Power down either with \overline{CE} or \overline{BHE} and \overline{BLE} HIGH
- Independent control of Upper and Lower Bytes
- Available in 44-pin TSOP II (forward) and fBGA

Functional Description

The CY62127BV is a high-performance CMOS Static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption by 99% when deselected. The device enters power-down mode when \overline{CE} is HIGH or when \overline{CE} is LOW and both \overline{BLE} and \overline{BHE} are HIGH.

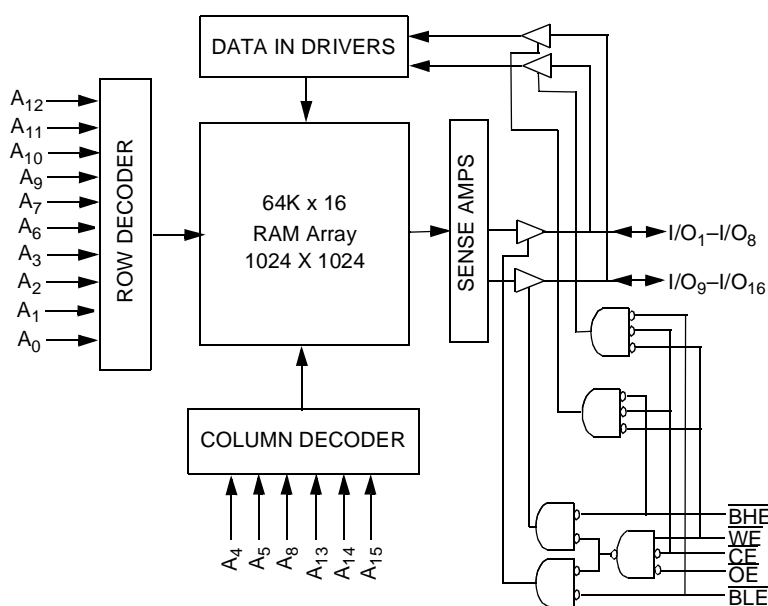
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₁ through I/O₈), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₉ through I/O₁₆) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O₁ to I/O₈. If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O₉ to I/O₁₆. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₁ through I/O₁₆) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY62127BV is available in standard 44-pin TSOP Type II (forward pinout) and fBGA packages.

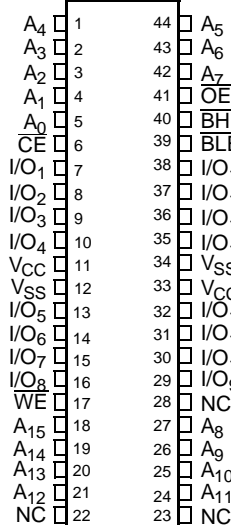
Logic Block Diagram



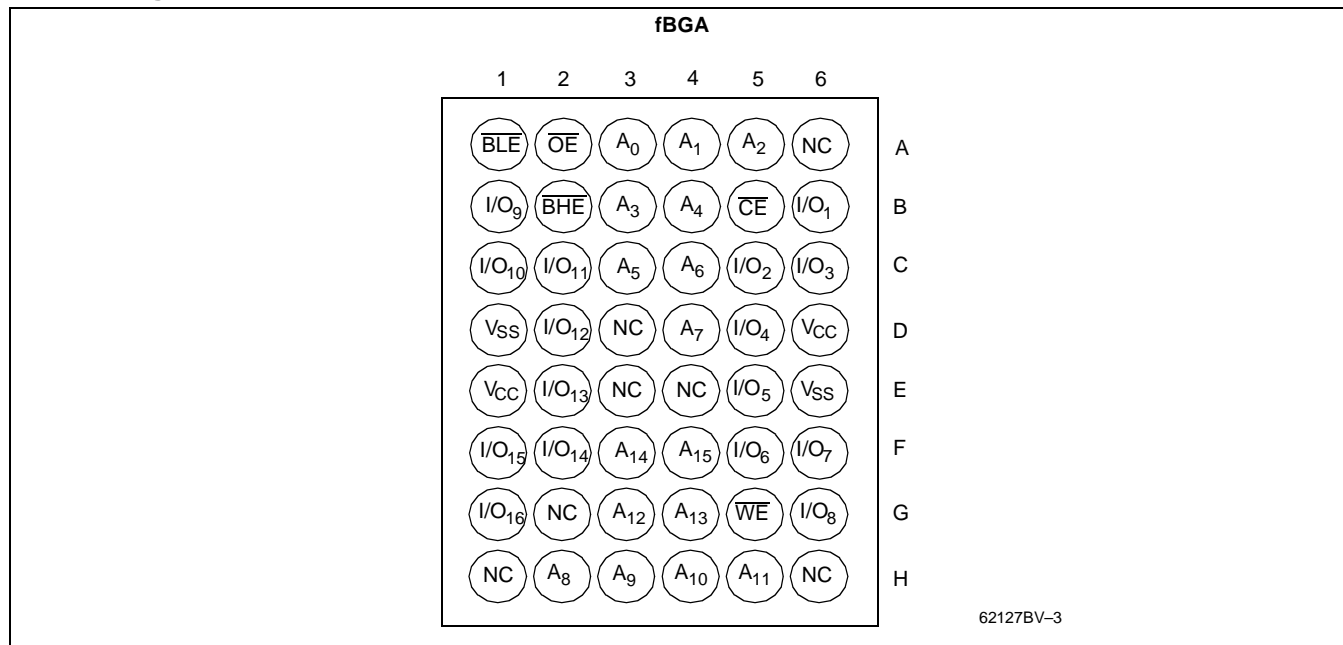
62127BV-1

Pin Configurations

TSOP II (Forward) Top View



62127BV-2

Pin Configurations (continued)

Selection Guide

	62127BV-55	62127BV-70	Units
Maximum Access Time	55	70	ns
Maximum Operating Current	20	15	mA
Maximum CMOS Standby Current	15	15	μA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Industrial	-40°C to +85°C	2.7V-3.6V

Notes:

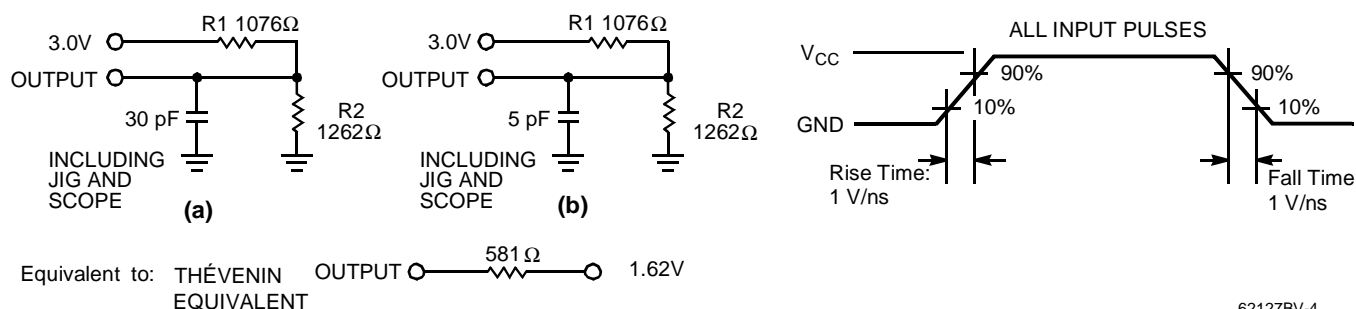
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	62127BV-55, 70			Unit
			Min.	Typ. ^[3]	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	2.2			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3		0.4	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.},$ $I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$	55 ns		20	mA
			70 ns		15	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$			2	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3\text{V},$ $V_{IN} \geq V_{CC} - 0.3\text{V},$ or $V_{IN} \leq 0.3\text{V}, f=0$		0.5	15	μA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 3.3\text{V}$	9	pF
C_{OUT}	Output Capacitance		9	pF

AC Test Loads and Waveforms


62127BV-4

Notes:

- Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ($T_A = 25^\circ\text{C}$, $V_{CC} = 3.0\text{V}$). Parameters are guaranteed by design and characterization, and not 100% tested.
- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[5] Over the Operating Range

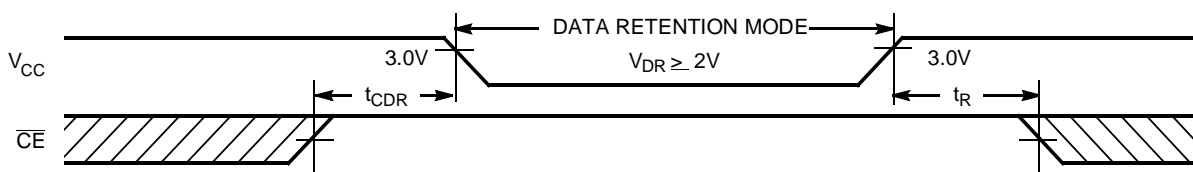
Parameter	Description	62127BV-55		62127BV-70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[7]	5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[6, 7]		20		25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[7]	10		10		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[6, 7]		20		25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		55		70	ns
t _{DBE}	Byte Enable to Data Valid		55		70	ns
t _{LZBE}	Byte Enable to LOW Z ^[7]	5		5		ns
t _{HZBE}	Byte Disable to HIGH Z ^[6, 7]		20		25	ns
WRITE CYCLE ^[8]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	40		50		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[7]	5		5		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[6, 7]		25		25	ns
t _{BW}	Byte Enable to End of Write	45		60		ns

Notes:

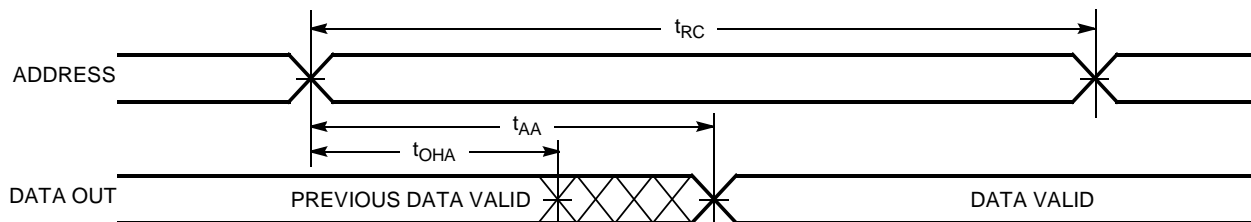
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- t_{HZOE}, t_{HZCE}, t_{HZWE}, and t_{HZBE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZWE} is less than t_{LZWE}, and t_{HZBE} is less than t_{LZBE}, for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write. Refer to truth table for further conditions from BHE and BLE.

Data Retention Characteristics (Over the Operating Range for “L” and “LL” version only)

Parameter	Description	Conditions ^[9]	Min.	Typ	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		3.6	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$.		0.5	15	μA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform


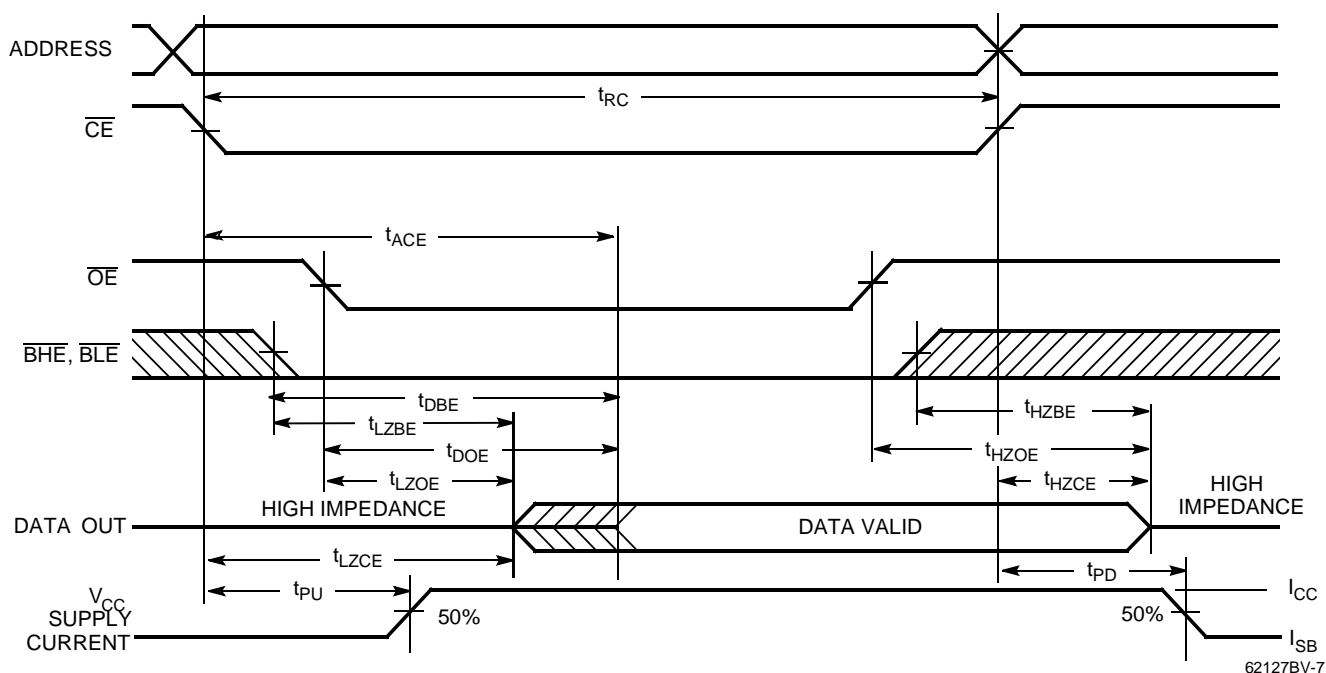
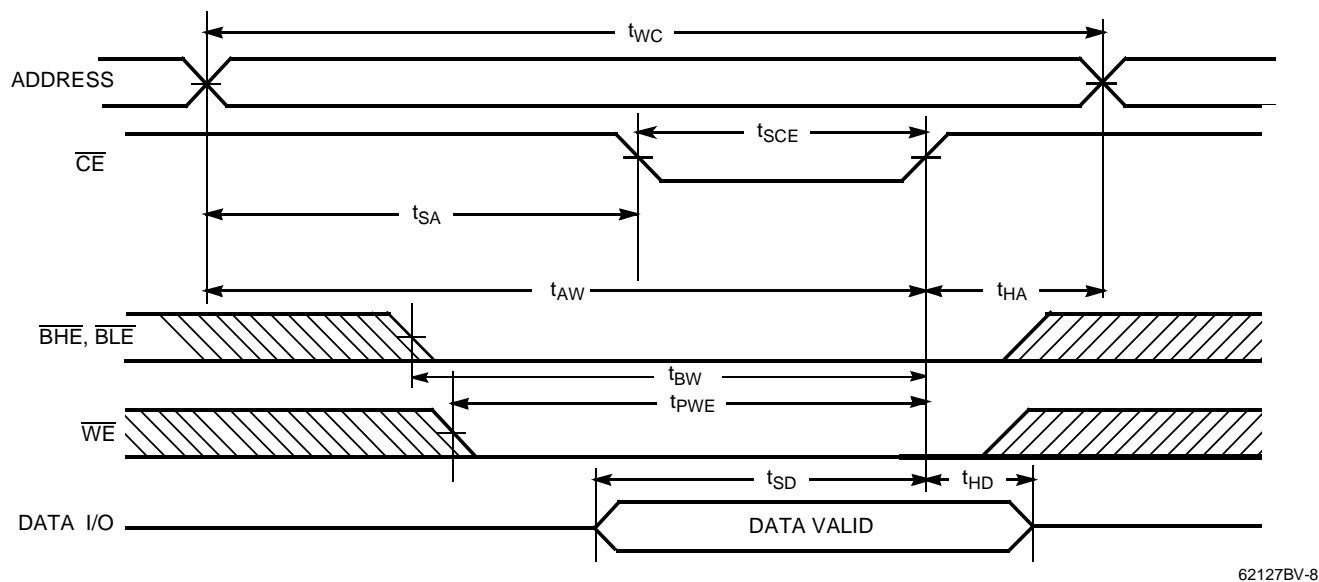
62127BV-5

Switching Waveforms
Read Cycle No.1^[10, 11]


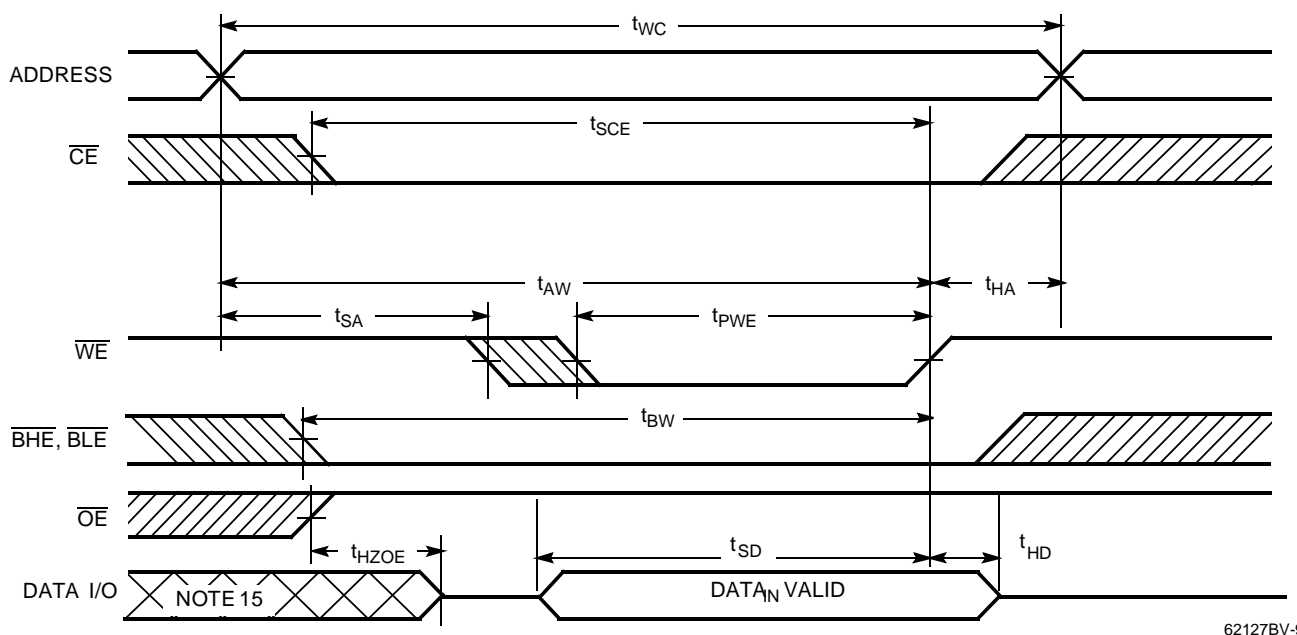
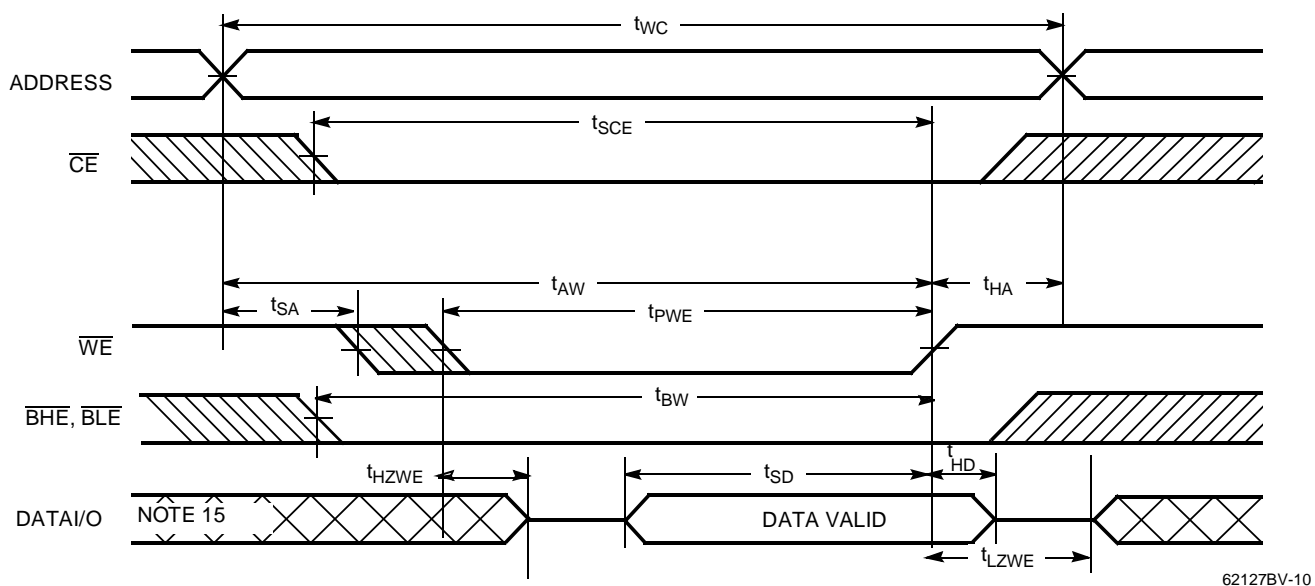
62127BV-6

Notes:

9. No input may exceed $V_{CC} + 0.3V$.
10. Device is continuously selected. $OE, CE, BHE, BLE = V_{IL}$.
11. WE is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 (\overline{OE} Controlled)^[11, 12, 13]

Write Cycle No. 1 (\overline{CE} Controlled)^[13, 14]

Notes:

12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$ or BHE and $BLE = V_{IH}$.
14. If \overline{CE} , BHE , or BLE go HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[13, 14]

Write Cycle No.3 (\overline{WE} Controlled, \overline{OE} LOW)^[13, 14]

Note:

15. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

CE	OE	WE	BLE	BHE	I/O ₁ –I/O ₈	I/O ₉ –I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I _{CC})
L	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I _{CC})
L	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I _{CC})
L	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I _{CC})
L	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I _{CC})
L	H	H	L	L	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Power Down	Standby (I _{SB})

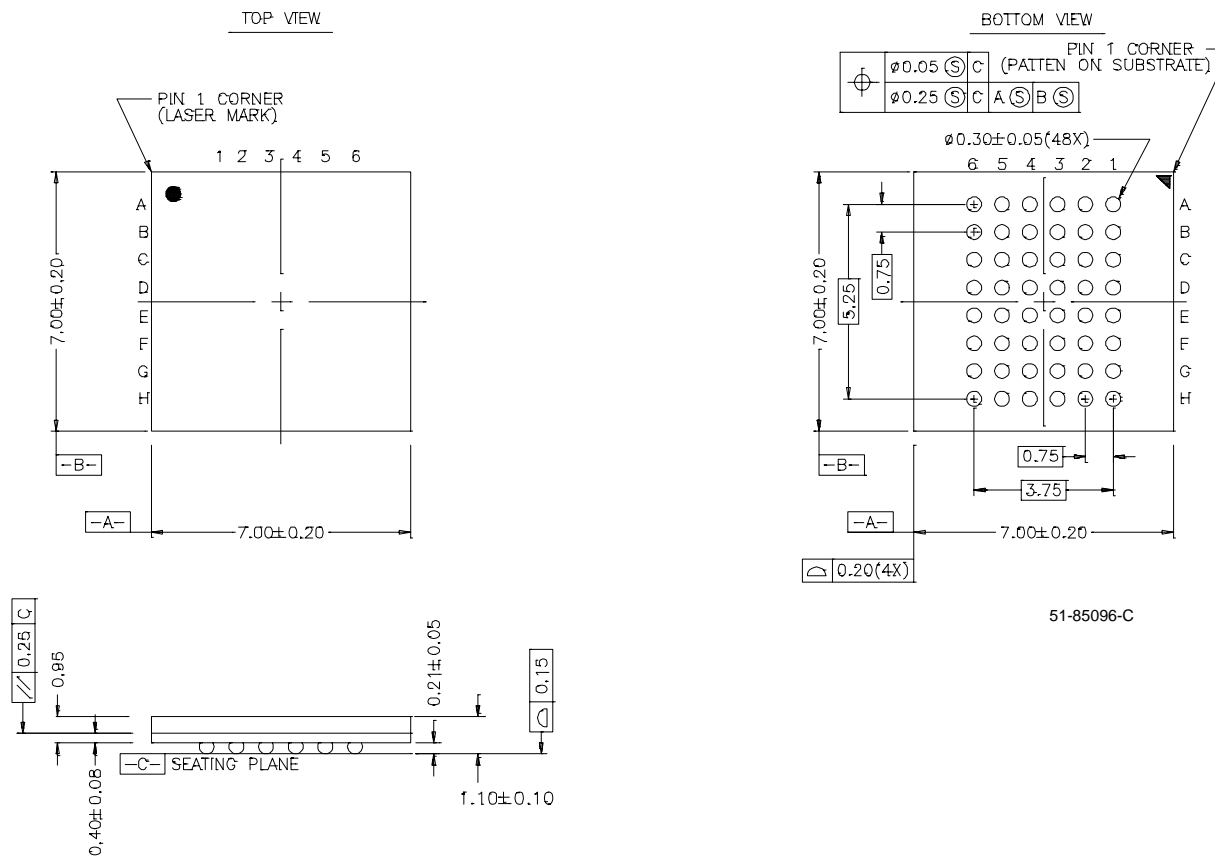
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62127BVLL-55ZI	Z44	44-Lead TSOP II	Industrial
	CY62127BVLL-55BAI	BA48	48-Ball Fine Pitch Ball Grid Array (fBGA)	
70	CY62127BVLL-70ZI	Z44	44-Lead TSOP II	
	CY62127BVLL-70BAI	BA48	48-Ball Fine Pitch Ball Grid Array (fBGA)	

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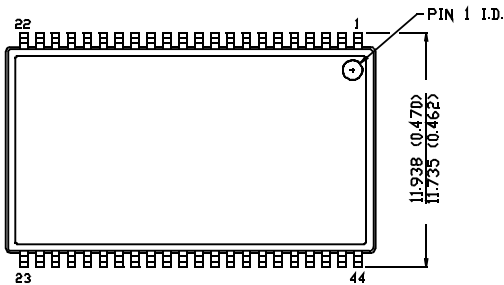
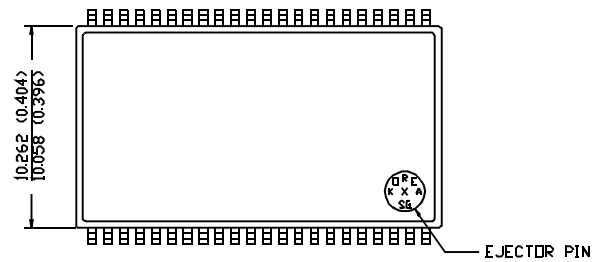
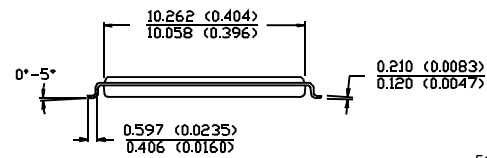
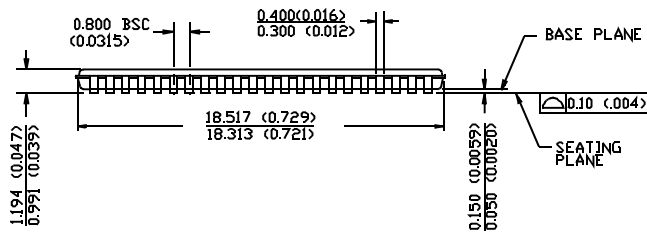
Package Diagrams

48-Ball (7.00 mm x 7.00 mm) Fine Pitch BGA BA48



Package Diagrams (continued)

44-Pin TSOP II Z44

 DIMENSION IN MM (INCH)
 MAX
 MIN

TOP VIEW

BOTTOM VIEW


51-85087-A