PRELIMINARY

CY62135V MoBL™
CY62135V18 MoBL2™

128K x 16 Flash Compatible Static RAM

Features

- **Low voltage range:**
  - **— CY62135V: 2.7V–3.3V**
  - **— CY62135V18: 1.65–1.95V**
- **Ultra-low active/standby power**
- **Easy memory expansion with $\overline{CE}$ /CE2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **Pin out compatible with standard Flash devices**
- **Shipped in Wafer/Die form**

Functional Description

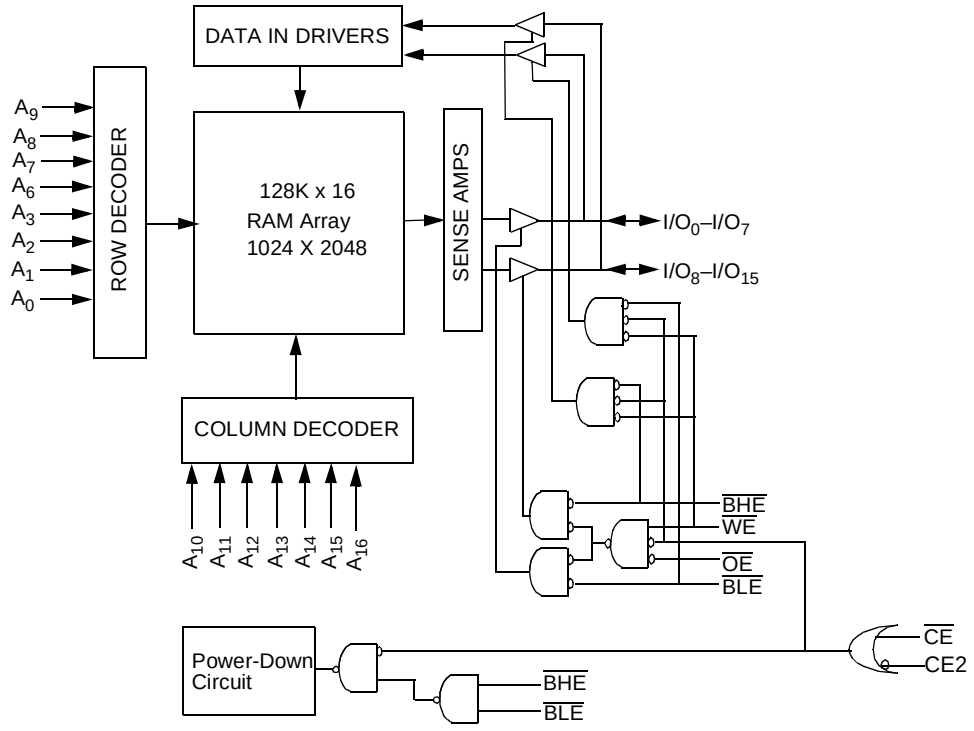
The CY62135V and CY62135V18 are high-performance CMOS static RAMs organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH or CE2 LOW) or when $\overline{CE}$ is LOW and when CE2 is HIGH and both $\overline{BLE}$ and $\overline{BHE}$ are HIGH[1]. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH or CE2 LOW), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, CE2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking chip enable ($\overline{CE}$) LOW, CE2 HIGH, and write enable ($\overline{WE}$) inputs LOW. If byte low enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If byte high enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW, CE2 HIGH, and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If byte high enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62135V/CY62135V18 are shipped in a wafer form.

Logic Block Diagram



Note:

1. Tying BBDISB to V_{CC} will disable the Byte Enable Power Down Feature. Tying it to V_{SS} will enable the Byte Enable Power Down Feature.

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Wafer and Die Specifications

Mechanical Specifications

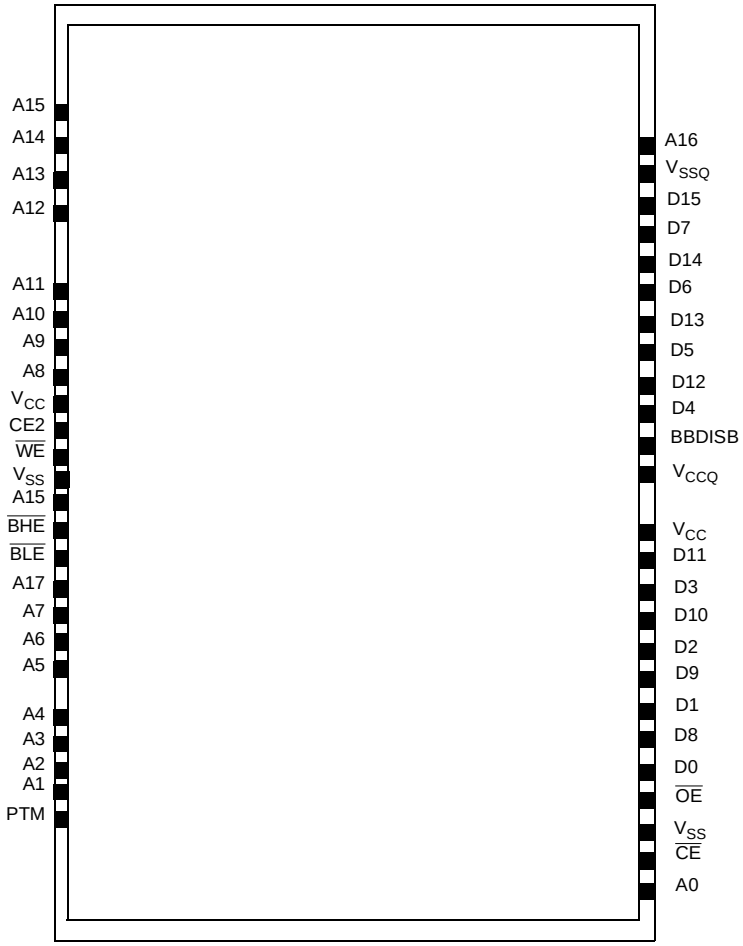
Process/Technology	CMOS, Double Metal, 0.25µ
Wafer Diameter	203.2 mm
Wafer Thickness, background	355.6 µm
Backside Wafer Surface	Silicon

Bond Pad Specifications

Bond Pad Opening	80µ
Topside Passivation	TBD
Bond Pad Metal Composition	300 A° Al, 0.5% Cu

Bond Pad Locations

The next figure shows the locations of the bond pads and table below provides the X and Y coordinates of these bond pads.



PAD Locations on Die (Die Size: 3.498 mm x 5.731 mm)

Pin Definitions

Pin Name	Location	Location	Function
A15	–1635.3	1944.925	Address
A14	–1635.300	1805.25	Address
A13	–1635.300	1633.7	Address
A12	–1635.300	1494.025	Address
A11	–1635.300	1102.475	Address
A10	–1635.300	962.8	Address
A9	–1635.300	791.275	Address
A8	–1635.300	651.575	Address
V_{CC}	–1635.300	514.275	Power
CE2	–1635.300	376.975	Active HIGH Chip Enable
$\overline{WEB}$	–1635.300	237.275	Active LOW Write Enable
V_{SS}	–1635.300	–186.65	Ground
$\overline{BHE}$	–1635.300	–323.95	Active LOW Byte High Enable
$\overline{BLE}$	–1635.300	–463.625	Active LOW Byte Low Enable
NC	–1635.300	–635.175	Address Expansion for 4M
A7	–1635.300	–774.85	Address
A6	–1635.300	–946.4	Address
A5	–1635.300	–1086.075	Address
A4	–1635.300	–1477.625	Address
A3	–1635.300	–1617.3	Address
A2	–1635.300	–1788.85	Address
A1	–1635.300	–1928.525	Address
A0	1618.575	–2099.425	Address
$\overline{CE}$	1618.575	–1959.725	Active LOW Chip Enable
V_{SS}	1618.575	–1821.525	Ground
$\overline{OE}$	1618.575	–1700.45	Active LOW Output Enable
D0	1618.575	–1528.925	I/O Data Bus
D8	1618.575	–1348.475	I/O Data Bus
D1	1618.575	–1147.25	I/O Data Bus
D9	1618.575	–966.8	I/O Data Bus
D2	1618.575	–795.25	I/O Data Bus
D10	1618.575	–614.8	I/O Data Bus
D3	1618.575	–413.575	I/O Data Bus
D11	1618.575	–233.125	I/O Data Bus
V_{CC}	1618.575	–95.825	Power
V_{CCQ}	1618.575	251.375	Power for I/O Pins
BBDISB	1618.575	389.6	Byte Enable Power Down Disable[1]
D4	1618.575	533.65	I/O Data Bus
D12	1618.575	714.1	I/O Data Bus
D5	1618.575	915.325	I/O Data Bus
D13	1618.575	1095.775	I/O Data Bus
D6	1618.575	1267.3	I/O Data Bus
D14	1618.575	1447.75	I/O Data Bus
D7	1618.575	1648.975	I/O Data Bus
D15	1618.575	1829.425	I/O Data Bus
V_{SSQ}	1618.575	1970.675	Ground for I/O Pins
A16	1618.575	2091.925	Address
PTM	–1635.300	–2295.050	Parallel Test Mode Pad, internally held low with a resistor, meant for testing purposes only.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62135V	Industrial	–40°C to +85°C	2.7V to 3.3V
CY62135V18	Industrial	–40°C to +85°C	1.65V to 1.95V

Shaded areas contain advance information.

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Commercial)			
					Operating (I_{CC})		Standby (I_{SB2})	
	$V_{CC(min)}$	$V_{CC(typ)}$[3]	$V_{CC(max)}$		Typ.[3]	Maximum	Typ.[3]	Maximum
CY62135V	2.7V	3.0V	3.3V	70 ns	7	12 mA	1 µA	10 µA
CY62135V18	1.65V	1.8V	1.95V	70 ns	3	7 mA	1 µA	15 µA

Shaded areas contain advance information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62135V			Unit
				Min.	Typ.[3]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = 2.7V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V			0.4	V
V_{IH}	Input HIGH Voltage		V_{CC} = 3.3V	2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V	–0.5		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	±1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS levels	V_{CC} = 3.3V		7	12	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I_{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}				100	µA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0			1	10	µA

Notes:

2. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.

Electrical Characteristics Over the Operating Range

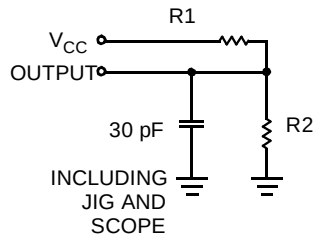
Parameter	Description	Test Conditions		CY62135V18 Min.	CY62135V18 Typ.[3]	CY62135V18 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65V	1.5			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65V			0.2	V
V_{IH}	Input HIGH Voltage		V_{CC} = 1.95V	1.4		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage		V_{CC} = 1.65V	–0.5		0.4	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	±1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}, CMOS levels	V_{CC} = 1.95V		3	7	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I_{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}				100	µA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0			1	15	µA

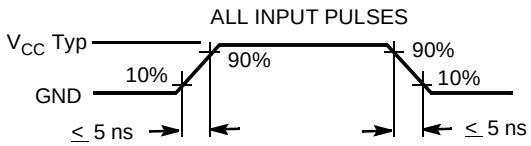
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

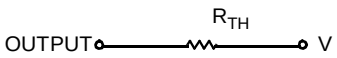
Note:
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



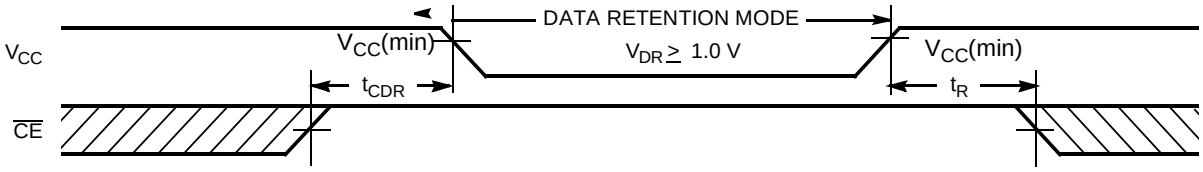
Parameters	3.0V	1.8V	UNIT
R1	1105	15294	Ohms
R2	1550	11300	Ohms
R_{TH}	645	6500	Ohms
V_{TH}	1.75	0.85	Volts

Shaded area contain advanced information.

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[5]	Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention (CY62135V18)		1.0		1.95	V
V_{DR}	V_{CC} for Data Retention (CY62135V)		1.0		3.3	V
I_{CCDR}	Data Retention Current	V_{CC} = 1.0V $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed V_{CC}+0.3V		0.1	1	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Note:

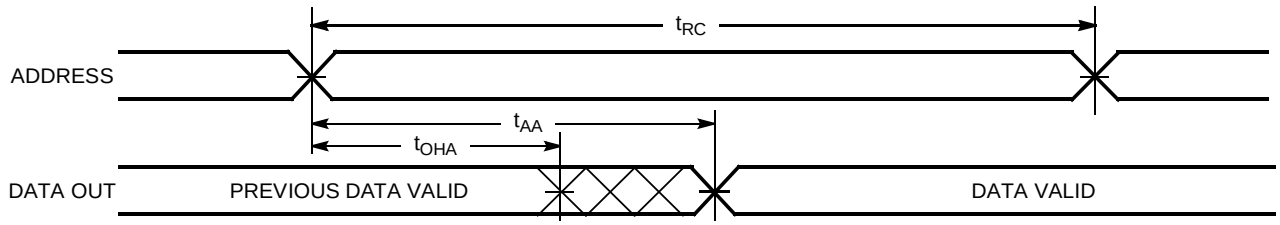
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

Switching Characteristics Over the Operating Range[5]

Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		70	ns
t_{DBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		70	ns
t_{LZBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z	10		ns
t_{HZBE}	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z		25	ns
WRITE CYCLE[8, 9]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	10		ns

Switching Waveforms

Read Cycle No. 1[10,11]

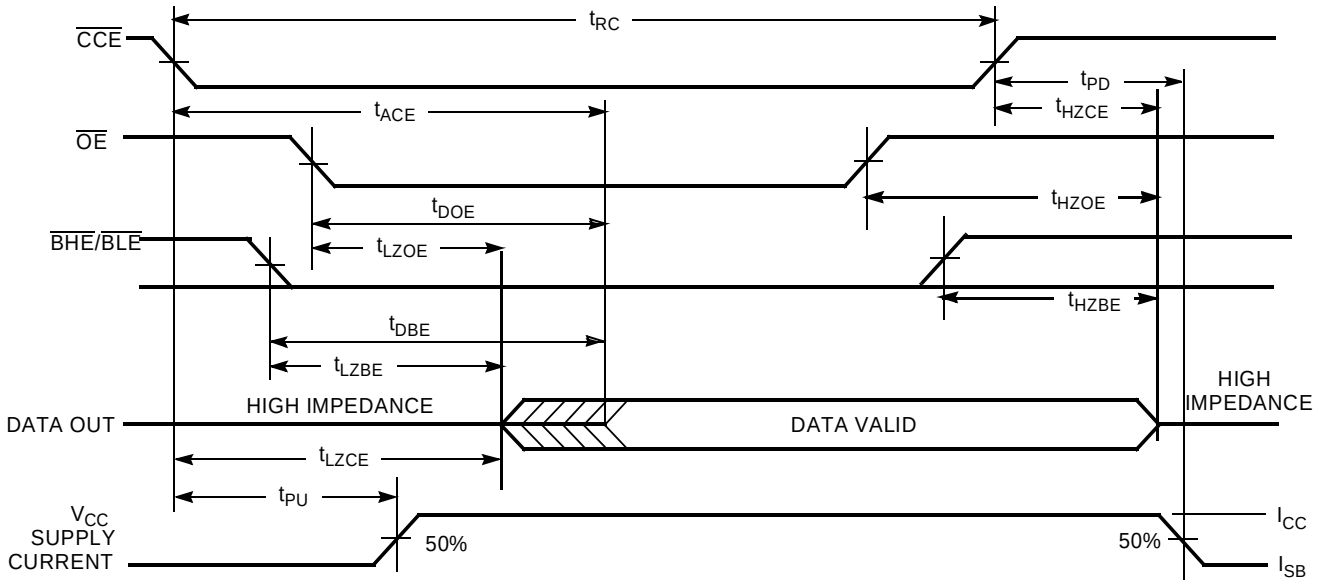


Notes:

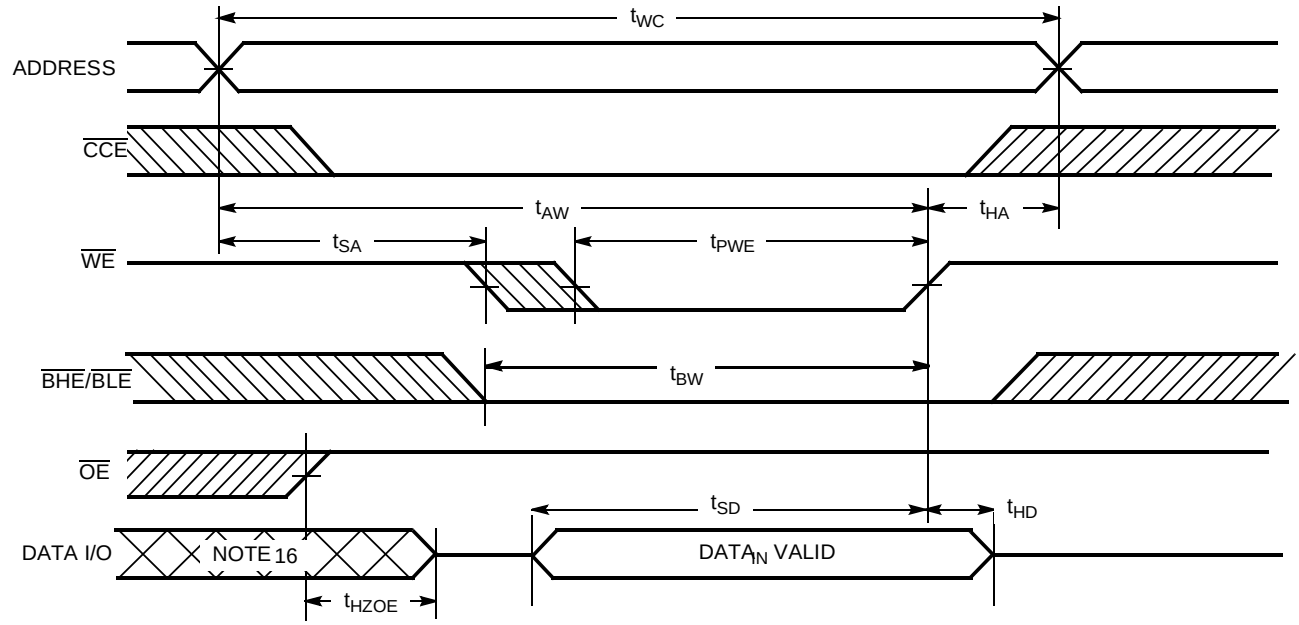
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, CE2 = V_{IH}.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 [11, 12, 13]



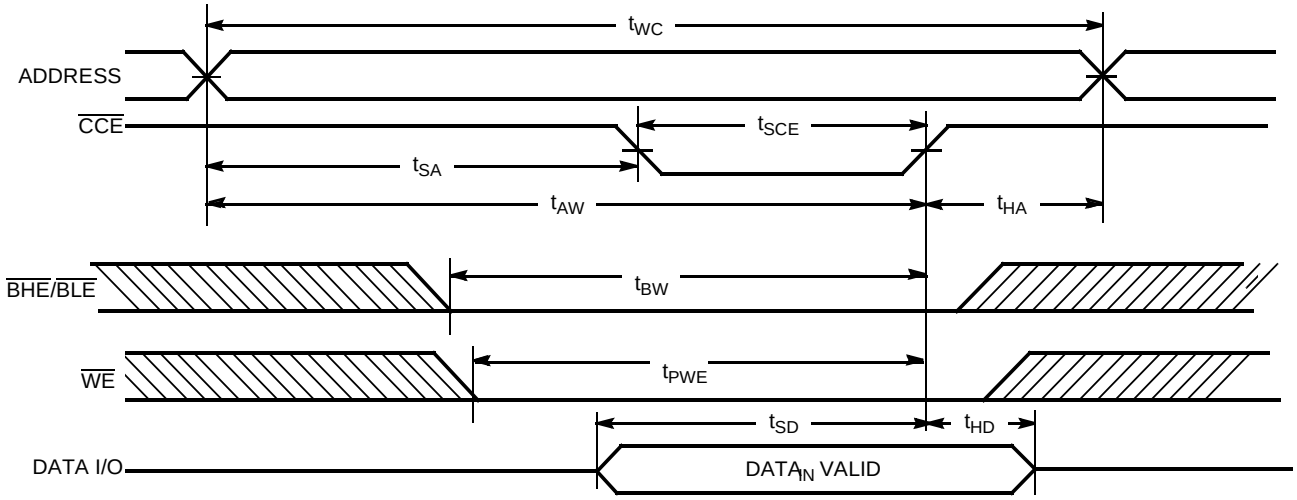
Write Cycle No. 1 (WE Controlled) [8, 12, 14, 15]



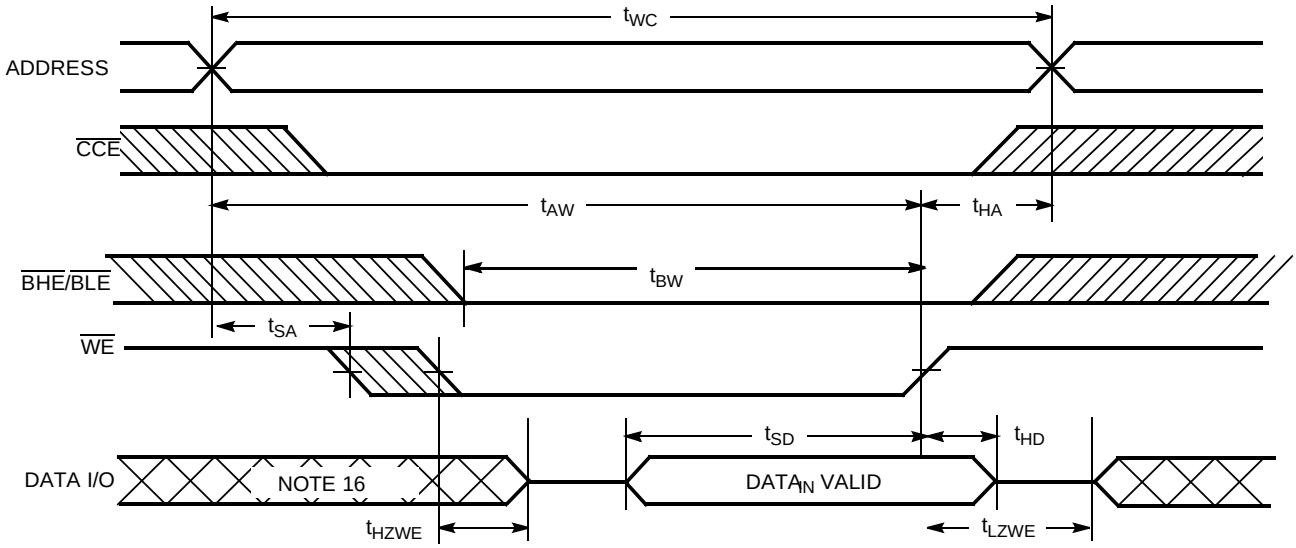
Notes:
12. CCE is the combination of both CE and CE2(CE = V_{IL}, CE2 = V_{IH}).
13. Address valid prior to or coincident with CE transition LOW.
14. Data I/O is high impedance if OE = V_{IH}.
15. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

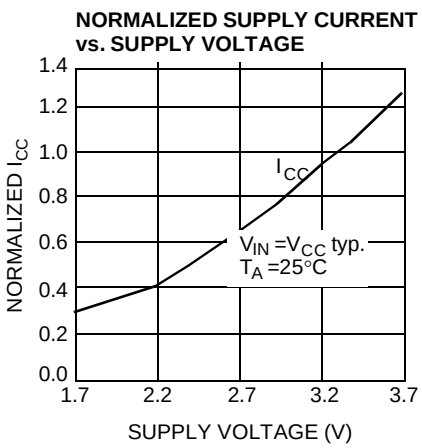
Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12, 14, 15]

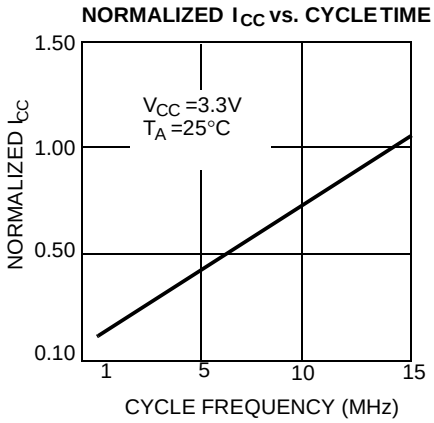


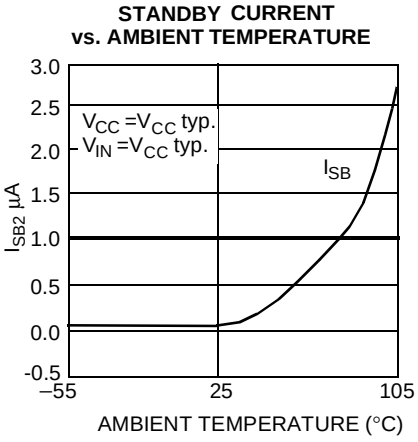
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 12, 15]



Typical DC and AC Characteristics







Truth Table

$\overline{CE}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode
H	X	X	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	X	X	High Z	Deselect/Power-Down
X	X	X	X	H	H	High Z[1]	Deselect/Power-Down[1]
L	H	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read
L	H	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read
L	H	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0 –I/O_7 in High Z	Read
L	H	H	H	L	L	High Z	Deselect/Output Disabled
L	H	H	H	H	L	High Z	Deselect/Output Disabled
L	H	H	H	L	H	High Z	Deselect/Output Disabled
L	H	L	X	L	L	Data In (I/O_O–I/O_{15})	Write
L	H	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write
L	H	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62135V-WAF	TBD	Wafer Boxes	Industrial
70	CY62135V18-WAF	TBD	Wafer Boxes	Industrial

Shaded areas contain advance information.

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