CY62137CV18 MoBL2™

128K x 16 Static RAM

Features

- **Low voltage range:**
  - **CY62137CV18: 1.65V–1.95V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

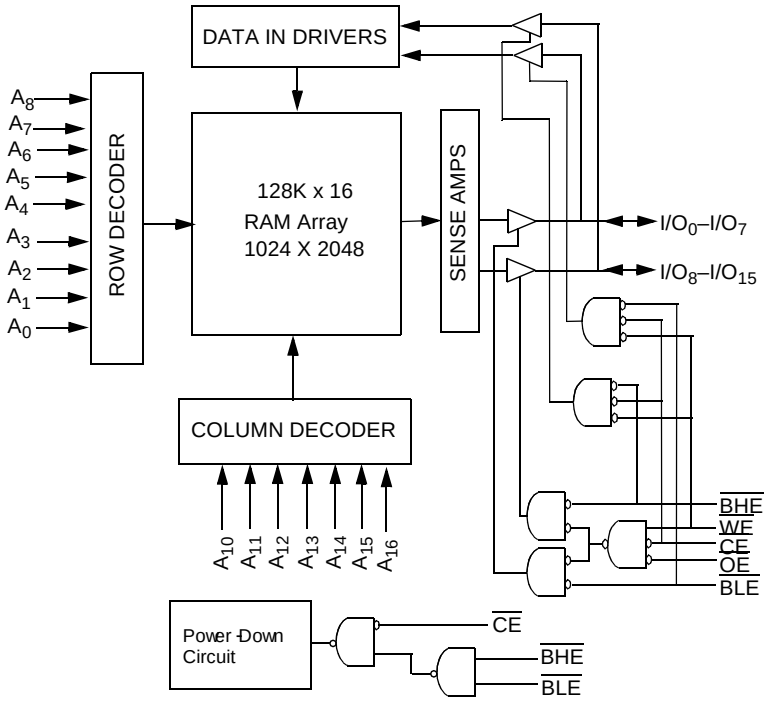
The CY62137CVApril 27, 200118 is a high-performance CMOS static RAM organized as 131,072 words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH) or when $\overline{CE}$ is LOW and both $\overline{BLE}$ and $\overline{BHE}$ are HIGH. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

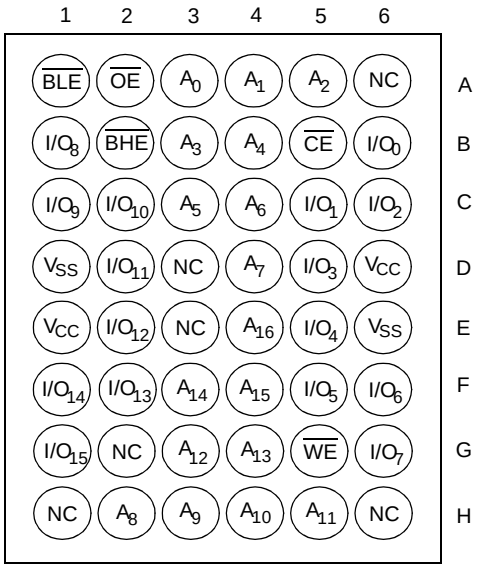
The CY62137CV18 is available in 48-ball FBGA packaging.

Logic Block Diagram



Pin Configuration

FBGA
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with
Power Applied–55°C to +125°C

Supply Voltage to Ground Potential–0.5V to +2.4V

DC Voltage Applied to Outputs
in High Z State[1]–0.5V to V_{CC} + 0.5V

DC Input Voltage[1]–0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62137CV18	Industrial	–40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V_{CC} Range			Power	Power Dissipation (Industrial)			
					Operating (I_{CC})		Standby (I_{SB2})	
	$V_{CC(min.)}$	$V_{CC(typ.)}$[2]	$V_{CC(max.)}$		Typ.[2]	Max.	Typ.[2]	Max
CY62137CV18	1.65V	1.80V	1.95V	LL	4 mA	7 mA	1 µA	8 µA

Notes:
1. V_{IL}(min.) = –2.0V for pulse durations less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ., T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62137CV18 Min.	CY62137CV18 Typ.[2]	CY62137CV18 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65V		1.5			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65V				0.2	V
V_{IH}	Input HIGH Voltage		V_{CC} = 1.95V		1.4		V_{CC} + 0.2V	V
V_{IL}	Input LOW Voltage		V_{CC} = 1.65V		–0.5		0.4	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1	+1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS levels	V_{CC} = 1.95V			4	7	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels				1	2	mA
		I_{OUT} = 0 mA, f = 0 MHz, CMOS Levels				100	500	µA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC}–0.2V V_{IN} ≥ V_{CC}–0.2V or V_{IN} ≤ 0.2V, f = 0	V_{CC} = 1.95V	LL		1	8	µA

Capacitance[3]

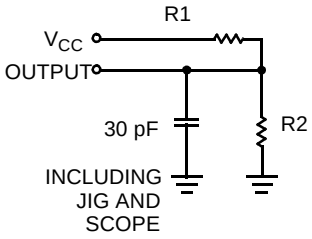
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC}= $V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

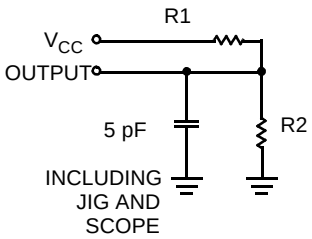
Description	Test Conditions	Symbol	BGA	Units
Thermal Resistance (Junction to Ambient)[3]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	55	°C/W
Thermal Resistance (Junction to Case)[3]		Θ_{JC}	16	°C/W

Note:
3. Tested initially and after any design or process changes that may affect these parameters.

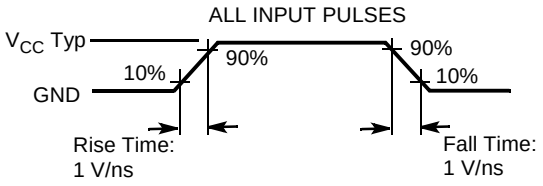
AC Test Loads and Waveforms



(a)

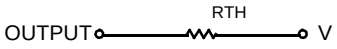


(b)



(c)

Equivalent to: THÉVENIN EQUIVALENT

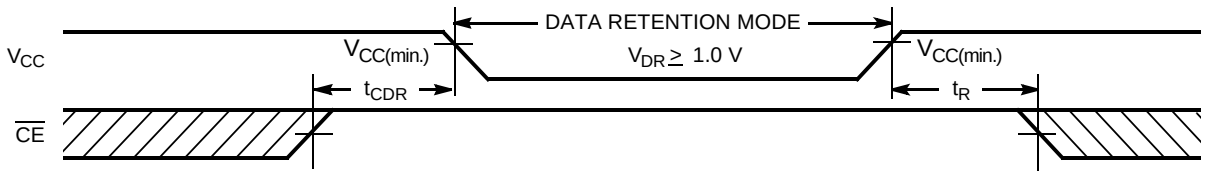


Parameters	1.8V	UNIT
R1	15294	Ohms
R2	11300	Ohms
R_{TH}	6500	Ohms
V_{TH}	0.85V	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[5]		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.0		1.95	V
I_{CCDR}	Data Retention Current	V_{CC} = 1.0V $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.3V$ No input may exceed V_{CC}+0.2V	LL		0.5	2	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0			ns
t_R[4]	Operation Recovery Time			t_{RC}			µs

Data Retention Waveform



Notes:

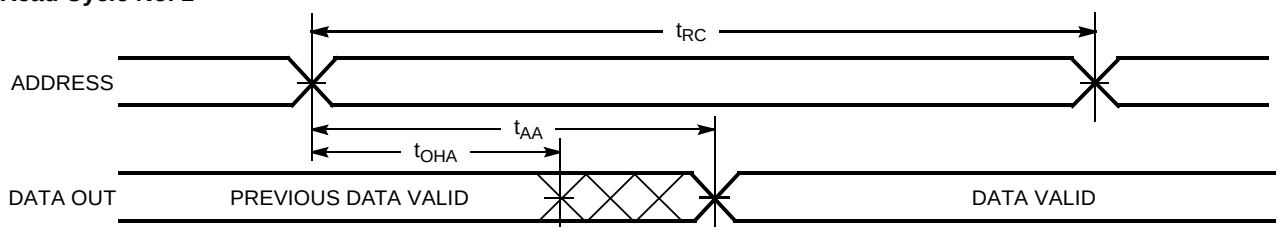
4. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.

Switching Characteristics Over the Operating Range[5]

Parameter	Description	55 ns		70 ns		Unit
				Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[6, 7]	5		5		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z[8]		20		25	ns
WRITE CYCLE[8, 9]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		60		ns
t_{AW}	Address Set-Up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	40		60		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	5		10		ns

Switching Waveforms

Read Cycle No. 1[10, 11]

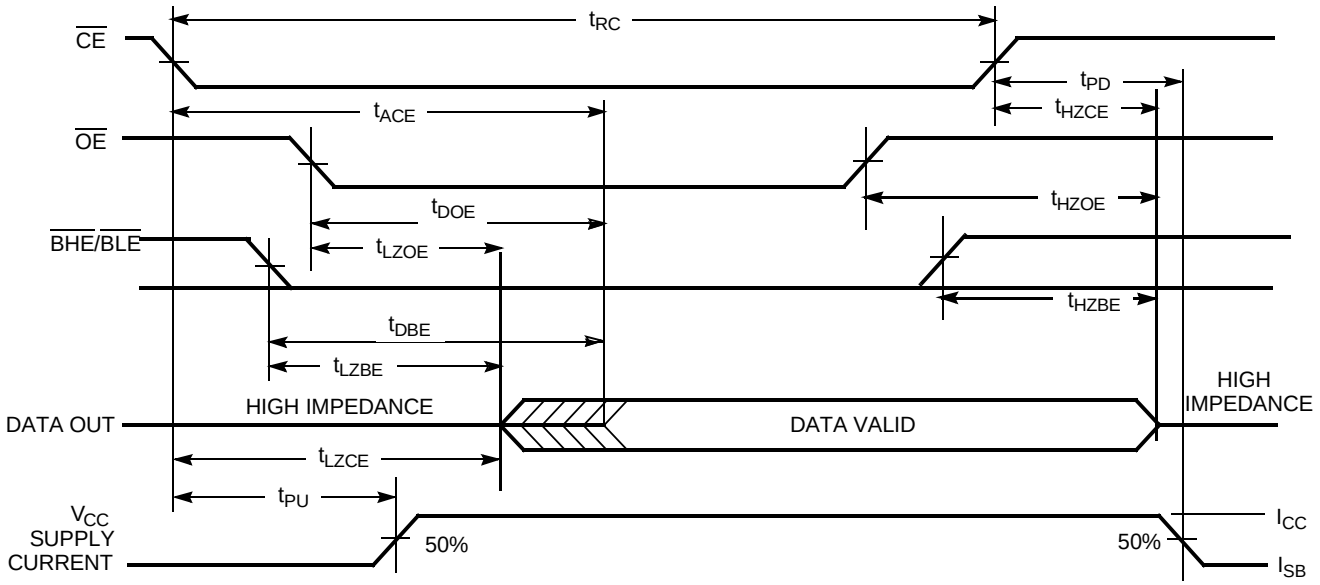


Notes:

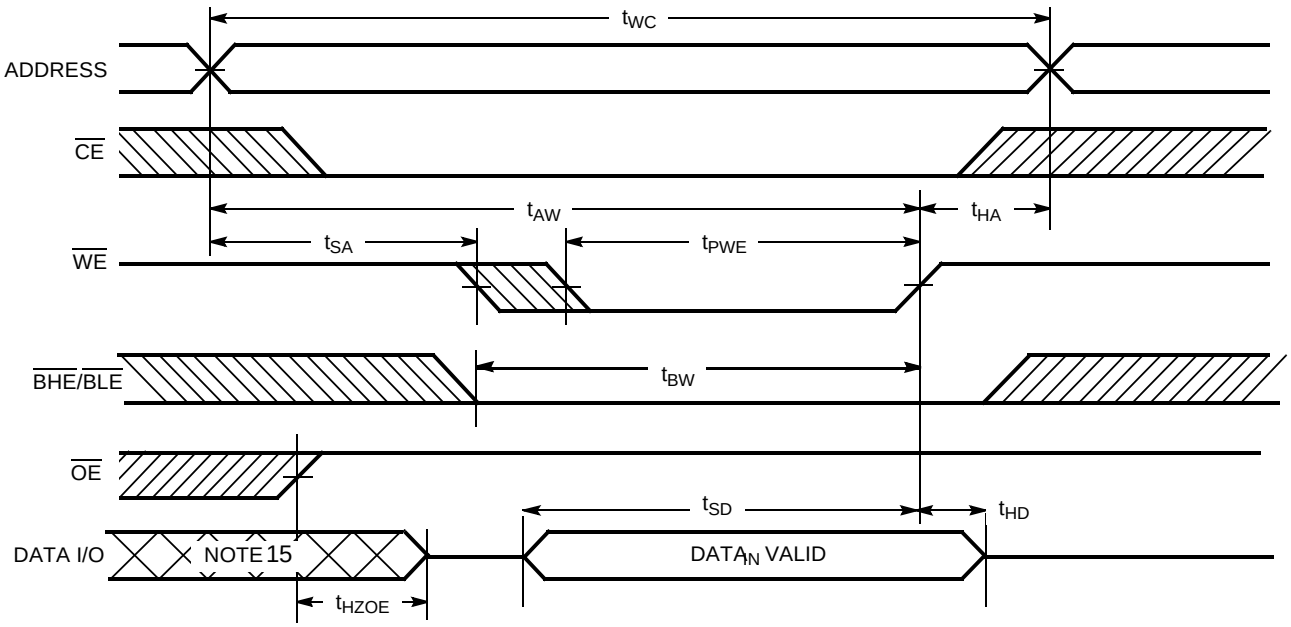
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±100 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.
10. Device is continuously selected. OE, CE = V_{IL}.
11. WE is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 [11, 12]



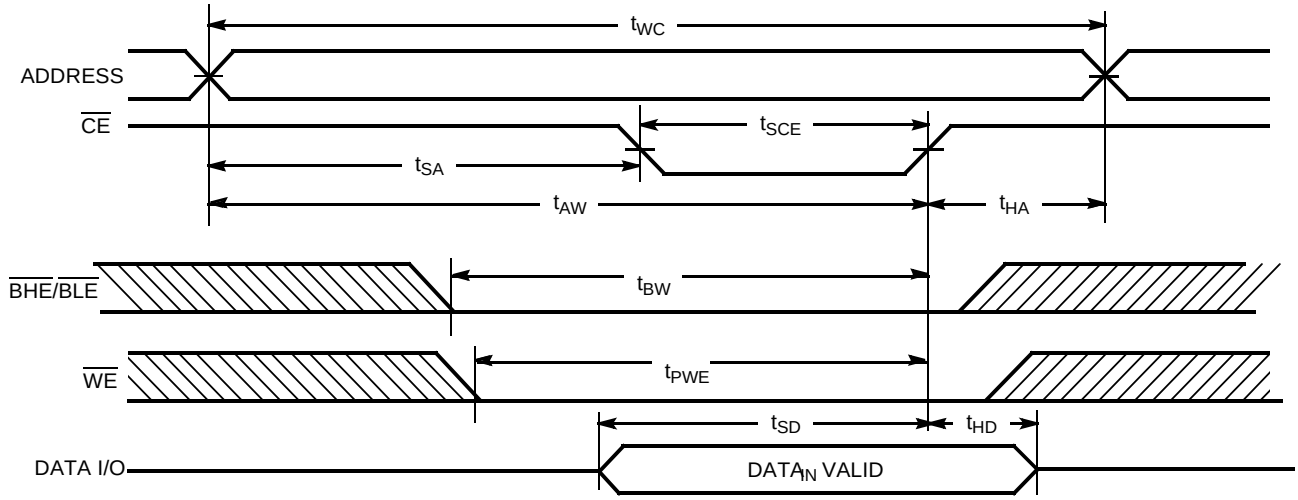
Write Cycle No. 1 (WE Controlled) [8, 13, 14]



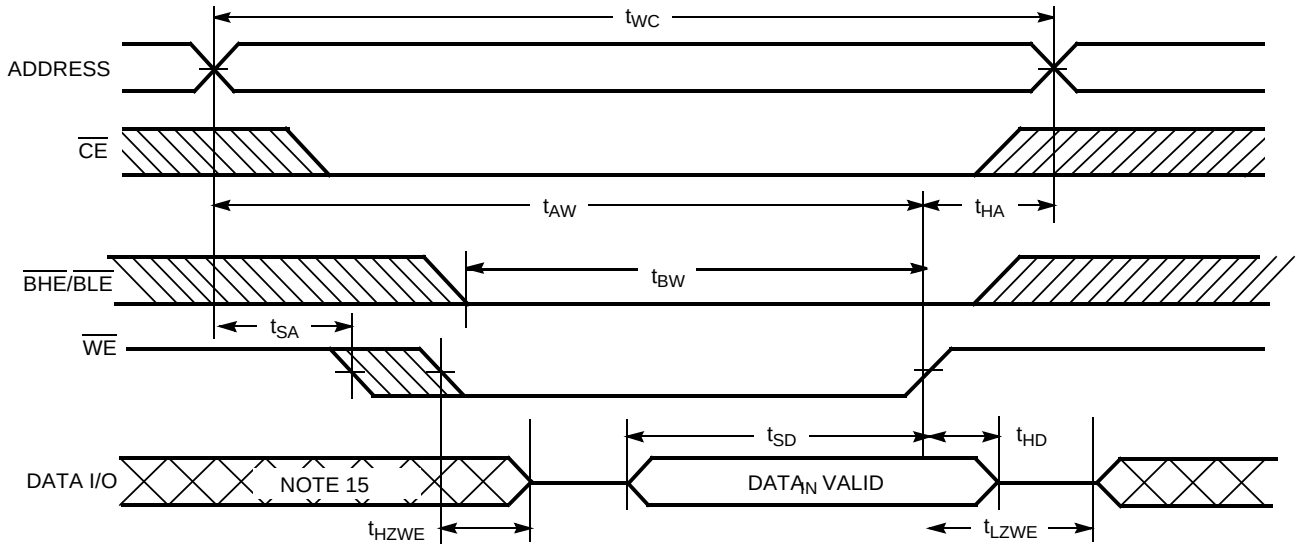
Notes:
12. Address valid prior to or coincident with CE transition LOW.
13. Data I/O is high impedance if OE = V_{IH}.
14. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 13, 14]

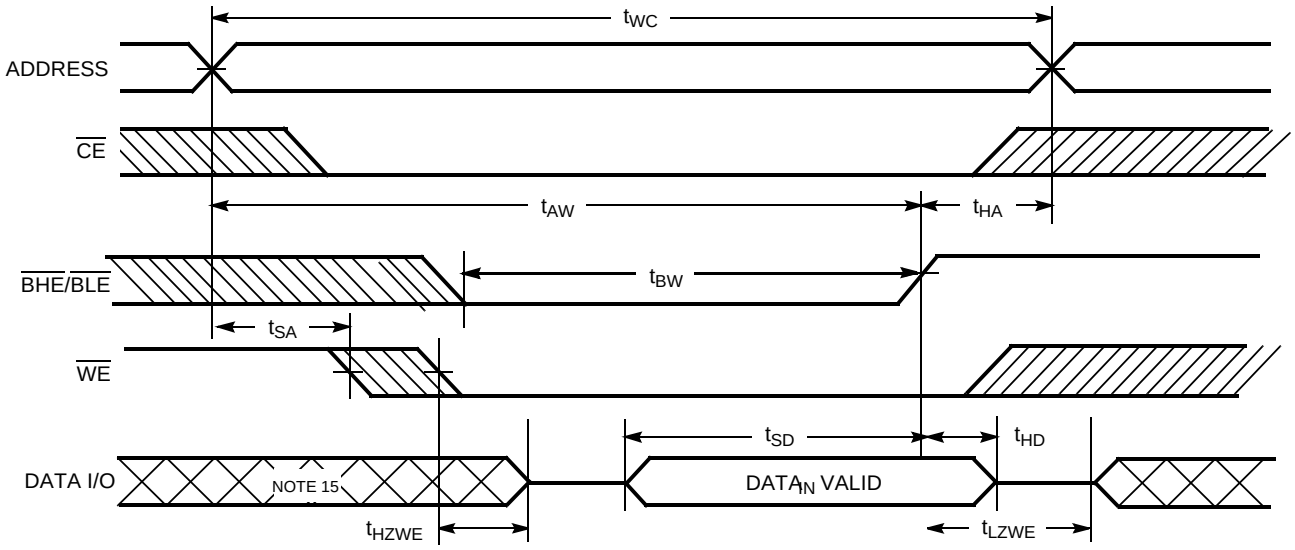


Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 14]



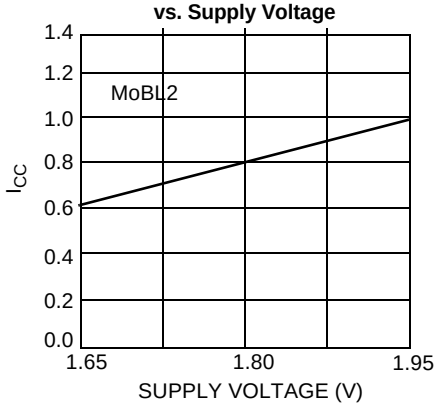
Switching Waveforms (continued)

Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)[15]

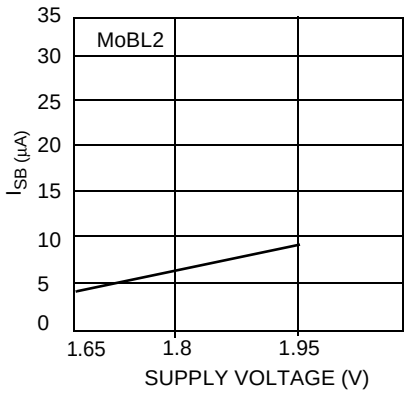


Typical DC and AC Characteristics

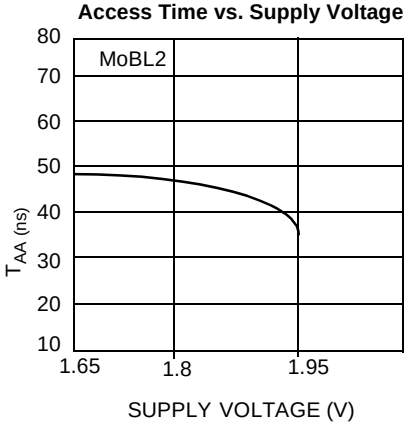
Normalized Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

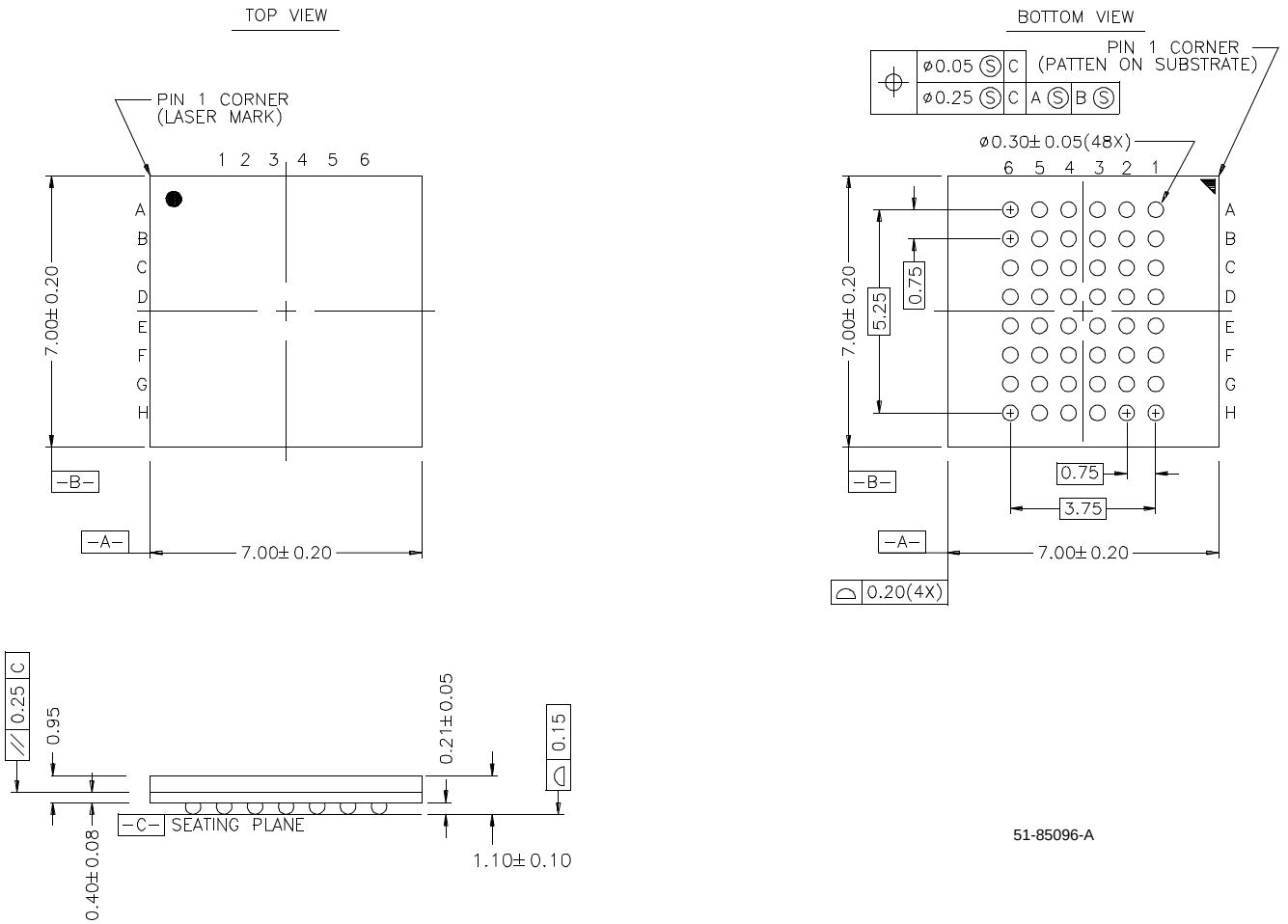
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0 –I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62137CV18LL-70BAI	BA48	48-Ball Fine Pitch BGA	Industrial
55	CY62137CV18LL-55BAI			

Package Diagrams

48-Ball (7.00 mm x 7.00 mm x 1.10 mm) Fine Pitch BGA BA48



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106265	05/07/01	HRT/MGN	New Data Sheet