



## 128K x 16 Static RAM

### Features

- **Low voltage range:**  
— CY62137V: 2.7V–3.6V
- **Ultra-low active, standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

### Functional Description

The CY62137V is a high-performance CMOS static RAM organized as 131,072 words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}$  HIGH) or when  $\overline{CE}$  is LOW and both BLE and BHE are HIGH. The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a

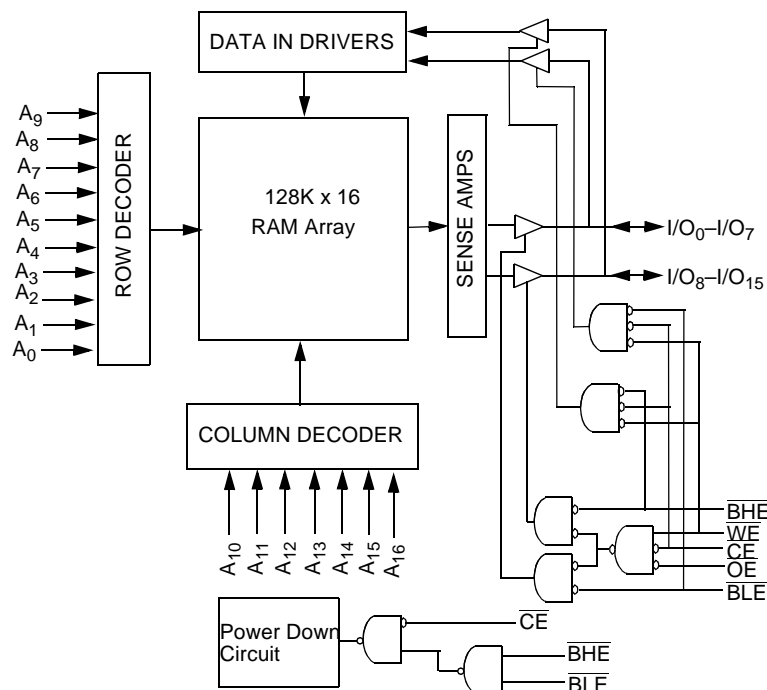
high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62137V is available in 48-ball FBGA and standard 44-pin TSOP Type II (forward pinout) packaging.

### Logic Block Diagram



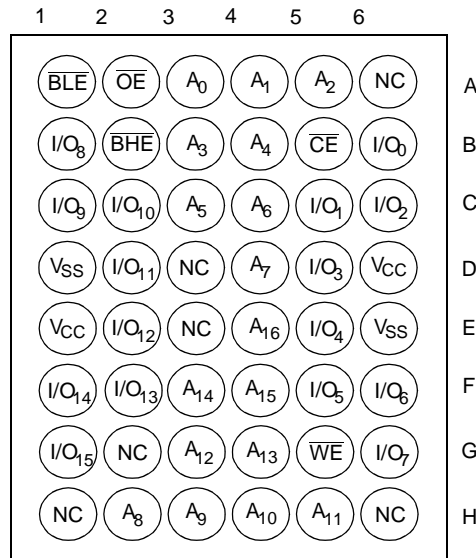
### Pin Configurations

#### TSOP II (Forward)

Top View			
A <sub>4</sub>	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	$\overline{OE}$
A <sub>0</sub>	5	40	BHE
$\overline{CE}$	6	39	BLE
I/O <sub>0</sub>	7	38	I/O <sub>15</sub>
I/O <sub>1</sub>	8	37	I/O <sub>14</sub>
I/O <sub>2</sub>	9	36	I/O <sub>13</sub>
I/O <sub>3</sub>	10	35	I/O <sub>12</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>4</sub>	13	32	I/O <sub>11</sub>
I/O <sub>5</sub>	14	31	I/O <sub>10</sub>
I/O <sub>6</sub>	15	30	I/O <sub>9</sub>
I/O <sub>7</sub>	16	29	I/O <sub>8</sub>
$\overline{WE}$	17	28	NC
A <sub>16</sub>	18	27	A <sub>8</sub>
A <sub>15</sub>	19	26	A <sub>9</sub>
A <sub>14</sub>	20	25	A <sub>10</sub>
A <sub>13</sub>	21	24	A <sub>11</sub>
A <sub>12</sub>	22	23	NC

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**Pin Configurations** (continued)

**48-Ball FBGA**
**Top View**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with  
Power Applied –55°C to +125°C

Supply Voltage to Ground Potential –0.5V to +4.6V

DC Voltage Applied to Outputs  
in High Z State<sup>[1]</sup> –0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> –0.5V to V<sub>CC</sub> + 0.5V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

**Operating Range**

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62137V	Industrial	–40°C to +85°C	2.7V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Power	Power Dissipation (Industrial)			
					Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[2]</sup>	V <sub>CC(max.)</sub>		Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.
CY62137V	2.7V	3.0V	3.6V	LL	7 mA	15 mA	1 μA	15 μA

**Notes:**

- V<sub>IL</sub>(min.) = –2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC Typ.</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions			CY62137V			Unit	
					Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = −1.0 mA	V <sub>CC</sub> = 2.7V		2.4			V	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V				0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> = 3.6V		2.2		V <sub>CC</sub> + 0.5V	V	
V <sub>IL</sub>	Input LOW Voltage		V <sub>CC</sub> = 2.7V		−0.5		0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>			−1	±1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled			−1	±1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = 3.6V			7	15	mA	
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels				1	2	mA	
I <sub>SB1</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>MAX</sub>		V <sub>CC</sub> = 3.6V			100	μA	
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		V <sub>CC</sub> = 3.6V	LL		1	15	μA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

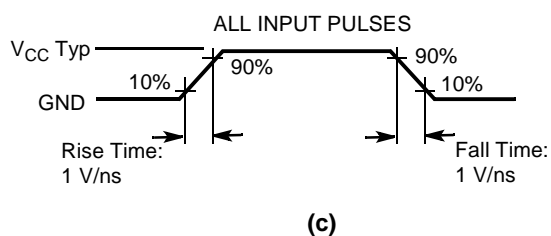
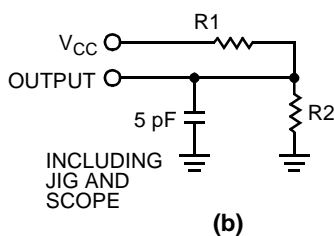
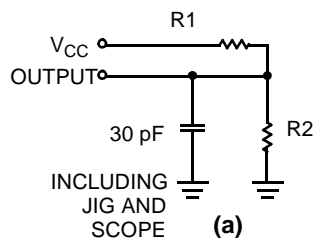
**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	TSOPII	Unit
Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	60	°C/W
Thermal Resistance (Junction to Case) <sup>[3]</sup>		Θ <sub>JC</sub>	16	22	°C/W

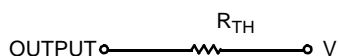
**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

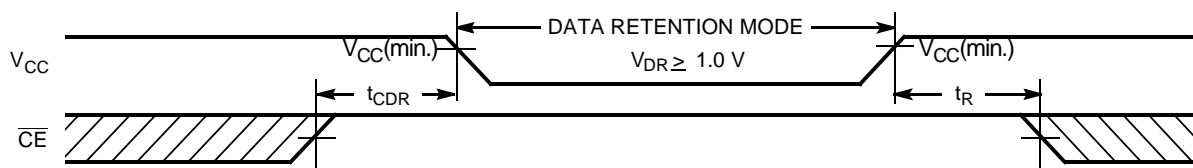


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.75V	Volts

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions <sup>[4]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.0		3.6	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V No input may exceed V <sub>CC</sub> + 0.3V	LL	0.5	7.5	μA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub>	Operation Recovery Time		70			ns

## Data Retention Waveform



### Note:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to V<sub>CC</sub> typ., and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.

**Switching Characteristics** Over the Operating Range<sup>[4]</sup>

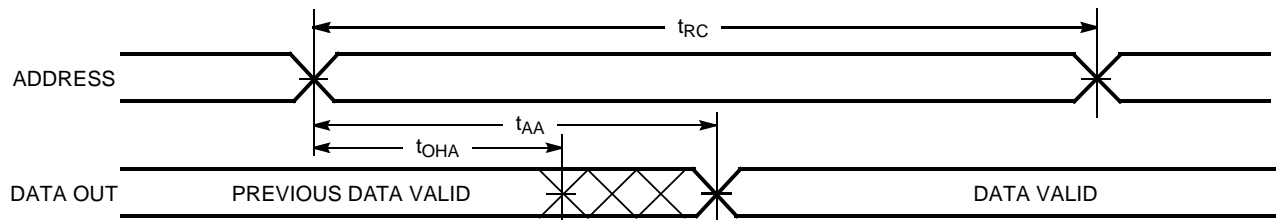
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[5]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[5]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		25		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t <sub>DBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub> <sup>(7)</sup>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z	5		5		ns
t <sub>HZBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z		25		25	ns
WRITE CYCLE <sup>[8, 9]</sup>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		50		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[5]</sup>	5		10		ns
t <sub>BW</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to End of Write	50		60		ns

**Notes:**

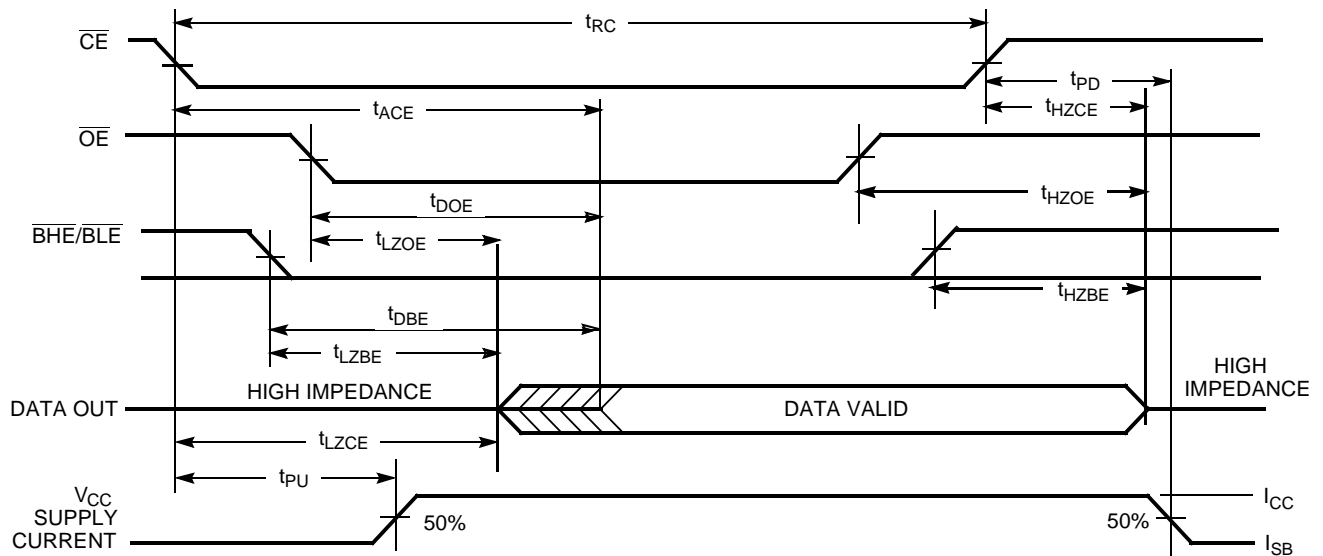
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- If both byte enables are toggled together this value is 10 ns.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

### Read Cycle No. 1<sup>[10, 11]</sup>

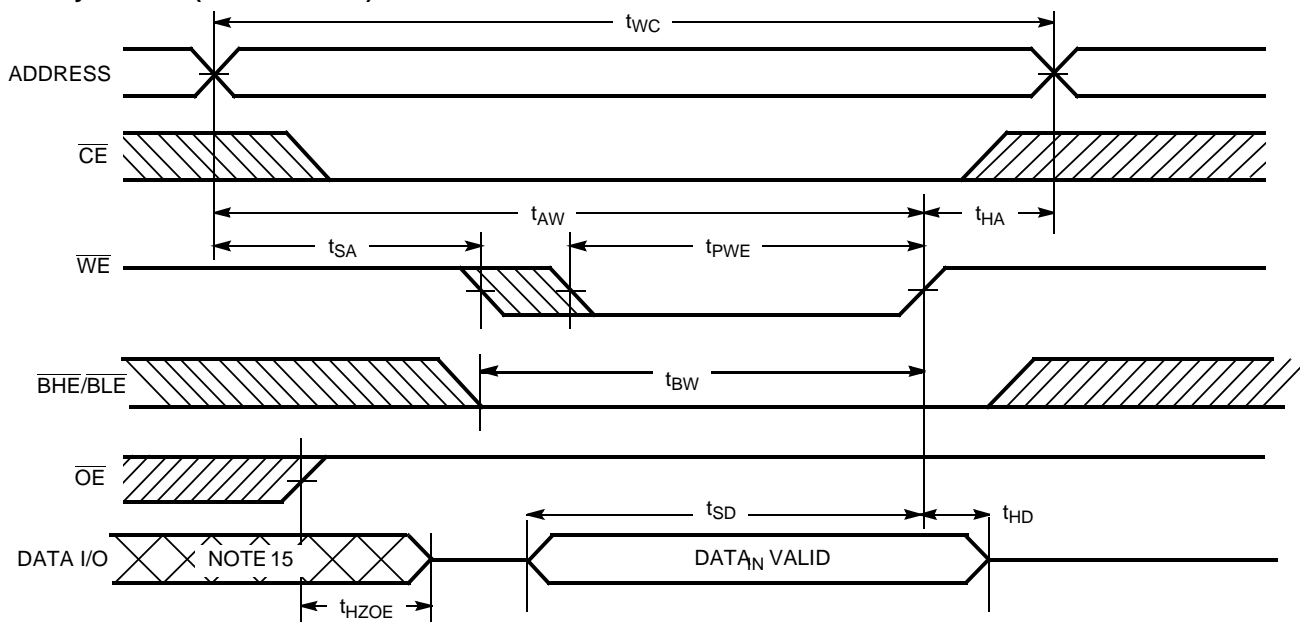
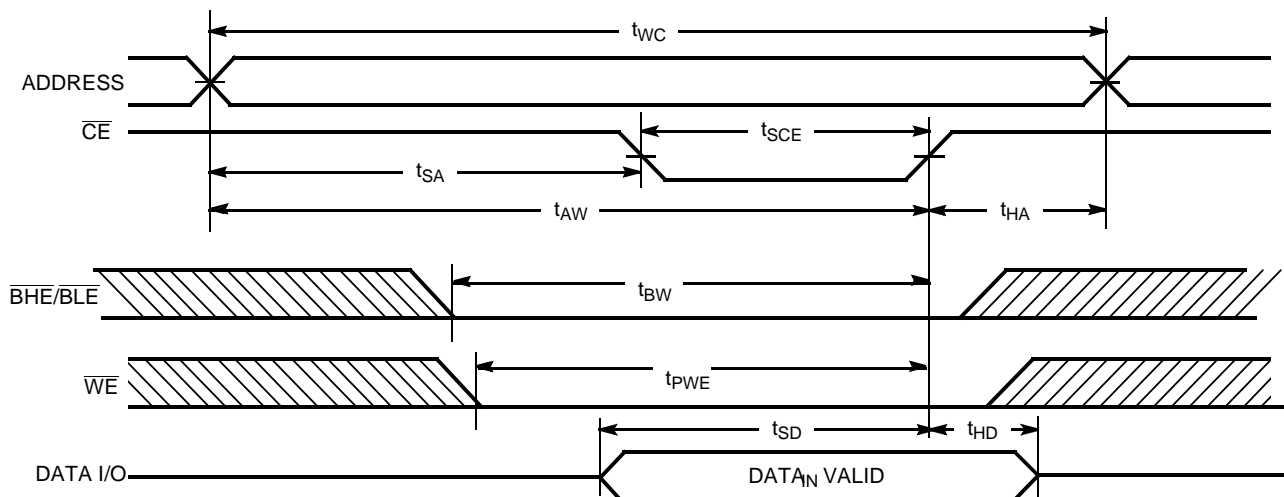


### Read Cycle No. 2<sup>[11, 12]</sup>

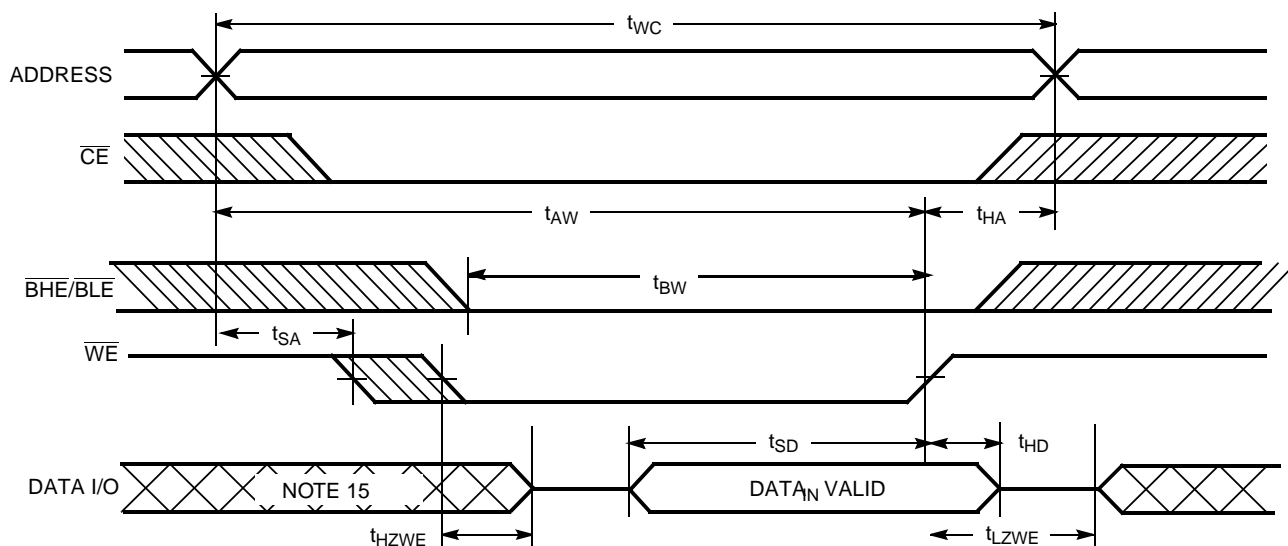
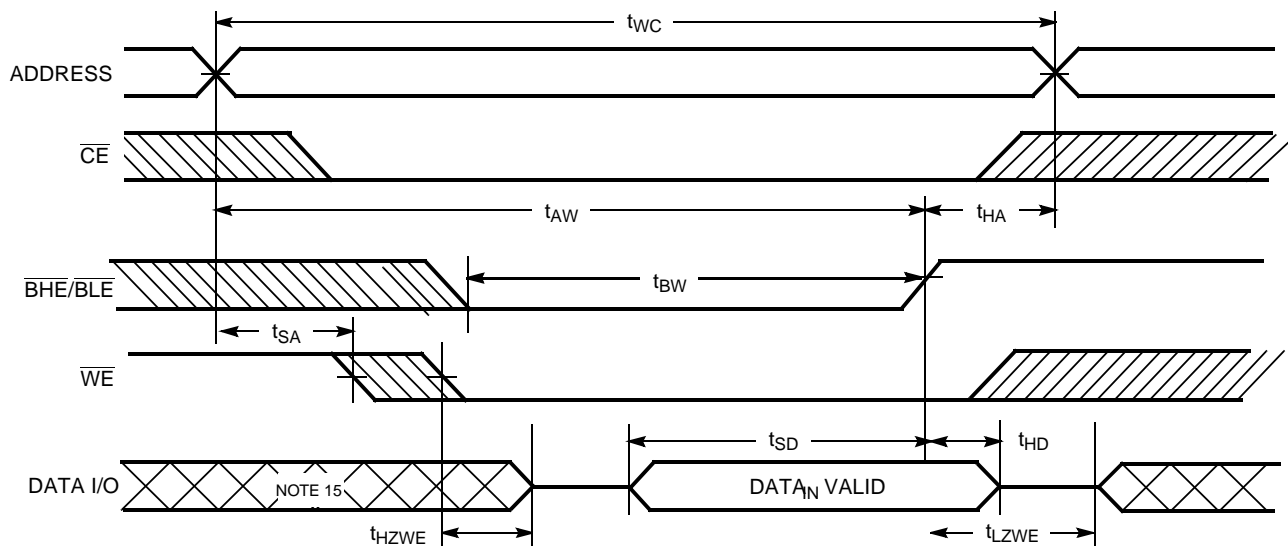


#### Notes:

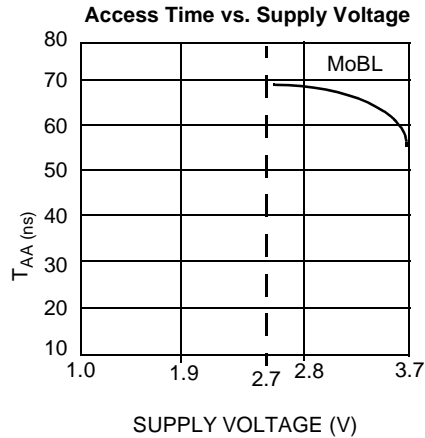
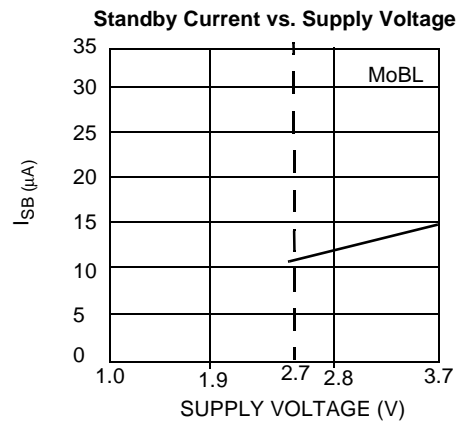
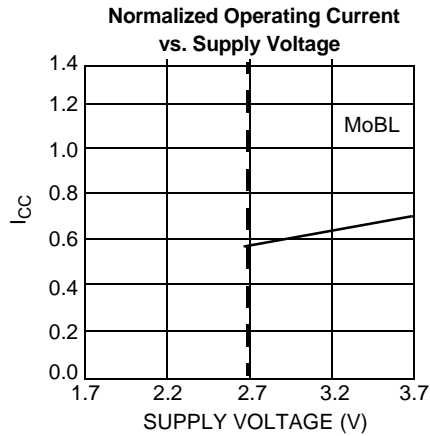
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}=V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)** <sup>[8, 13, 14]</sup>

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** <sup>[8, 13, 14]</sup>

**Notes:**

13. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[9, 14]</sup>**

**Write Cycle No. 4 (BHE/BL $\overline{\text{E}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[15]</sup>**


## Typical DC and AC Characteristics



## Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )



Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62137VLL-55ZI	Z44	44-Pin TSOP II	Industrial
	CY62137VLL-55BAI	BA48	48-Ball Fine Pitch BGA	
70	CY62137VLL-70ZI	Z44	44-Pin TSOP II	Industrial
	CY62137VLL-70BAI	BA48	48-Ball Fine Pitch BGA	

## Package Diagrams

**TOP VIEW**

PIN 1 CORNER  
(LASER MARK)

A B C D E F G H

1 2 3 4 5 6

7.00±0.20

A

B

7.00±0.20

**BOTTOM VIEW**

PIN 1 CORNER

⊕ ⌀0.05 (M) C

⊕ ⌀0.25 (M) C A B

⌀0.30±0.05(48X)

6 5 4 3 2 1

A B C D E F G H

7.00±0.20

A

5.25

0.75

2.625

1.875

0.75

3.75

B

7.00±0.20

C

0.15(4X)

**SIDE CROSS SECTION**

SEATING PLANE

0.25

0.95

0.21±0.05

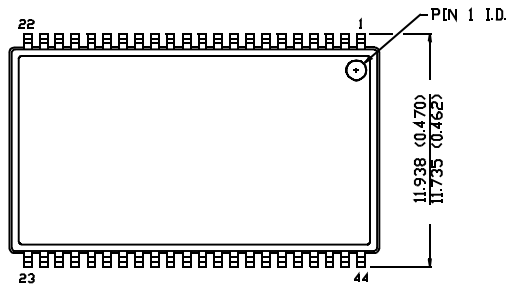
1.20 MAX.

0.10

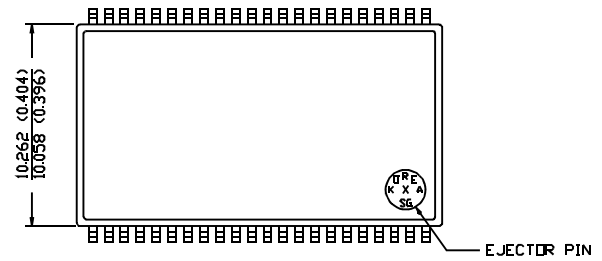
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**Package Diagrams (continued)**
**44-Pin TSOP II Z44**

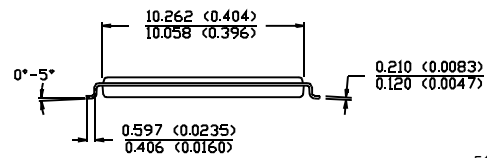
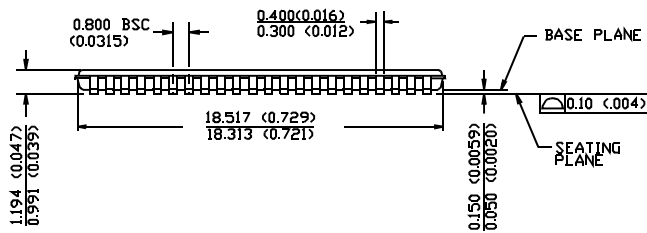
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



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