



PRELIMINARY

CY62143BV MoBL™

256K x 16 Static RAM

Features

- **Low voltage range:**
— CY62143BV: 2.7V–3.6V
- **Ultra-low active, standby power**
- **Automatic power-down when deselected**
- **TTL Compatible inputs and outputs**
- **CMOS for optimum speed/power**
- **Extra Active High Chip Select (CE₂)**

Functional Description

The CY62143BV is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode when deselected (CE₁ HIGH or CE₂ LOW). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state if one of

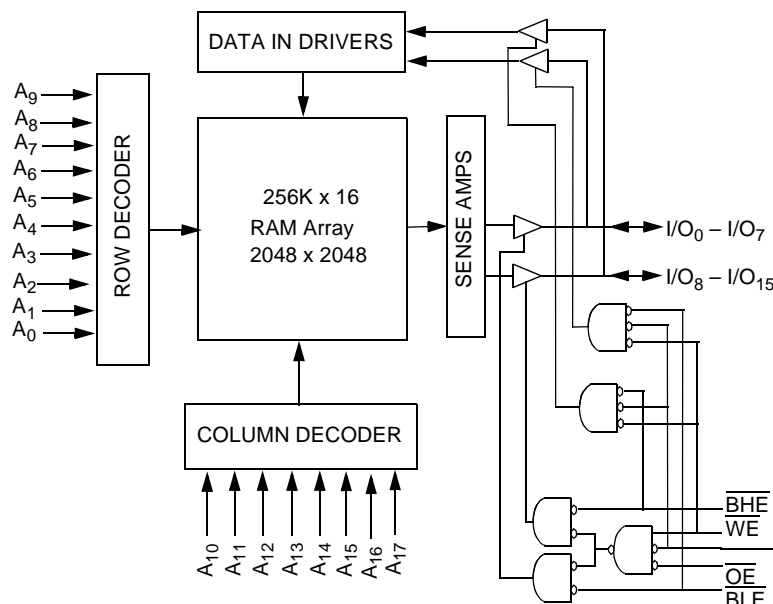
the following conditions occur: when deselected ($\overline{\text{CE}}_1$ HIGH or CE₂ LOW) or if outputs are disabled ($\overline{\text{OE}}$ HIGH) or if BHE and BLE are disabled, (BHE, BLE HIGH) or if during a write operation (CE₁ LOW and CE₂ HIGH, and WE LOW).

Writing to this device is accomplished by Chip Enable $\overline{\text{CE}}_1$ LOW and CE₂ HIGH and taking Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable (CE₁ LOW and CE₂ HIGH) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

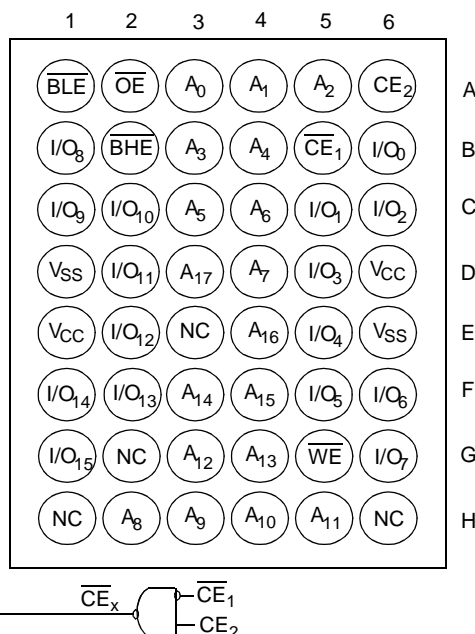
The CY62143BV is available in a 48-ball FBGA package.

Logic Block Diagram



Pin Configurations

FBGA (Top View)



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with
Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential -0.5V to $+4.6\text{V}$

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{\text{CC}} + 0.5\text{V}$

DC Input Voltage^[1] -0.5V to $V_{\text{CC}} + 0.5\text{V}$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>2100\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62143BV	Industrial	-40°C to $+85^{\circ}\text{C}$	2.7V to 3.6V

Product Portfolio

Product	V_{CC} Range			Power	Power Dissipation (Industrial)			
					Operating (I_{CC})		Standby (I_{SB2})	
	$V_{\text{CC(min.)}}$	$V_{\text{CC(typ.)}}^{[2]}$	$V_{\text{CC(max.)}}$		Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62143BV	2.7V	3.0V	3.6V	LL	7 mA	15 mA	2 μA	20 μA

Notes:

- $V_{\text{IL(min.)}} = -2.0\text{V}$ for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{\text{CC}} = V_{\text{CC(typ.)}}$, $T_{\text{A}} = 25^{\circ}\text{C}$.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62143BV			Unit
			Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA, V _{CC} = 2.7V	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA, V _{CC} = 2.7V			0.4	V
V _{IH}	Input HIGH Voltage	V _{CC} = 3.6V	2.2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage	V _{CC} = 2.7V	-0.5		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	±1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1	+1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS Levels		7	15	mA
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels		1	2	mA
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0		2	20	μA
		$\overline{CE}_2 \leq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0				
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0, V _{CC} = 3.6V, LL				
		$\overline{CE}_2 \leq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0, V _{CC} = 3.6V, LL				

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ.)}	6	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance

Description	Test Conditions	Symbol	BGA	TSOPII	Units
Thermal Resistance (Junction to Ambient) ^[3]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ _{JA}	55	60	°C/W
Thermal Resistance (Junction to Case) ^[3]		Θ _{JC}	16	22	°C/W

Note:

3. Tested initially and after any design or process changes that may affect these parameters.

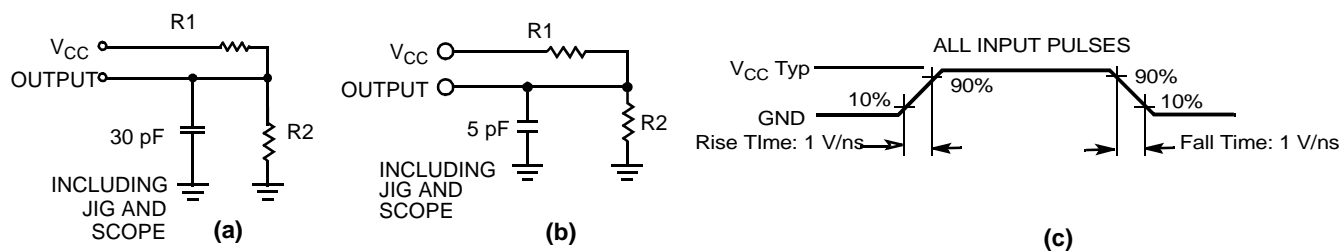
Switching Characteristics Over the Operating Range^[4]

Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE}_x LOW to Data Valid		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[5, 7]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[7]		25	ns
t _{LZCE}	\overline{CE}_x LOW to Low Z ^[5]	10		ns
t _{HZCE}	\overline{CE}_x HIGH to High Z ^[5, 7]		25	ns
t _{PU}	\overline{CE}_x LOW to Power-Up	0		ns
t _{PD}	\overline{CE}_x HIGH to Power-Down		70	ns
t _{DBE}	\overline{BHE} / \overline{BLE} LOW to Data Valid		70	ns
t _{LZBE} ^[6]	\overline{BHE} / \overline{BLE} LOW to Low Z	5		ns
t _{HZBE}	\overline{BHE} / \overline{BLE} HIGH to High Z		25	ns
WRITE CYCLE ^[8, 9]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	\overline{CE}_x LOW to Write End	60		ns
t _{AW}	Address Set-Up to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	50		ns
t _{BW}	\overline{BHE} / \overline{BLE} Pulse Width	60		ns
t _{SD}	Data Set-Up to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[5, 7]		25	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[5]	10		ns

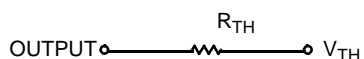
Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- If both byte enables are toggled together this value is 10ns
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE}_x LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

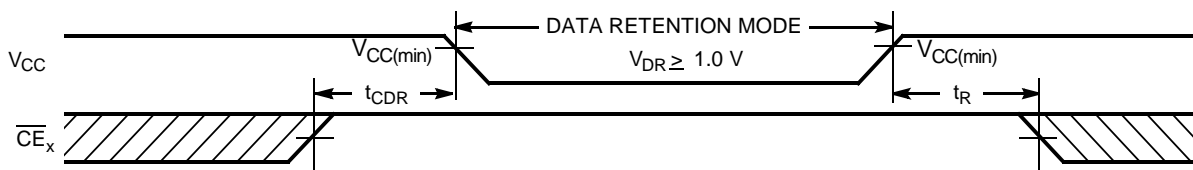


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75V	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention			1.0		3.6	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.0V CE ₁ ≥ V _{CC} − 0.3V, CE ₂ ≤ 0.3V V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V No input may exceed V _{CC} + 0.3V	LL		1	10	μA
t _{CDR} ^[10]	Chip Deselect to Data Retention Time			0			ns
t _R ^[11]	Operation Recovery Time			70			ns

Data Retention Waveform

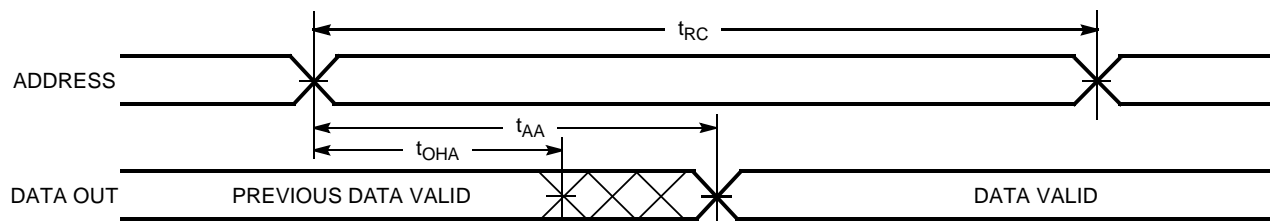


Note:

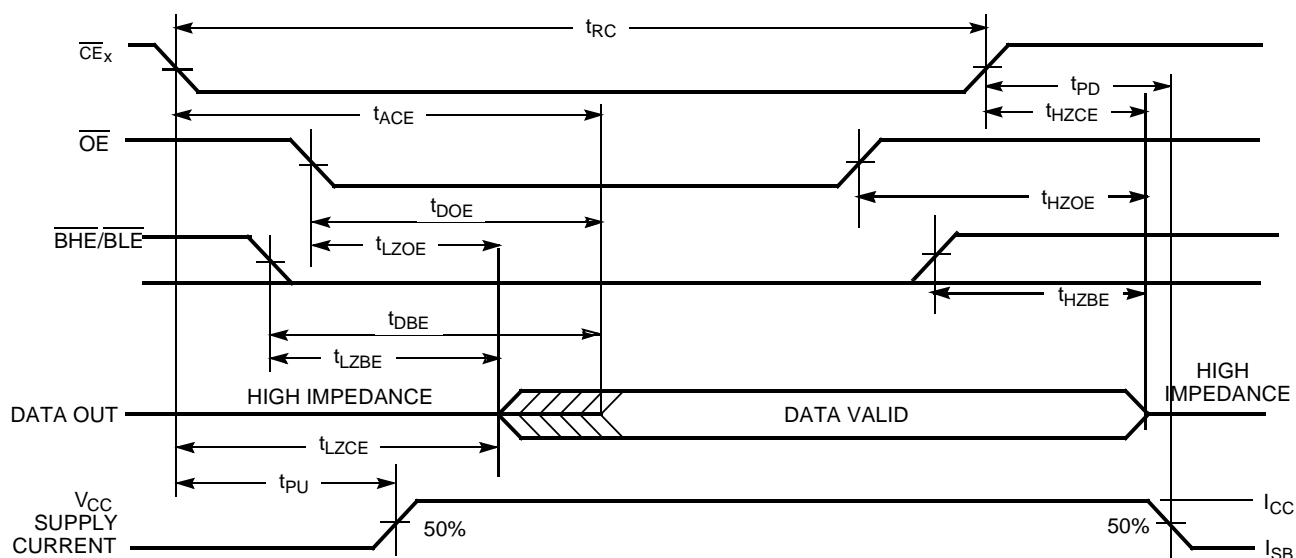
10. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 10 \mu s$ or stable at $V_{CC(min.)} > 10 \mu s$.
11. \overline{CE}_x is the combinatorial output of \overline{CE}_1 and \overline{CE}_2 .

Switching Waveforms

Read Cycle No. 1 ^[12, 13]

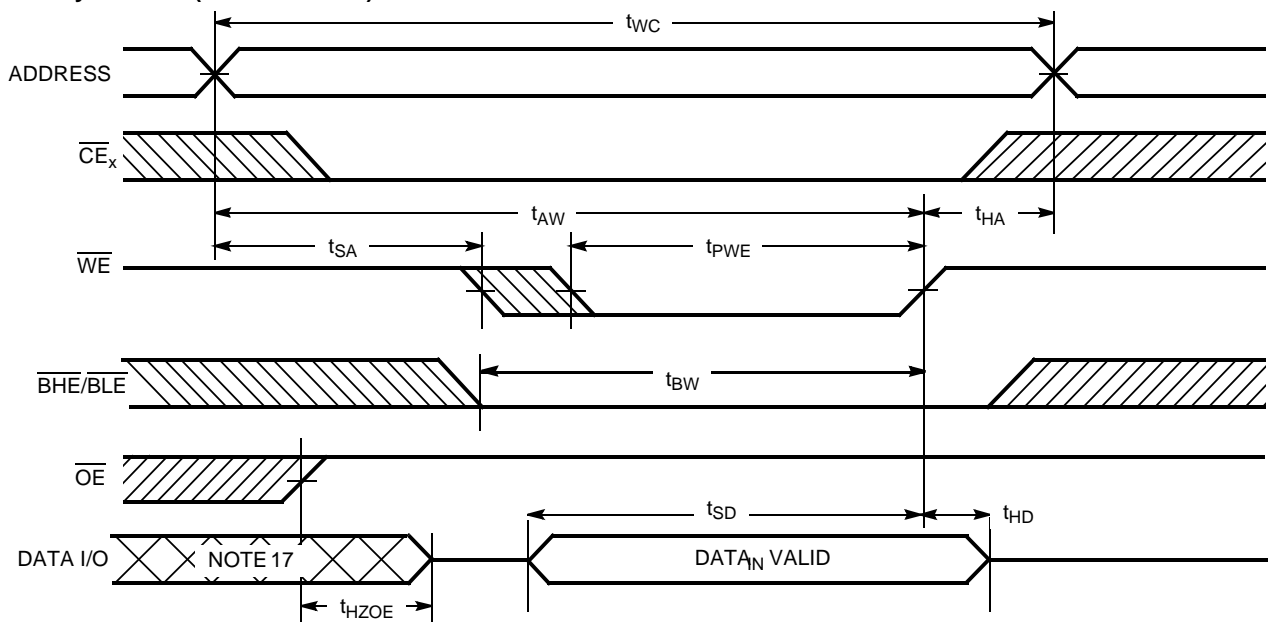
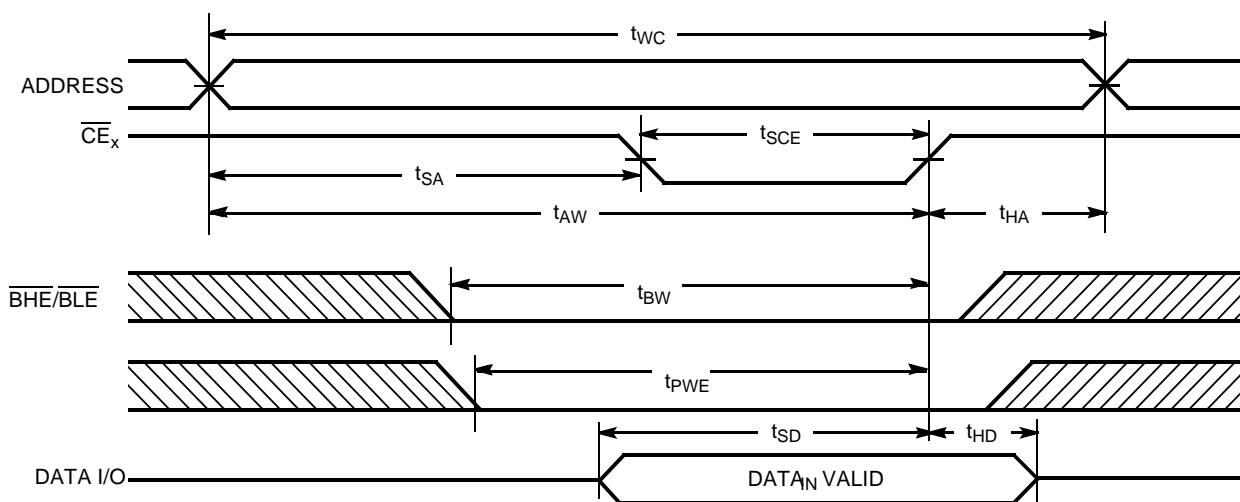


Read Cycle No. 2 ^[13, 14]

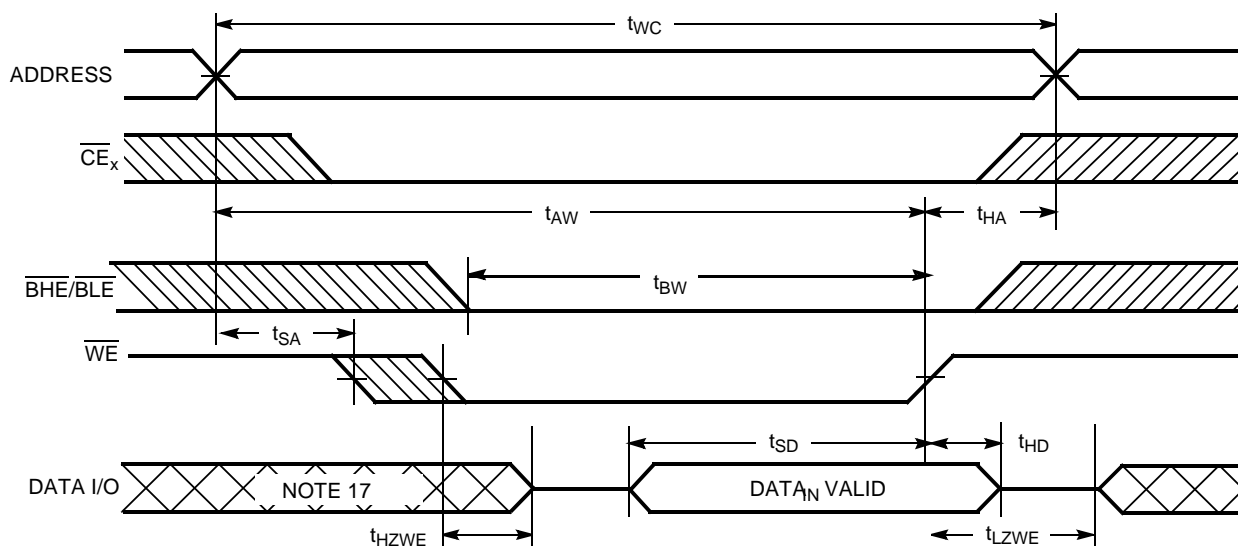
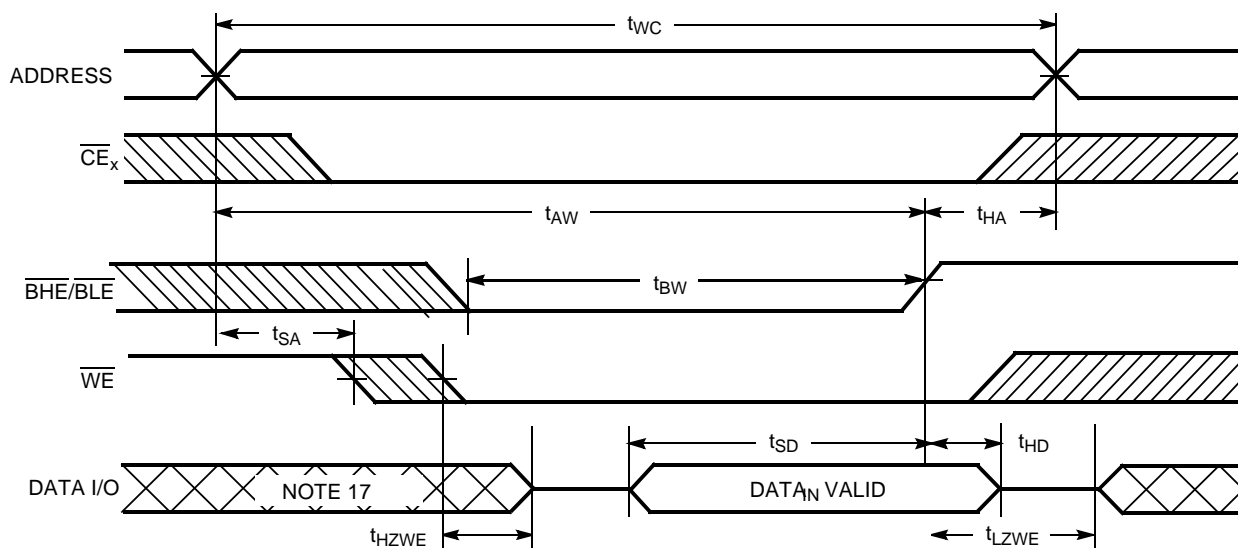


Notes:

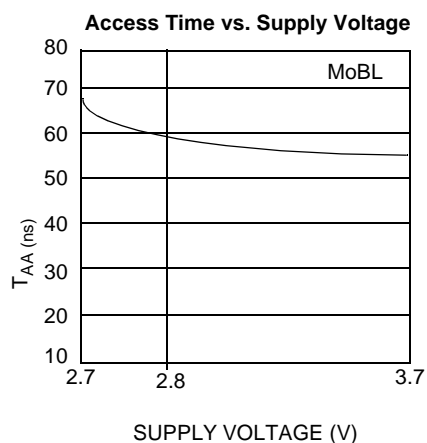
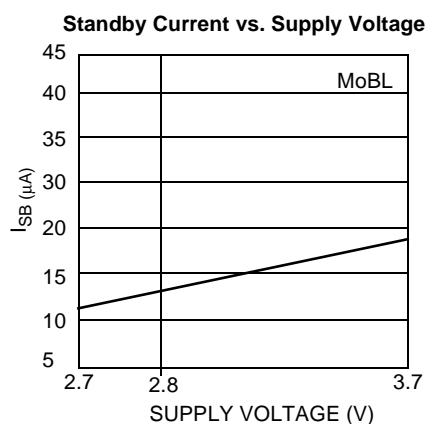
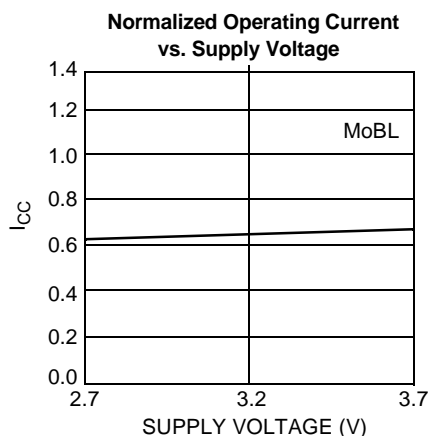
12. Device is continuously selected. \overline{OE} , $\overline{CE}_x = V_{IL}$.
13. \overline{WE} is HIGH for read cycle.
14. Address valid prior to or coincident with \overline{CE}_x transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (WE Controlled) [8, 15, 16]

Write Cycle No. 2 (\overline{CE} Controlled) [8, 15, 16]

Notes:

15. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
16. If \overline{CE}_x goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[9, 16]

Write Cycle No. 4 ($\overline{\text{BHE/BL0}}$ Controlled, $\overline{\text{OE}}$ LOW)^[17]


Typical DC and AC Characteristics



Truth Table

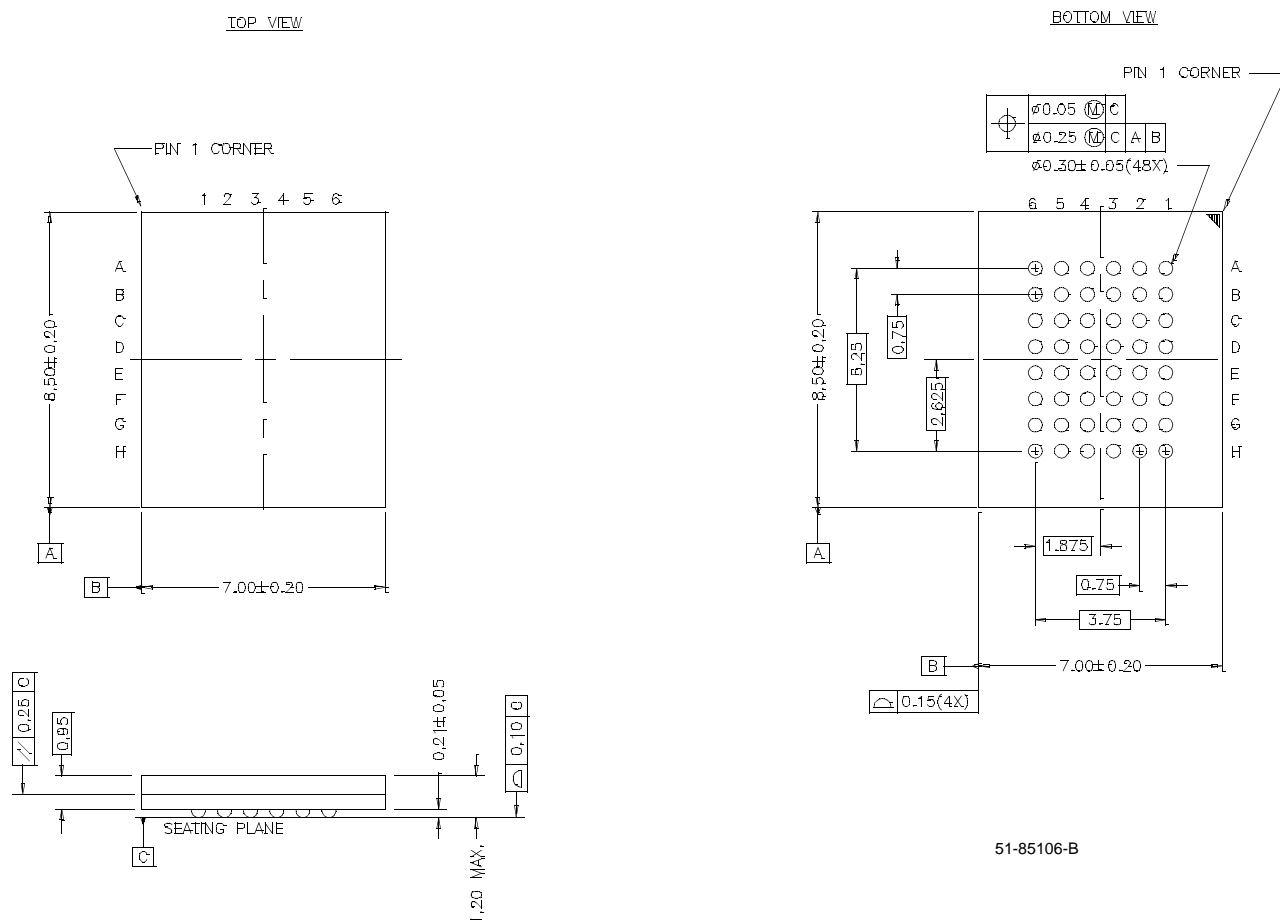
\overline{CE}_2	\overline{CE}_1	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
X	H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
H	L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
H	L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
H	L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
H	L	H	H	L	L	High Z	Deselect/Output Disabled	Active (I_{CC})
H	L	H	H	H	L	High Z	Deselect/Output Disabled	Active (I_{CC})
H	L	H	H	L	H	High Z	Deselect/Output Disabled	Active (I_{CC})
H	L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
H	L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
H	L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})
L	X	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62143BVLL-70BAI	BA48B	48-Ball Fine Pitch BGA	Industrial

Package Diagrams

48-Ball (7.00 mm x 8.50 mm x 1.20 mm) Fine Pitch BGA BA48B





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Document Title: CY62143BV MoBL 256K x 16 Static RAM Document Number: 38-05042				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106989	06/14/01	MGN	New Data Sheet