



PRELIMINARY

CY62147CV18 MoBL2™

## 256K x 16 Static RAM

### Features

- Low voltage range:  
— CY62147CV18: 1.65V–1.95V
- Pin Compatible w/ CY6147V18/BV18
- Ultra-low active, standby power
- Easy memory expansion with CE and OE features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power

### Functional Description

The CY62147CV18 is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (CE HIGH) or when CE is LOW and both BLE and

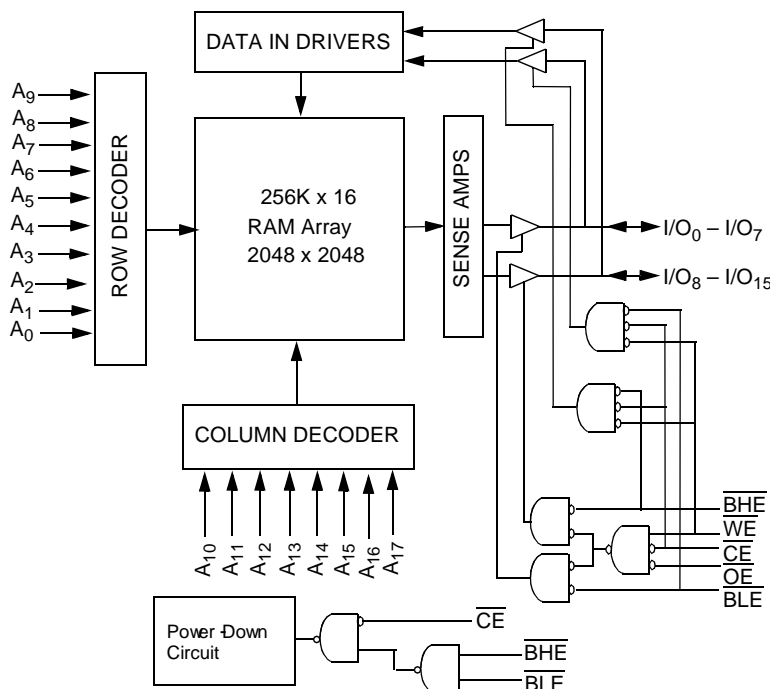
BHE are HIGH. The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled (OE HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

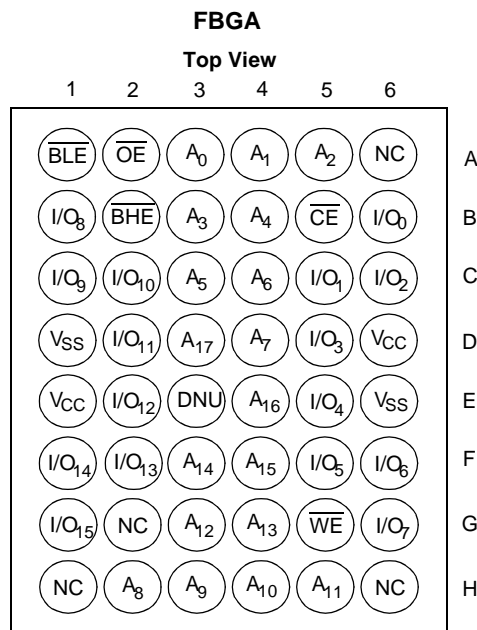
The CY62147CV18 is available in a 48-ball FBGA packaging.

### Logic Block Diagram



MoBL, MoBL2 and More Battery Life are trademarks of Cypress Semiconductor Corporation.

## Pin Configuration



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with  
Power Applied –55°C to +125°C

Supply Voltage to Ground Potential –0.5V to +2.4V

DC Voltage Applied to Outputs

in High Z State<sup>[1]</sup> –0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> –0.5V to V<sub>CC</sub> + 0.5V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62147CV18	Industrial	–40°C to +85°C	1.65V to 1.95V

## Product Portfolio

Product	V <sub>CC</sub> Range			Power	Power Dissipation (Industrial)			
					Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[2]</sup>	V <sub>CC(max.)</sub>		Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62147CV18	1.65V	1.8V	1.95V	Std.	4 mA	7 mA	1 µA	10 µA

### Notes:

- V<sub>IL(min.)</sub> = –2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62147CV18			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = 1.65V	1.5			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 1.65V			0.2	V
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> = 1.95V	1.4		V <sub>CC</sub> + 0.2V	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>CC</sub> = 1.65V	-0.5		0.4	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	±1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1	+1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = 1.95V		4	7	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels			1	5	mA
		I <sub>OUT</sub> = 0 mA, f = 0 Hz, CMOS Levels			100	500	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0$	V <sub>CC</sub> = 1.95V	Std.	1	10	μA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ.)	8	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

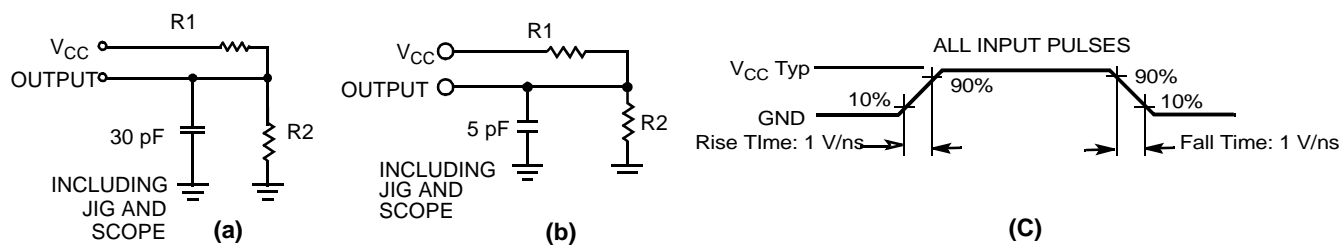
**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance (Junction to Case) <sup>[3]</sup>		Θ <sub>JC</sub>	16	°C/W

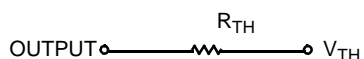
**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

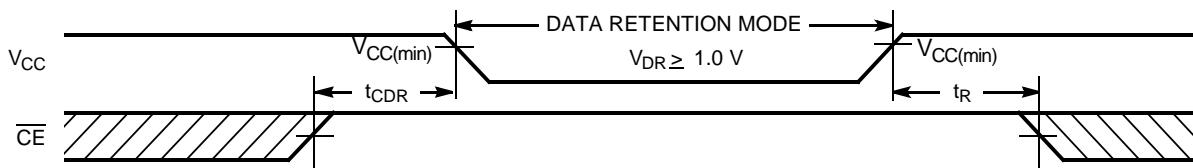


Parameters	1.8V	Unit
R1	25K	$\Omega$
R2	25K	$\Omega$
$R_{TH}$	12.5K	$\Omega$
$V_{TH}$	0.90V	V

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0		1.95	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V$ $CE \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ No input may exceed $V_{CC} + 0.2V$	Std.	1	10	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[4]}$	Operation Recovery Time		$t_{RC}$			ns

## Data Retention Waveform



### Note:

- Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} > 10 \mu s$  or stable at  $V_{CC(min.)} > 10 \mu s$ .

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

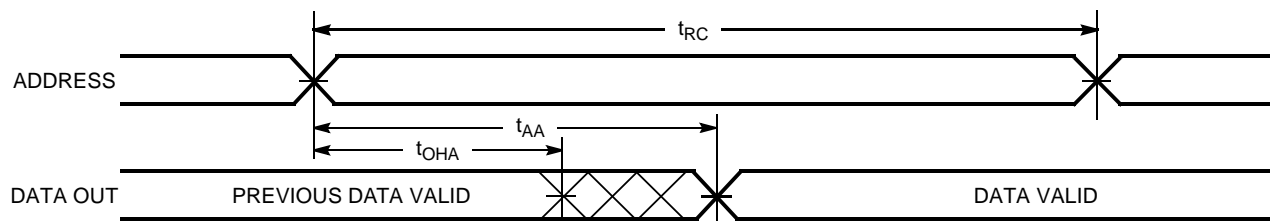
Parameter	Description	55ns		70ns		Unit
		Min.	Max	Min	Max.	
READ CYCLE						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	0		0		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6, 7]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	5		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t <sub>DBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		30		45	ns
t <sub>LZBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z	5		5		ns
t <sub>HZBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z		20		25	ns
WRITE CYCLE <sup>[8, 9]</sup>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	40		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	40		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		50		ns
t <sub>BW</sub>	$\overline{BHE}$ / $\overline{BLE}$ Pulse Width					ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		15		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	5		10		ns

**Notes:**

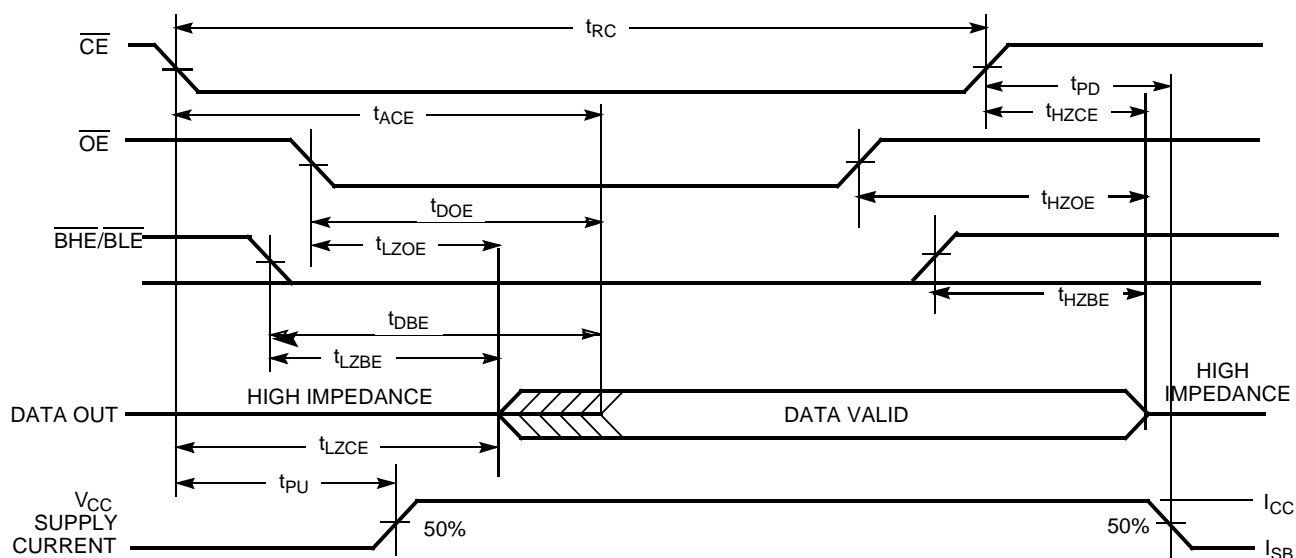
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

**Read Cycle No. 1** <sup>[10, 11]</sup>

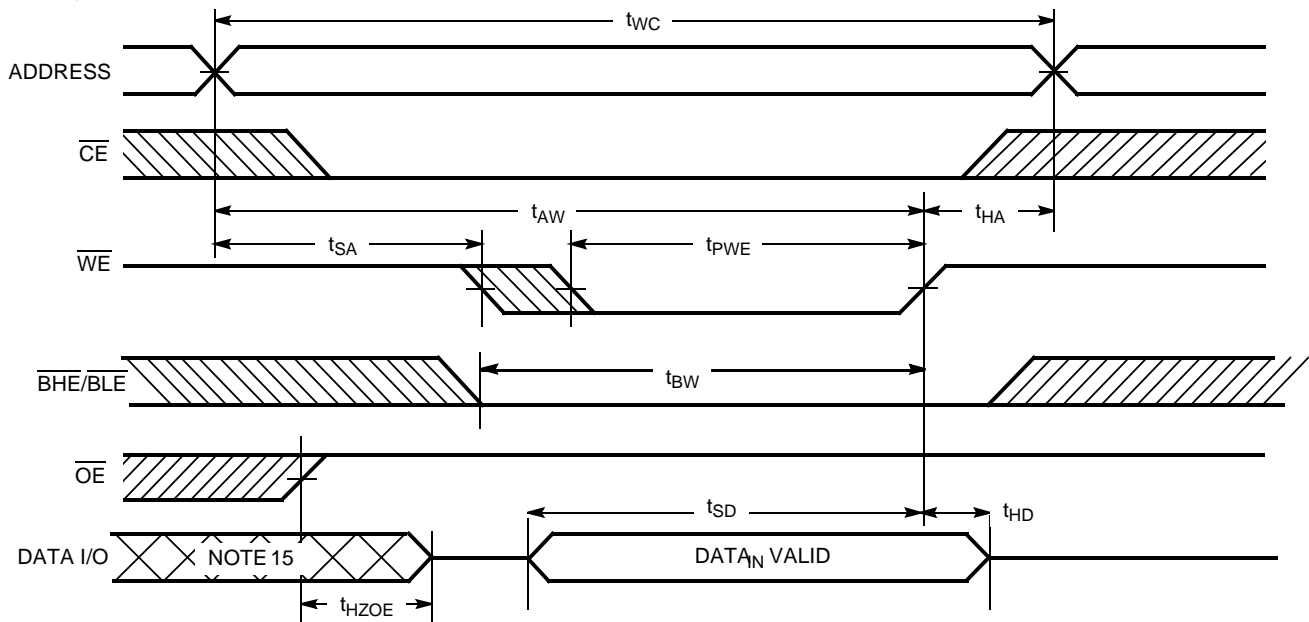
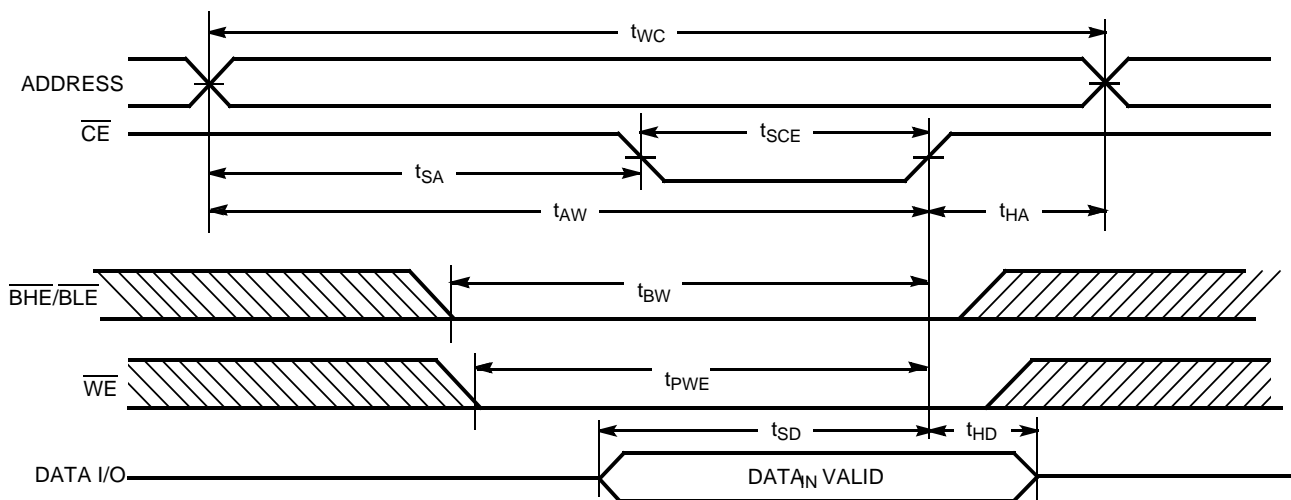


**Read Cycle No. 2** <sup>[11, 12]</sup>

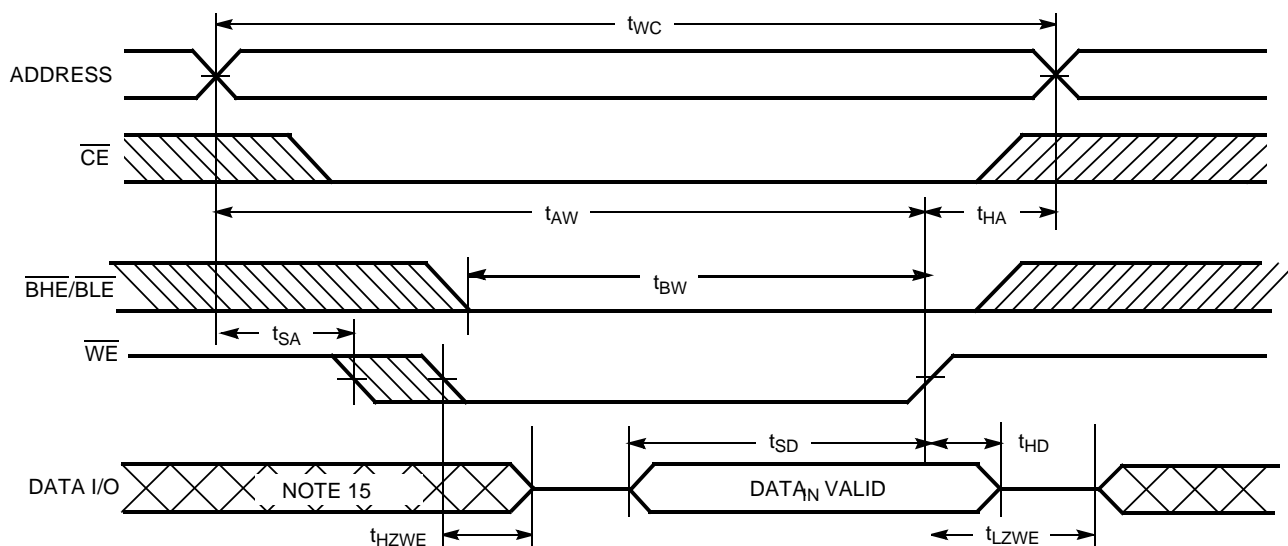
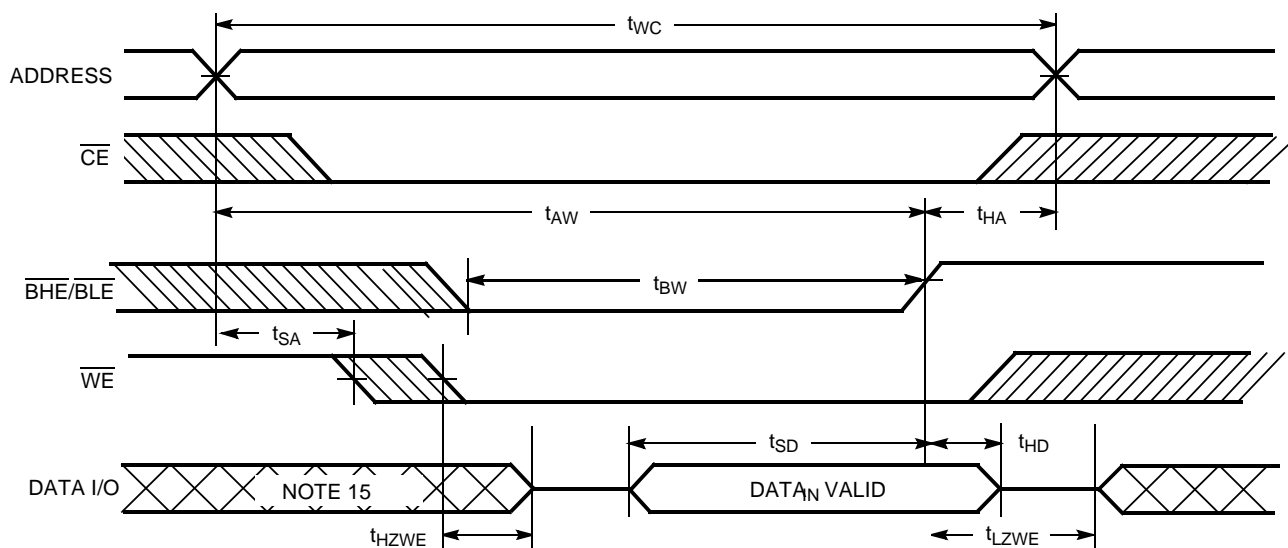


**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

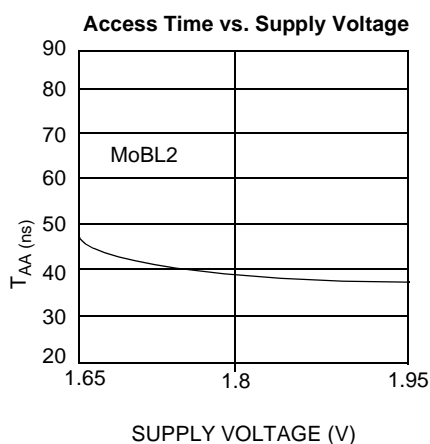
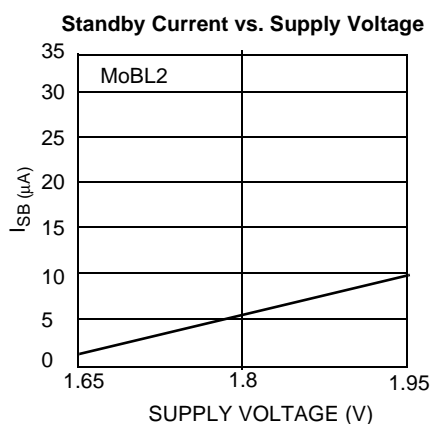
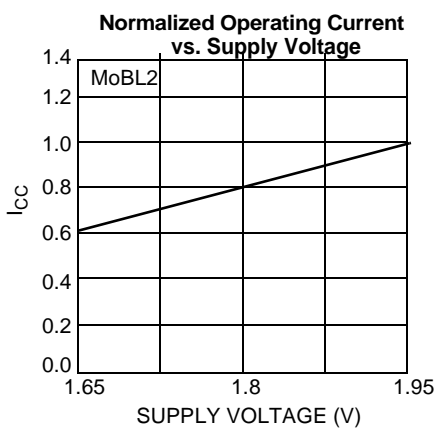
**Switching Waveforms (continued)**
**Write Cycle No. 1 (WE Controlled)** [8, 13, 14]

**Write Cycle No. 2 (CE Controlled)** [8, 13, 14]

**Notes:**

13. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[9, 14]</sup>**

**Write Cycle No. 4 (BHE/BL $\overline{\text{E}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[15]</sup>**




## Typical DC and AC Characteristics



## Truth Table

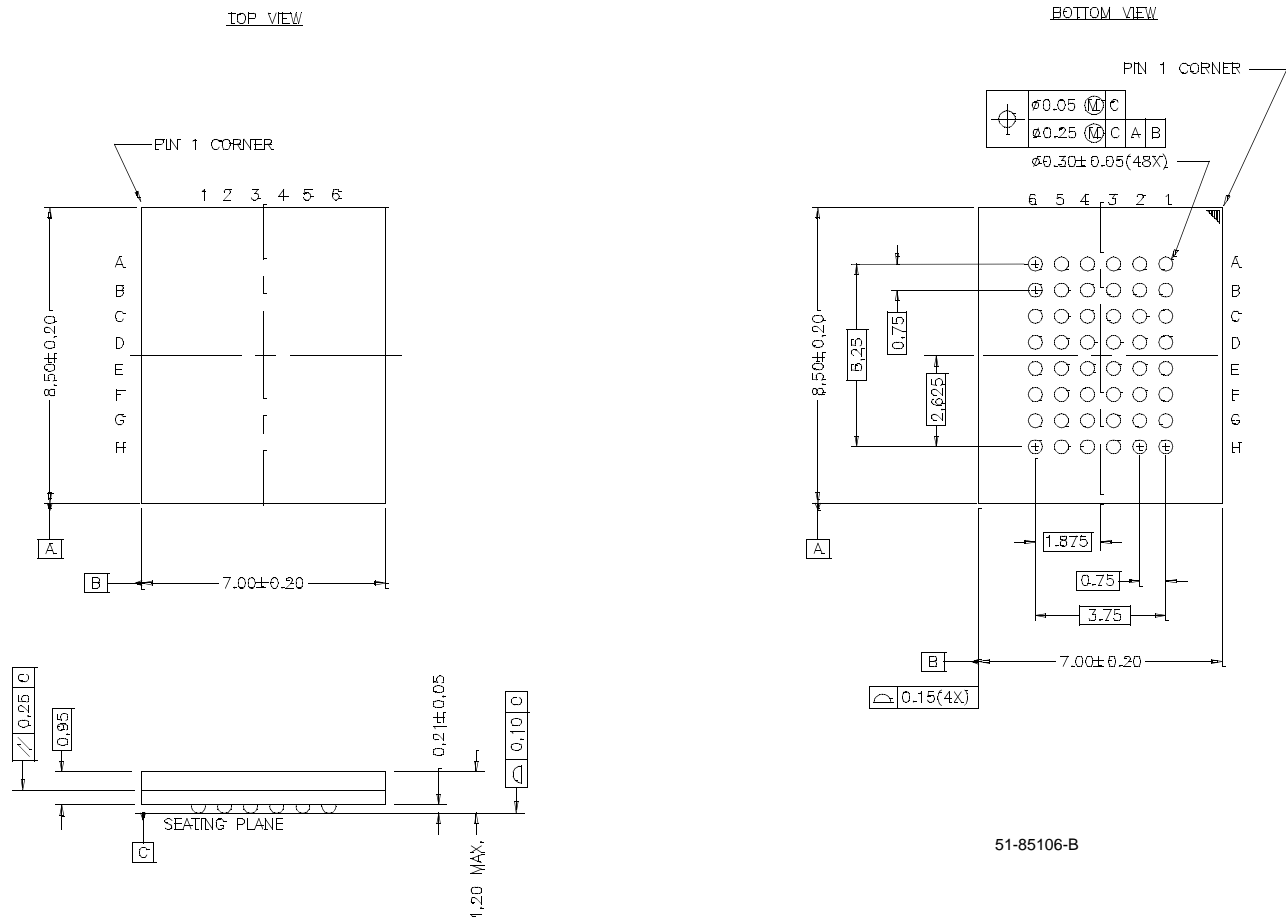
CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147CV18LL-70BAI	BA49	48-Ball Fine Pitch BGA	Industrial
55	CY62147CV18LL-55BAI			

## Package Diagrams

### 48-Ball (7.00 mm x 8.5 mm x 1.1 mm) Thin BGA BA49



51-85106-B



**PRELIMINARY**

**CY62147CV18 MoBL2™**

Document Title: CY62147CV18 MoBL2 256K x 16 SRAM Document Number: 38-05011				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106040	05/08/01	HRT/MGN	New Data Sheet