CY62147CV25/30/33

ADVANCE INFORMATION **MoBL™**

256K x 16 Static RAM

Features

- **Low voltage range:**
  - **— CY62147CV25: 2.2V–2.7V**
  - **— CY62147CV30: 2.7V–3.3V**
  - **— CY62147CV33: 3.0V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

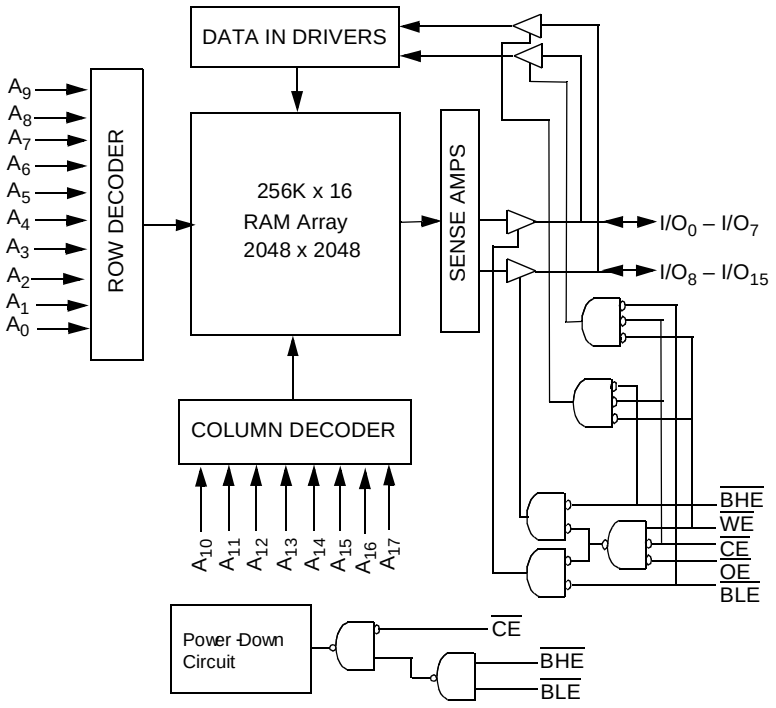
The CY62147CV25/30/33 are high-performance CMOS static RAMs organized as 262,144 words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH) or when $\overline{CE}$ is LOW and both BLE and $\overline{BHE}$ are HIGH. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and BLE are disabled ($\overline{BHE}$, BLE HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

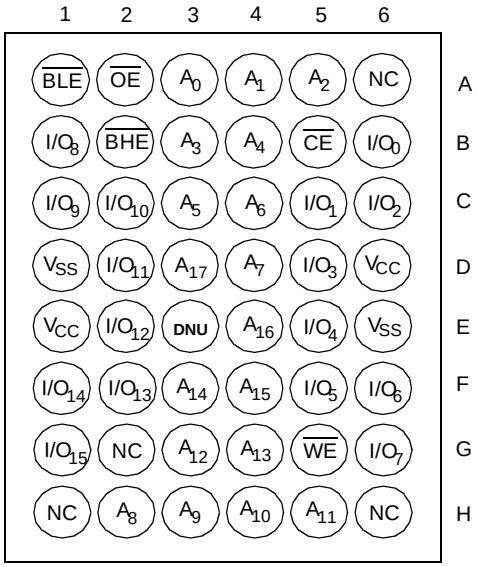
The CY62147CV25/30/33 are available in a 48-ball FBGA package. DNU on ball E3 is a “Do Not Use” pin, connecting to V_{SS} will not affect performance

Logic Block Diagram



Pin Configurations

FBGA (Top View)



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with
Power Applied–55°C to +125°C

Supply Voltage to Ground Potential–0.5V to +3.6V

DC Voltage Applied to Outputs
in High Z State[1]–0.5V to V_{CC} + 0.5V

DC Input Voltage[1]–0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)20 mA

Static Discharge Voltage >2100V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62147CV25	Industrial	–40°C to +85°C	2.2V to 2.7V
CY62147CV30			2.7V to 3.3V
CY62147CV33			3.0V to 3.6V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating (I_{CC})				Standby (I_{SB2})	
					55 ns		70 ns			
	$V_{CC(min.)}$	$V_{CC(typ.)}$[2]	$V_{CC(max.)}$		Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.
CY62147CV25	2.2V	2.5V	2.7V	55,70	12 mA	25 mA	7 mA	15 mA	5 µA	15 µA
CY62147CV30	2.7V	3.0V	3.3V	55,70	12 mA	25 mA	7 mA	15 mA	7 µA	15 µA
CY62147CV33	3.0V	3.3V	3.6V	55,70	12 mA	25 mA	7 mA	15 mA	8 µA	20 µA

Notes:
1. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62147CV25-55			CY62147CV25-70			Unit
					Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = Min.		2.0			2.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = Min.				0.4			0.4	V
V_{IH}	Input HIGH Voltage				1.8		V_{CC}+ 0.3V	1.8		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage				–0.3		0.6	–0.3		0.6	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS Levels	V_{CC} = Max.			12	25		7	15	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels				1	2		1	2	mA
I_{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{max} (Address and Data Only), f = 0 (OE,WE,BHE,and BLE)				5	15		5	15	µA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0, Vcc=Max.		LL							

Parameter	Description	Test Conditions			CY62147CV30-55			CY62147CV30-70			Unit
					Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = Min.		2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = Min.				0.4			0.4	V
V_{IH}	Input HIGH Voltage				2.2		V_{CC} + 0.5V	2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage				–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS Levels	V_{CC} = Max.			12	25		7	15	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels				1	2		1	2	mA
I_{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{max} (Address and Data Only), f = 0 (OE,WE,BHE,and BLE)				7	15		7	15	µA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0, Vcc=Max.		LL							

Parameter	Description	Test Conditions		CY62147CV33-55 Min.	CY62147CV33-55 Typ.	CY62147CV33-55 Max.	CY62147CV33-70 Min.	CY62147CV33-70 Typ.[2]	CY62147CV33-70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = Min.	2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA	V_{CC} = Min.			0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2		Vcc + 0.5V	2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage			-0.3		0.8	–0.3		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		-1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		-1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$, CMOS Levels	V_{CC} = Max.		12	25		7	15	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2		1	2	mA
I_{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{max} (Address and Data Only), f = 0 (OE,WE,BHE,and BLE)			8	20		8	20	µA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0, V_{CC} = Max.	LL							

Capacitance[3]

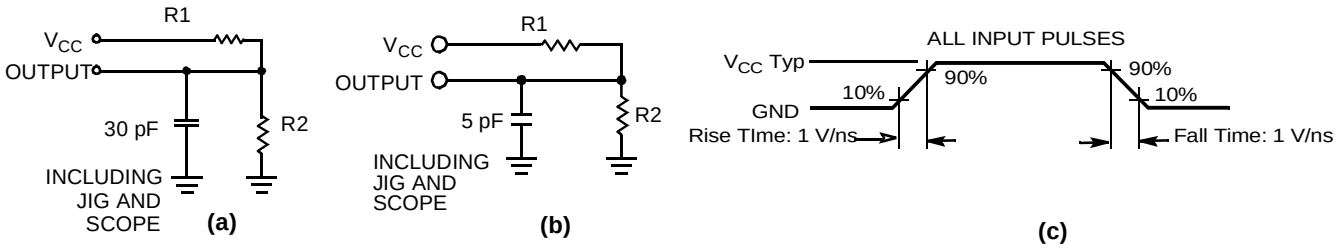
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

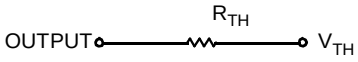
Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient)[3]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	55	°C/W
Thermal Resistance (Junction to Case)[3]		Θ_{JC}	16	°C/W

Note:
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

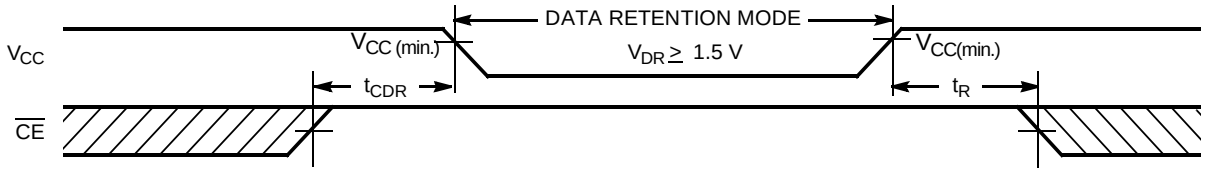


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.105	KΩ
R2	15.4	1.550	1.550	KΩ
R_{TH}	8	0.645	0.645	KΩ
V_{TH}	1.20	1.75	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5		V_{ccmax}	V
I_{CCDR}	Data Retention Current	$\overline{V_{CC}}$= 1.5V $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed V_{CC} + 0.3V	LL		3	10	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0			ns
t_R[4]	Operation Recovery Time			70			ns

Data Retention Waveform



Note:
4. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 50 µs or stable at $V_{CC(min.)}$ >50 µs.

Switching Characteristics Over the Operating Range[5]

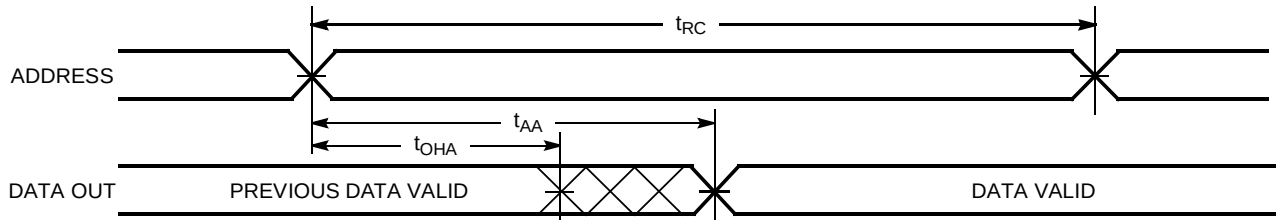
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6, 8]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 8]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t_{DBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		30		70	ns
t_{LZBE}[7]	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z	5		5		ns
t_{HZBE}	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z		20		25	ns
WRITE CYCLE[9, 10]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t_{AW}	Address Set-Up to Write End	0		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	45		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		50		ns
t_{BW}	$\overline{BHE}$ / $\overline{BLE}$ Pulse Width	0		60		ns
t_{SD}	Data Set-Up to Write End	30		30		ns
t_{HD}	Data Hold from Write End	5		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 8]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	10		10		ns

Notes:

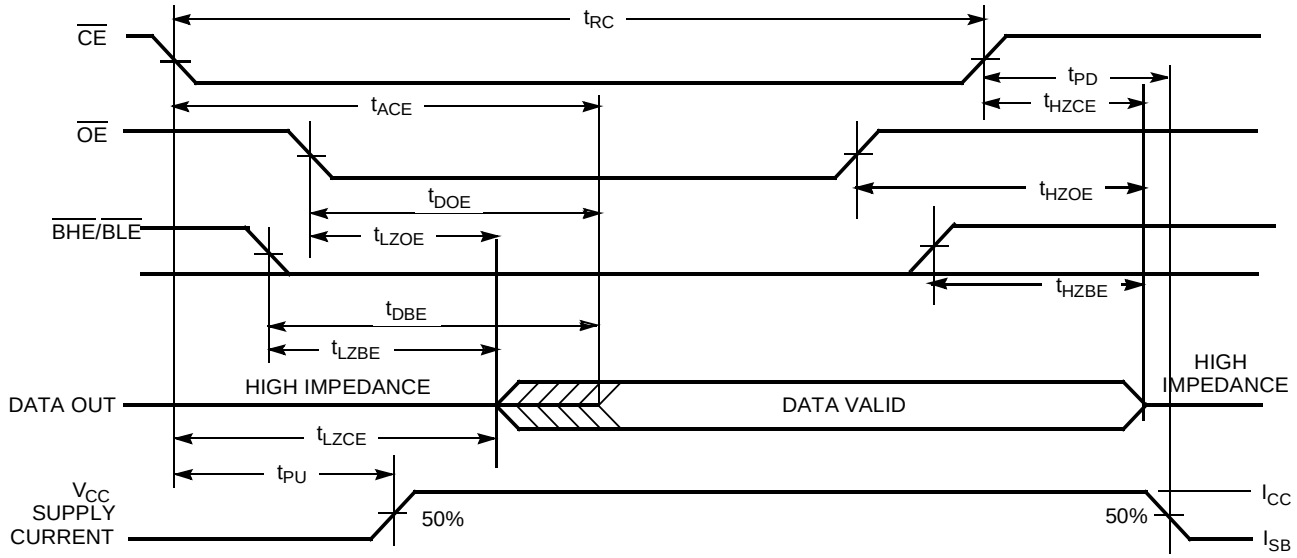
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. If both byte enables are toggled together this value is 10 ns
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Read Cycle No. 1 [11, 12]



Read Cycle No. 2 [12, 13]

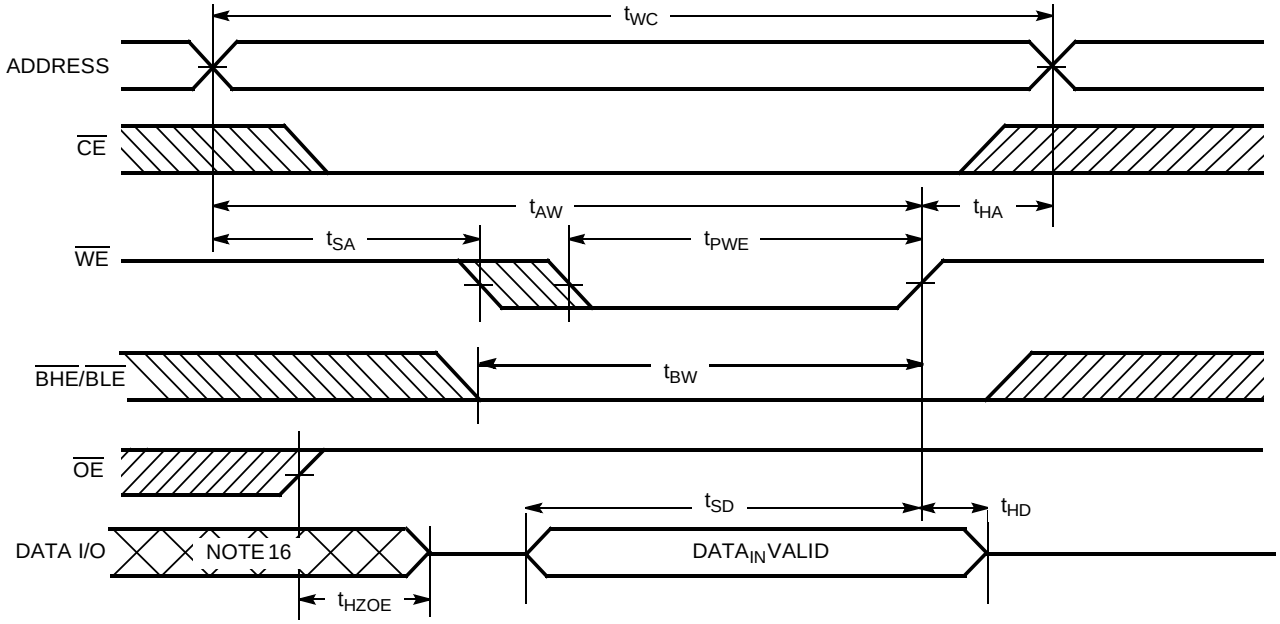


Notes:

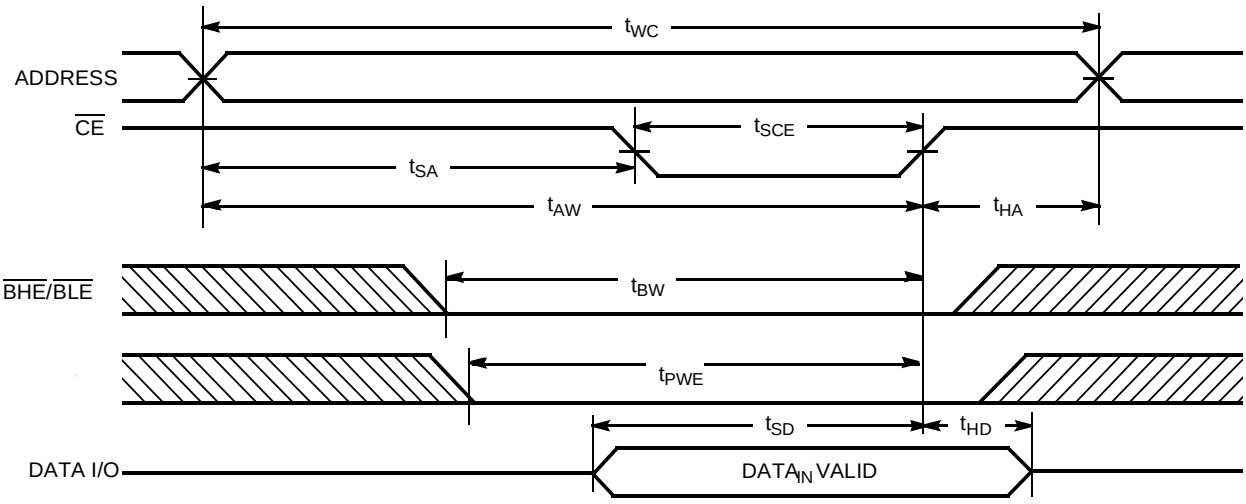
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled) [9, 14, 15]



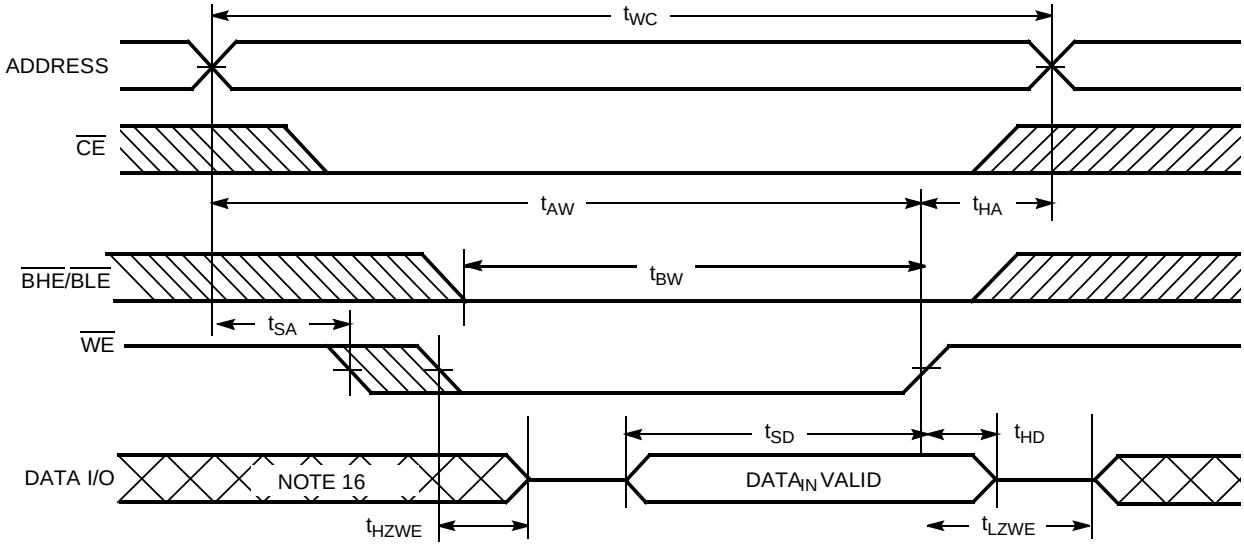
Write Cycle No. 2 (CE Controlled) [8, 14, 15]



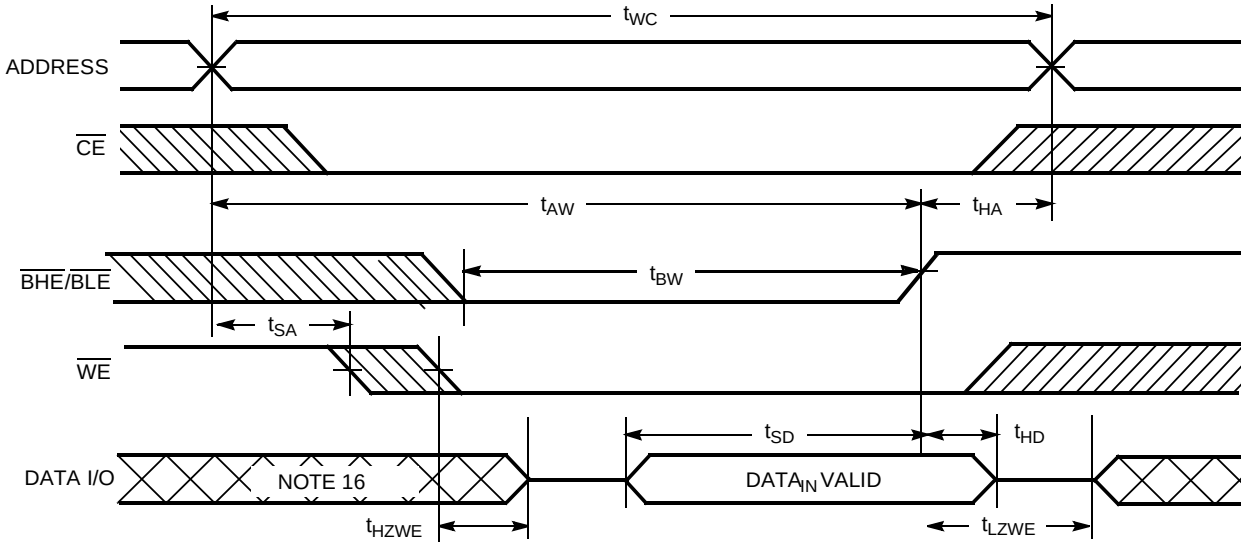
Notes:
14. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 15]



Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[16]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147CV25LL-70BAI	BA48B	48-Ball Fine Pitch BGA	Industrial
	CY62147CV30LL-70BAI			
	CY62147CV33LL-70BAI			
55	CY62147CV25LL-55BAI			
	CY62147CV30LL-55BAI			
	CY62147CV33LL-55BAI			

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Package Diagrams

48-Ball (7.00 mm x 8.5 mm x 1.20 mm) Fine Pitch BGA BA48B