

512K x 8 Static RAM

Features

- 4.5V – 5.5V operation
- CMOS for optimum speed/power
- Low active power
— 660 mW (max.)
- Low standby power (L version)
— 2.75 mW (max.)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} options

Functional Description

The CY62148 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. This device has

an automatic power-down feature that reduces power consumption by more than 99% when deselected.

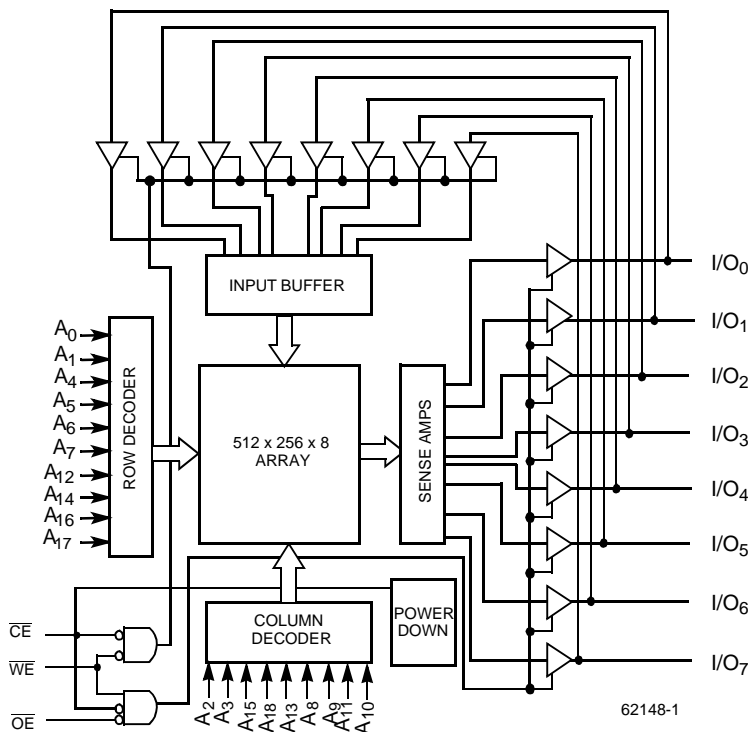
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

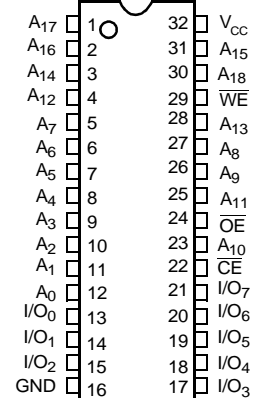
The CY62148 is available in a standard 32 pin 450-mil-wide body width SOIC and 32 pin TSOP II packages.

Logic Block Diagram



Pin Configuration

Top View
SOIC
TSOP II



Selection Guide

			CY62148 -70	CY62148 -100
Maximum Access Time (ns)			70	100
Maximum Operating Current			120	120
	L		90	90
	LL		90	90
Maximum CMOS Standby Current			2 mA	2 mA
	L		100 μ A	100 μ A
	Commercial	LL	20 μ A	20 μ A
	Industrial	LL	40 μ A	40 μ A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with
Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5\text{V}$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5\text{V}$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	4.5V–5.5V
Industrial	-40°C to $+85^{\circ}\text{C}$	

Electrical Characteristics Over the Operating Range

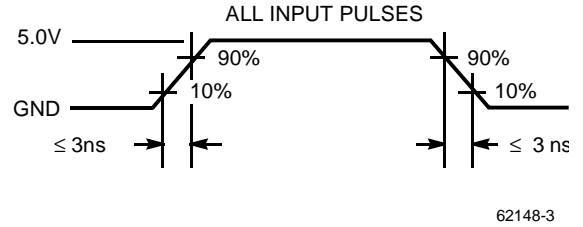
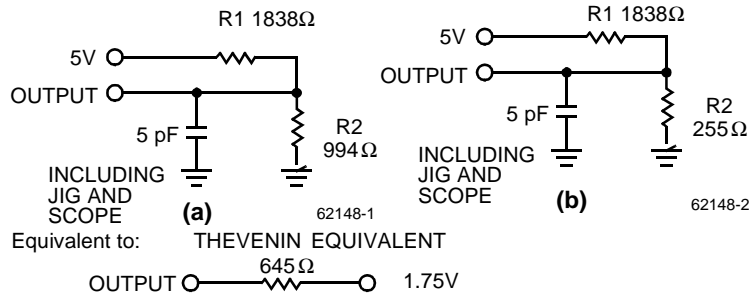
Parameter	Description	Test Conditions	Min.	Typ ^[3]	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1\text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1\text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage		2.2		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1		$+1$	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1		$+1$	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0\text{ mA},$ $f = f_{MAX} = 1/t_{RC}$			120	mA
		L			90	mA
		LL			90	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$			15	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3\text{V},$ $V_{IN} \geq V_{CC} - 0.3\text{V},$ or $V_{IN} \leq 0.3\text{V}, f = 0$		1.6 μA	2	mA
		L		1.6	100	μA
		Com'l LL		1.6	20	μA
		Ind'l LL		1.6	40	μA

Notes:

- $V_{IL}(\text{min.}) = -2.0\text{V}$ for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- Typical values are measured at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$, and are included for reference only and are not tested or guaranteed.

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


Switching Characteristics^[5] Over the Operating Range

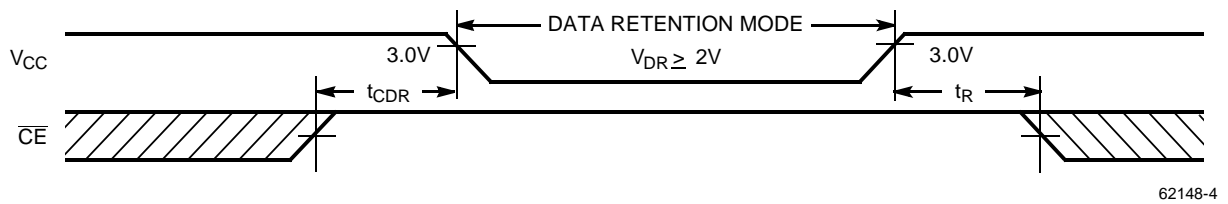
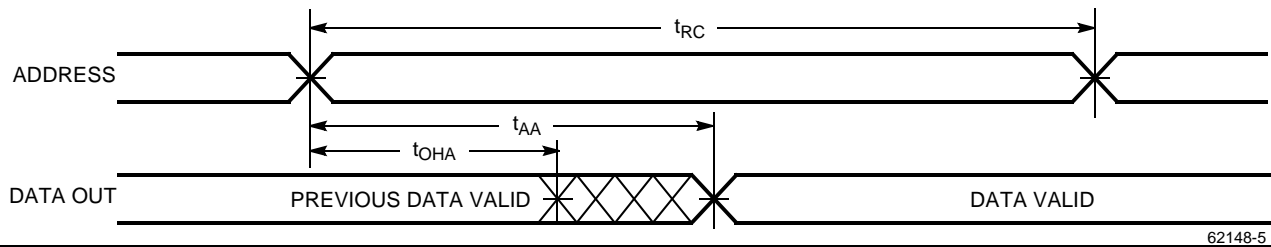
Parameter	Description	62148-70		62148-100		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	70		100		ns
t _{AA}	Address to Data Valid		70		100	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		70		100	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35		50	ns
t _{LZOE}	\overline{OE} LOW to Low Z	5		5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		25		30	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	10		10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25		30	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		70		100	ns
WRITE CYCLE ^[8]						
t _{WC}	Write Cycle Time	70		100		ns
t _{SCE}	\overline{CE} LOW to Write End	60		80		ns
t _{AW}	Address Set-Up to Write End	60		80		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	50		60		ns
t _{SD}	Data Set-Up to Write End	25		25		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[7]	5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25		30	ns

Notes:

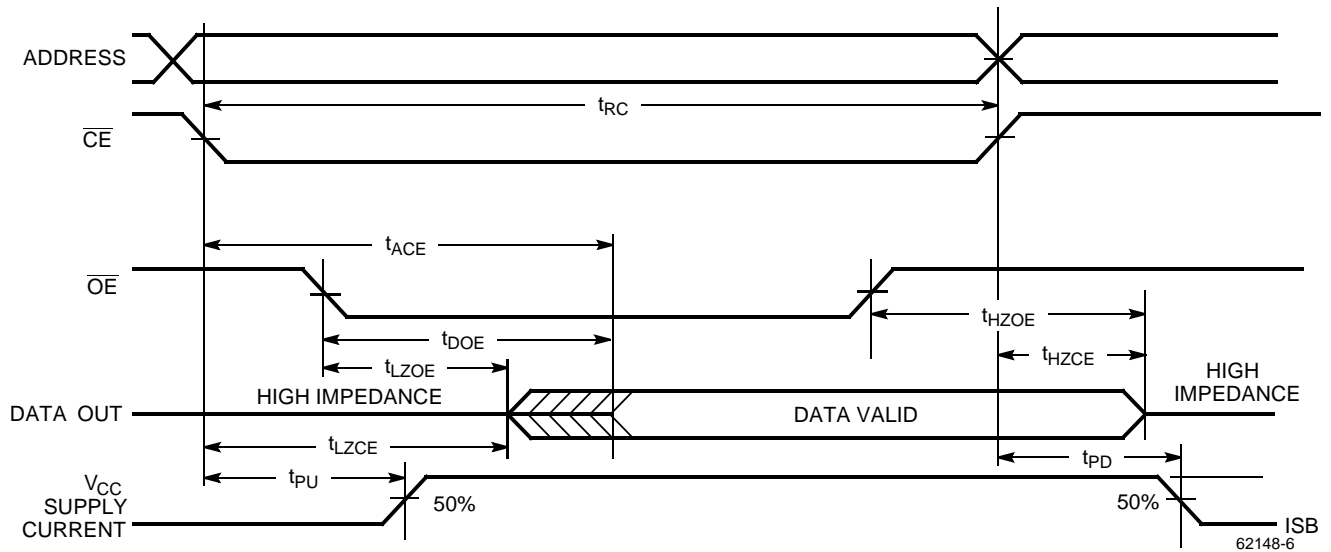
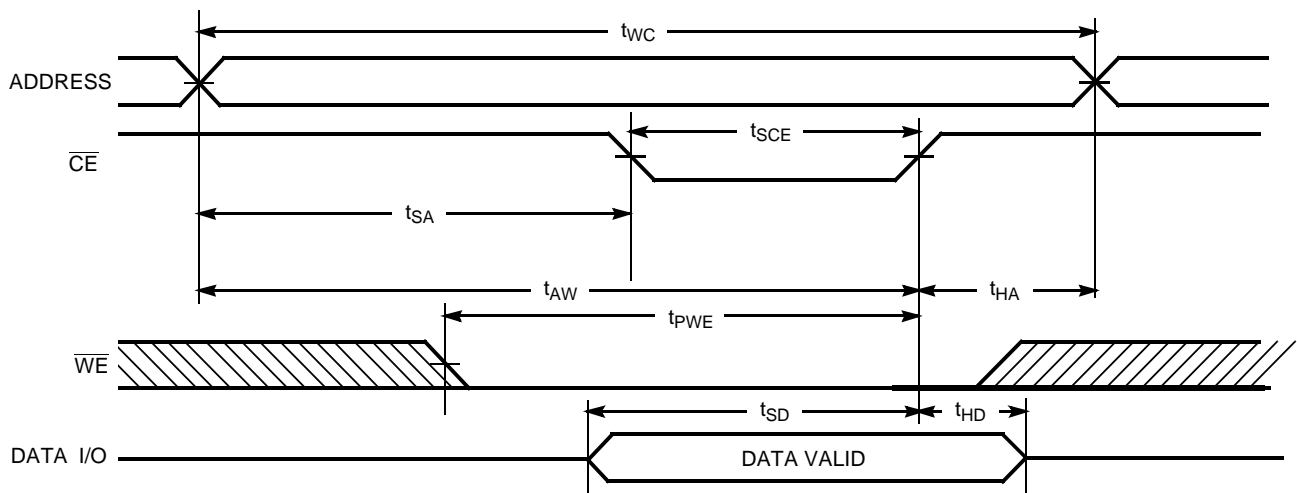
4. Tested initially and after any design or process changes that may affect these parameters.
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics (Over the Operating Range)

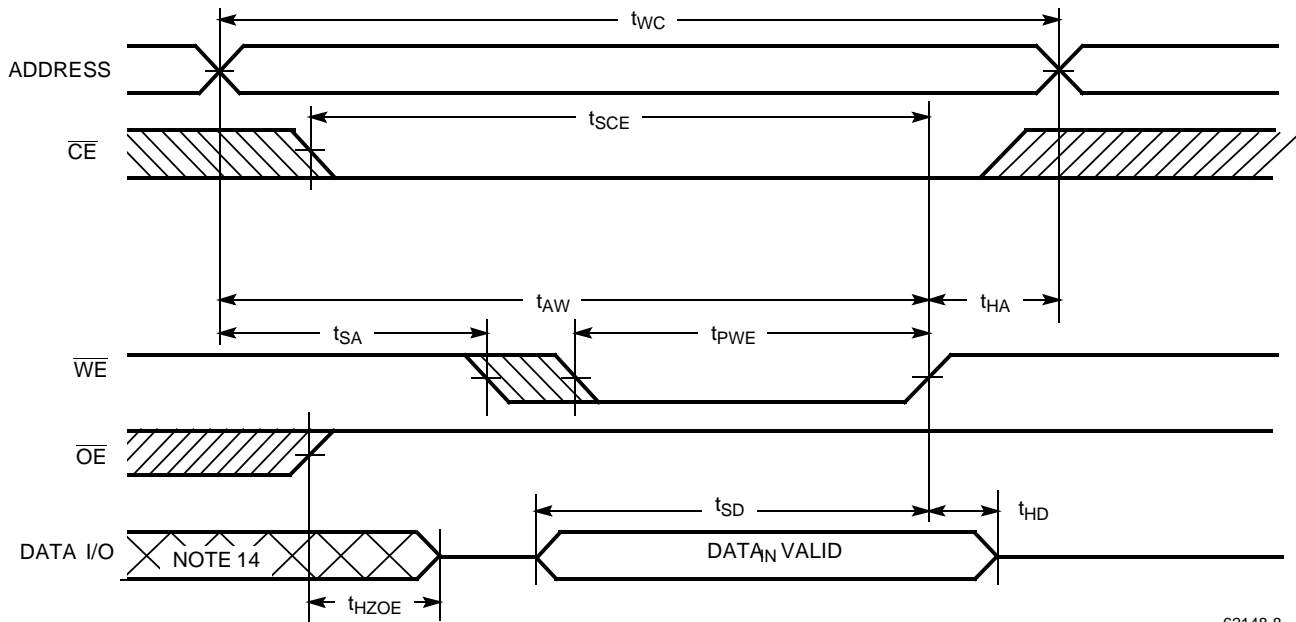
Parameter	Description			Conditions	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention				2.0			V
I_{CCDR}	Data Retention Current	Com'l		No input may exceed $V_{CC} + 0.3V$ $V_{CC} = V_{DR} = 3.0V, 0.3V$ $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} > V_{CC} - 0.3V$ or $V_{IN} < 0.3V$		1.6 μA	1.7	mA
			L				80	μA
			LL				20	μA
		Ind'l	LL				40	μA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time				0			ns
t_R	Operation Recovery Time				t_{RC}			ns

Data Retention Waveform

Switching Waveforms
Read Cycle No.1^[9, 10]

Notes:

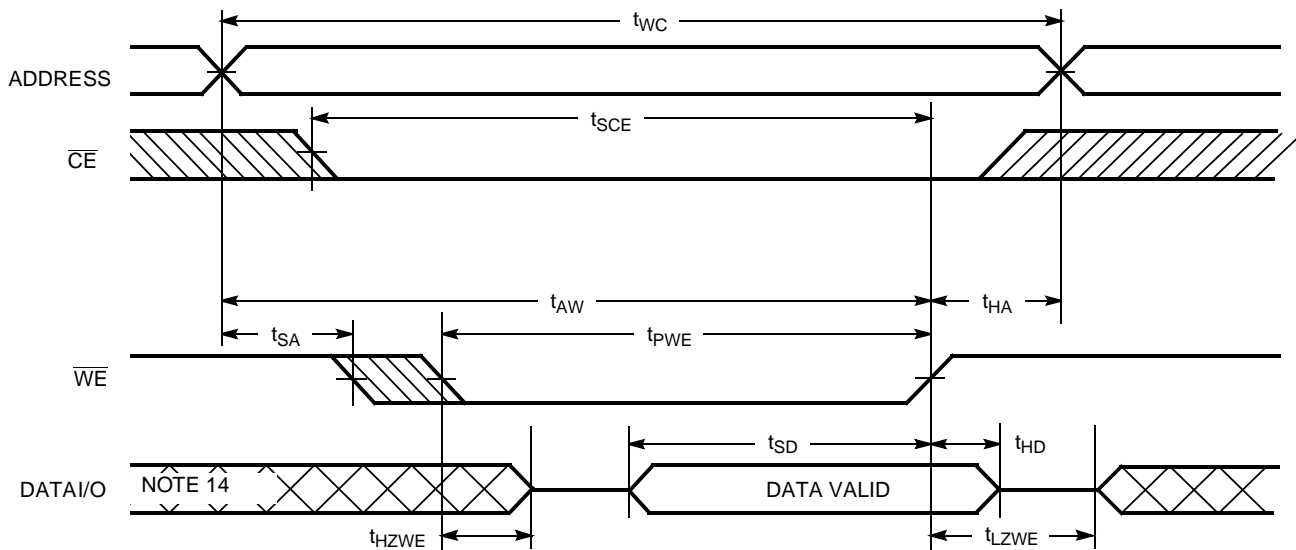
9. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
10. \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 (\overline{OE} Controlled)^[10, 11]

Write Cycle No. 1 (\overline{CE} Controlled)^[12, 13]

Notes:

11. Address valid prior to or coincident with \overline{CE} transition LOW.
12. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
13. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[12, 13]


62148-8

Write Cycle No.3 (\overline{WE} Controlled, \overline{OE} LOW)^[12, 13]


62148-9

Notes:

14. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	$I/O_0 - I/O_7$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Standby (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148-70SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY62148-70ZSC	ZS32	32-Lead TSOP II	
	CY62148L-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-70ZSC	ZS32	32-Lead TSOP II	
	CY62148LL-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-70ZSC	ZS32	32-Lead TSOP II	
	CY62148-70SI	S34	32-Lead (450-Mil) Molded SOIC	Industrial
	CY62148-70ZSI	ZS32	32-Lead TSOP II	
	CY62148L-70SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-70ZSI	ZS32	32-Lead TSOP II	
	CY62148LL-70SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-70ZSI	ZS32	32-Lead TSOP II	
100	CY62148-100SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148-100ZSC	ZS32	32-Lead TSOP II	
	CY62148L-100SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-100ZSC	ZS32	32-Lead TSOP II	
	CY62148LL-100ZSC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-100ZSC	ZS32	32-Lead TSOP II	
	CY62148-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148-100ZSI	ZS32	32-Lead TSOP II	
	CY62148L-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148L-100ZSI	ZS32	32-Lead TSOP II	
	CY62148LL-100SI	S34	32-Lead (450-Mil) Molded SOIC	
	CY62148LL-100ZSI	ZS32	32-Lead TSOP II	

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Package Diagrams

32-Lead (450 MIL) Molded SOIC S34

