



## 512K x 16 Static RAM

### Features

- Low voltage range:
  - CY62157CV25: 2.2V–2.7V
  - CY62157CV30: 2.7V–3.3V
  - CY62157CV33: 3.0V–3.6V
- Ultra-low active, standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- CMOS for optimum speed/power

### Functional Description

The CY62157CV25/30/33 are high-performance CMOS static RAMs organized as 512K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW) and both BLE and

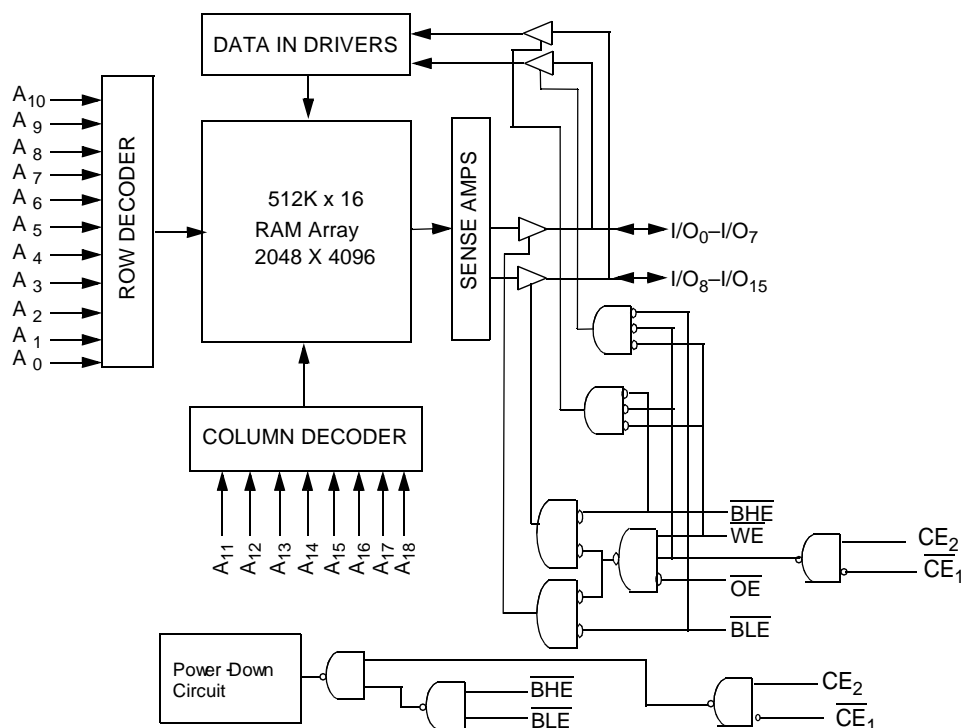
$\overline{BHE}$  are HIGH. The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH),  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}_1$  HIGH and  $\overline{CE}_2$  LOW, and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

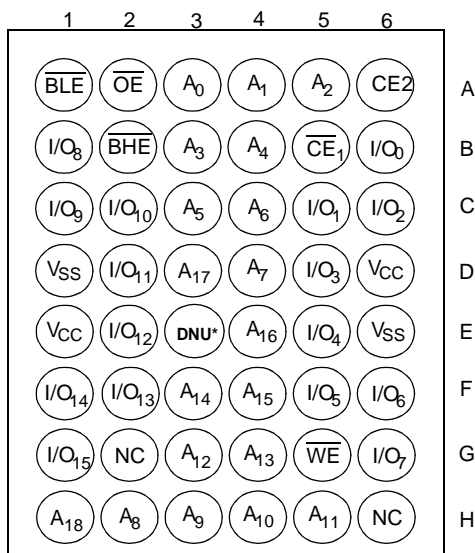
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62157CV25/30/33 are available in a 48-ball FBGA package. DNU\* on Ball E3 is a "Do Not Use" pin, connecting to  $V_{SS}$  will not affect performance.

### Logic Block Diagram



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**Pin Configurations**
**FBGA (Top View)**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential..... -0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2100V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Device	Range	Ambient Temperature	$V_{CC}$
CY62157CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62157CV30			2.7V to 3.3V
CY62157CV33			3.0V to 3.6V

**Product Portfolio**

Product	$V_{CC}$ Range			Speed	Power Dissipation (Industrial)					
					Operating ( $I_{CC}$ )				Standby ( $I_{SB2}$ )	
					55 ns		70 ns		Typ. <sup>[2]</sup>	Max
	$V_{CC(min.)}$	$V_{CC(typ.)}^{[2]}$	$V_{CC(max.)}$		Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.		
CY62157CV25	2.2V	2.5V	2.7V	55,70	12 mA	25 mA	7 mA	15 mA	6 $\mu A$	25 $\mu A$
CY62157CV30	2.7V	3.0V	3.3V	55,70	12 mA	25 mA	7 mA	15 mA	8 $\mu A$	25 $\mu A$
CY62157CV33	3.0V	3.3V	3.6V	55,70	12 mA	25 mA	7 mA	15 mA	10 $\mu A$	30 $\mu A$

**Notes:**

- $V_{IL(min.)} = -2.0V$  for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25^\circ C$ .

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62157CV25-55			CY62157CV25-70			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = Min.	2.0			2.0			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = Min.			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			1.8		V <sub>CC</sub> + 0.3V	1.8		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.6	-0.3		0.6	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = Max.		12	25		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels			1	2		1	2	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE, BHE, and BLE)			6	25		6	25	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = 0, $V_{CC} = \text{Max.}$	LL							

Parameter	Description	Test Conditions		CY62157CV30-55			CY62157CV30-70			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = Min.	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = Min.			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> + 0.5V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = Max.		12	25		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels			1	2		1	2	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE, BHE, and BLE)			8	25		8	25	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = 0, $V_{CC} = \text{Max.}$	LL							

Parameter	Description	Test Conditions		CY62157CV33-55			CY62157CV33-70			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = Min.	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = Min.			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> +0.5V	2.2		V <sub>CC</sub> +0.5V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = Max.		12	25		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels			1	2		1	2	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE, BHE, and BLE)			10	30		10	30	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = 0, V <sub>CC</sub> = Max.	LL							

### Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ.)	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

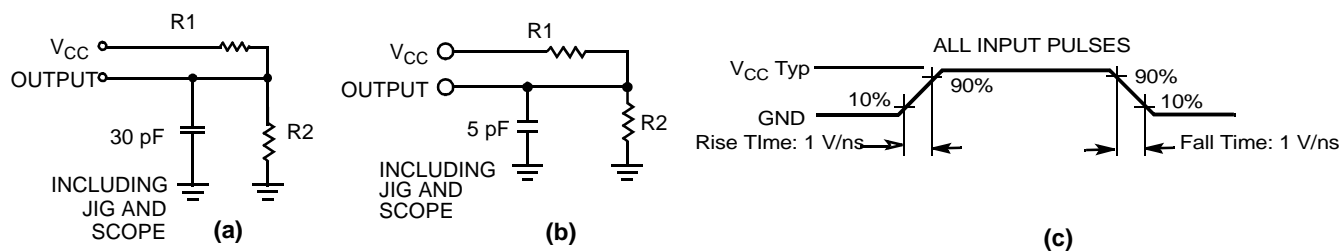
### Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance (Junction to Case) <sup>[3]</sup>		Θ <sub>JC</sub>	16	°C/W

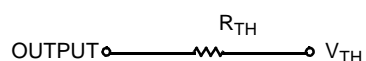
**Note:**

- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

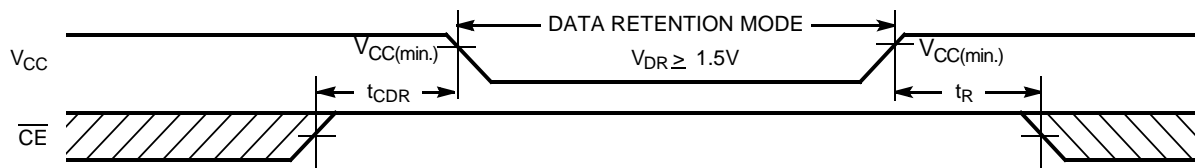


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.105	K $\Omega$
R2	15.4	1.550	1.550	K $\Omega$
$R_{TH}$	8	0.645	0.645	K $\Omega$
$V_{TH}$	1.20	1.75	1.75	V

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5		$V_{CCmax}$	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5V$ $CE_1 \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed $V_{CC} + 0.3V$	LL	4	20	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[4]}$	Operation Recovery Time		$t_{RC}$			ns

## Data Retention Waveform



### Note:

- Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} > 50 \mu s$  or stable at  $V_{CC(min.)} > 50 \mu s$ .
- $CE_x$  is the combinational output of  $CE_1$  and  $CE_2$ .

**Switching Characteristics** Over the Operating Range<sup>[6]</sup>

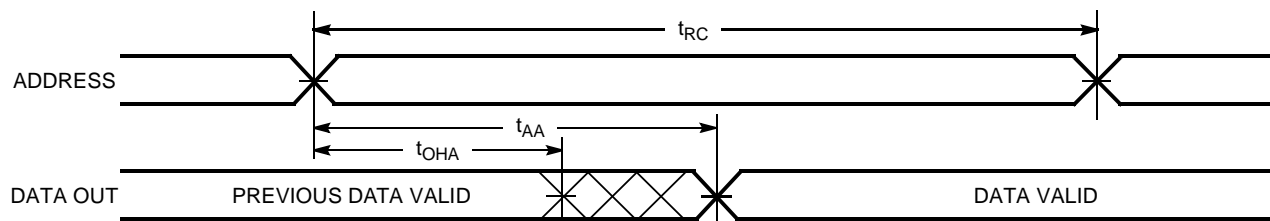
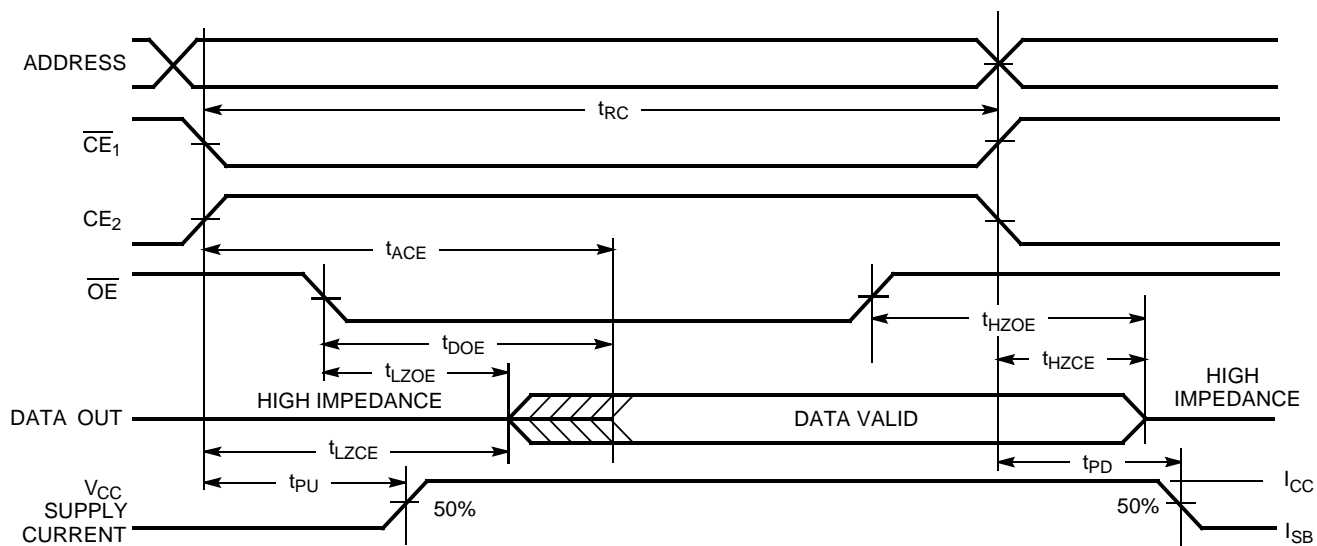
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7, 8]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[8]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t <sub>DBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub> <sup>[9]</sup>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z	5		5		ns
t <sub>HZBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z		25		25	ns
WRITE CYCLE <sup>[10, 11]</sup>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	45		50		ns
t <sub>BW</sub>	$\overline{BHE}$ / $\overline{BLE}$ Pulse Width	50		60		ns
t <sub>SD</sub>	Data Set-Up to Write End	30		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>		20		20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	5		10		ns

**Notes:**

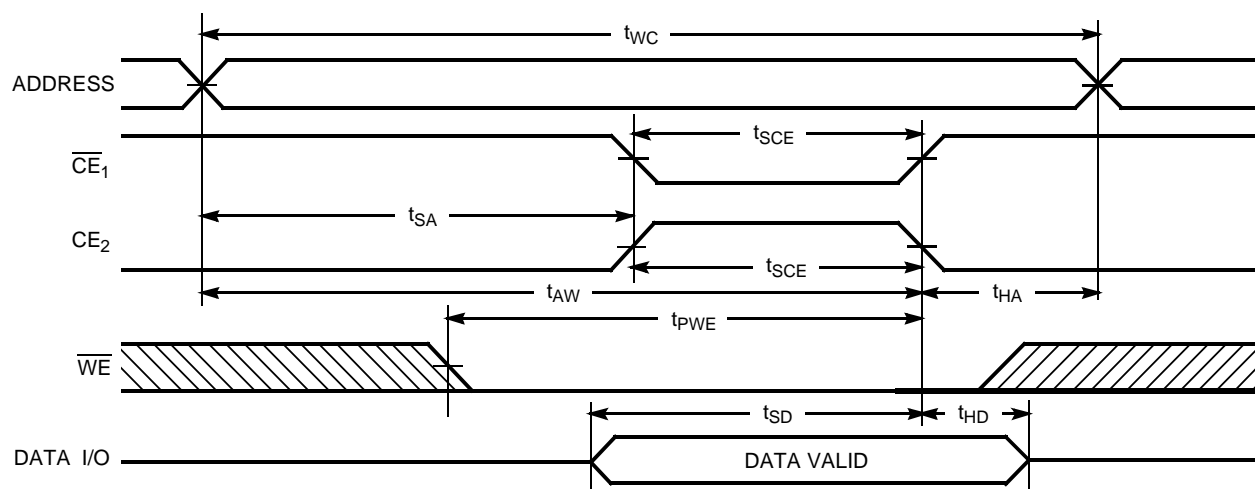
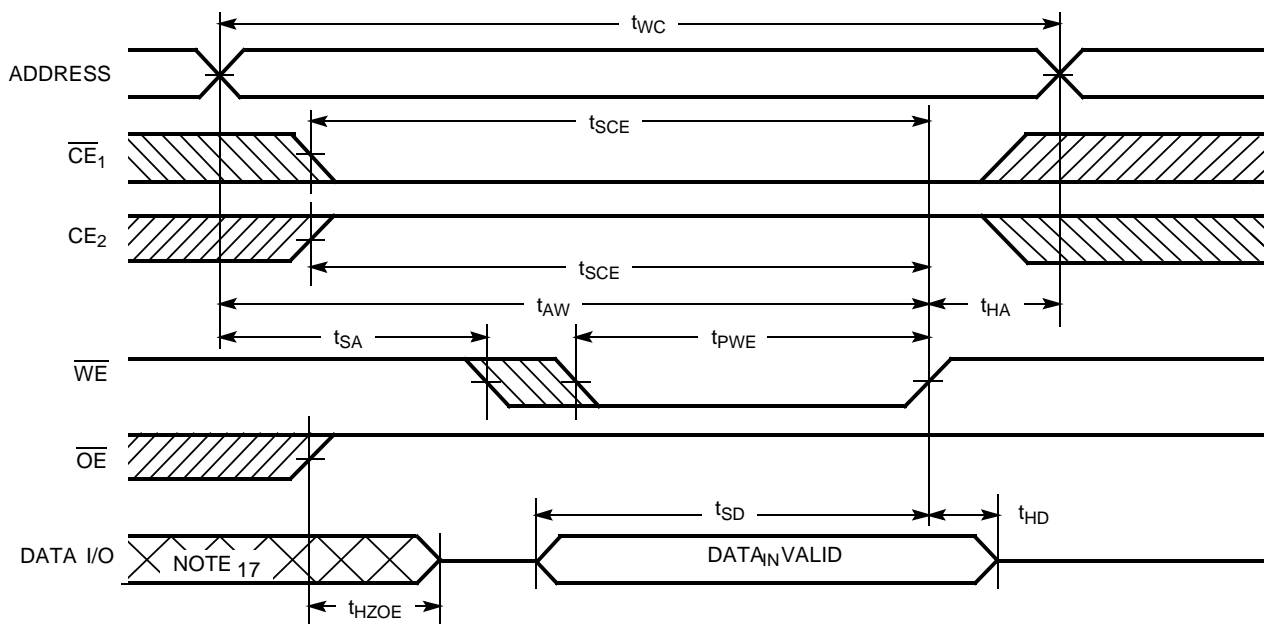
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
7. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
8.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
9. When both byte enables are toggled together this value is 10 ns.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH, and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .



### Read Cycle No. 1<sup>[12, 13]</sup>

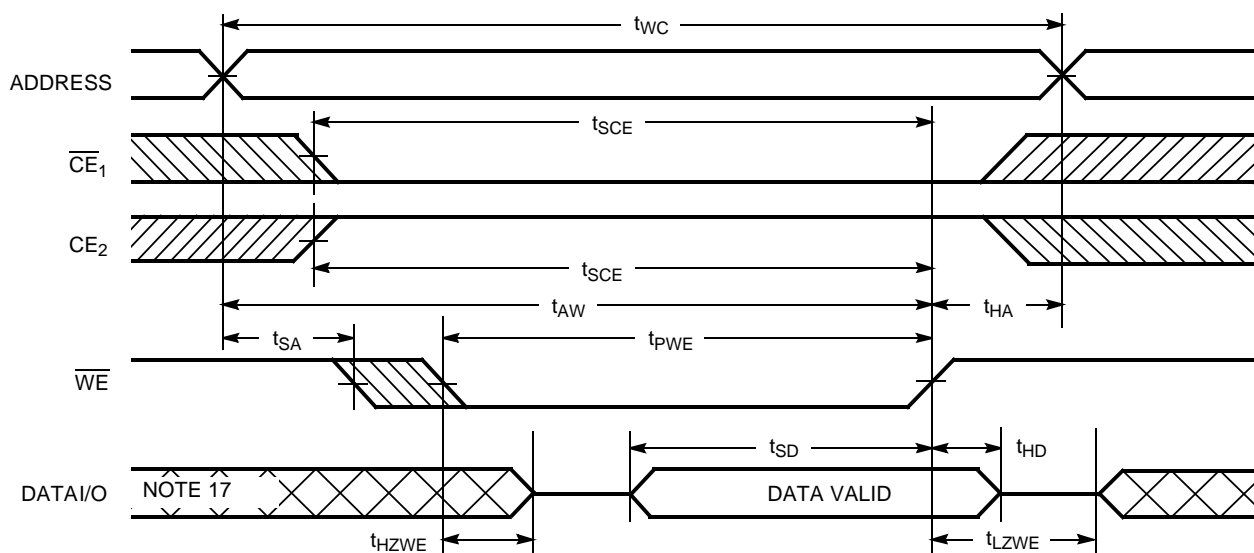
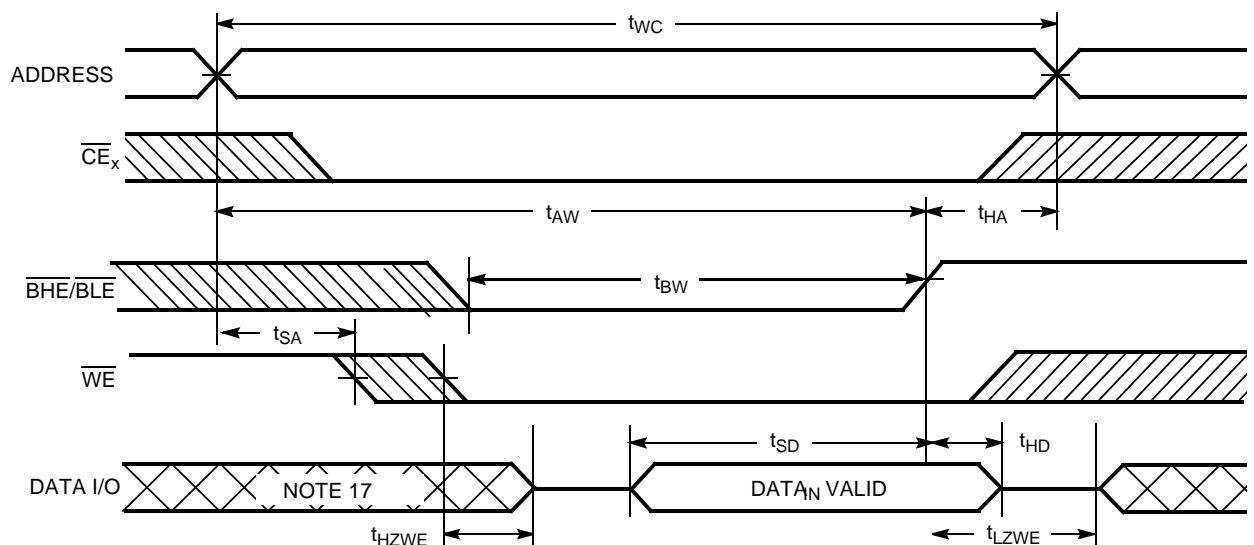
Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)<sup>[13,14]</sup>

12. Device is continuously selected.  $\overline{\text{OE}}, \overline{\text{CE}}_1 = \text{V}_{\text{IL}}, \text{CE}_2 = \text{V}_{\text{IH}}$ .
13.  $\overline{\text{WE}}$  is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{\text{CE}}_1$  transition LOW and  $\text{CE}_2$  transition HIGH.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[15,16]</sup>**

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[15,16]</sup>**

**Notes:**

15. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
16. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.



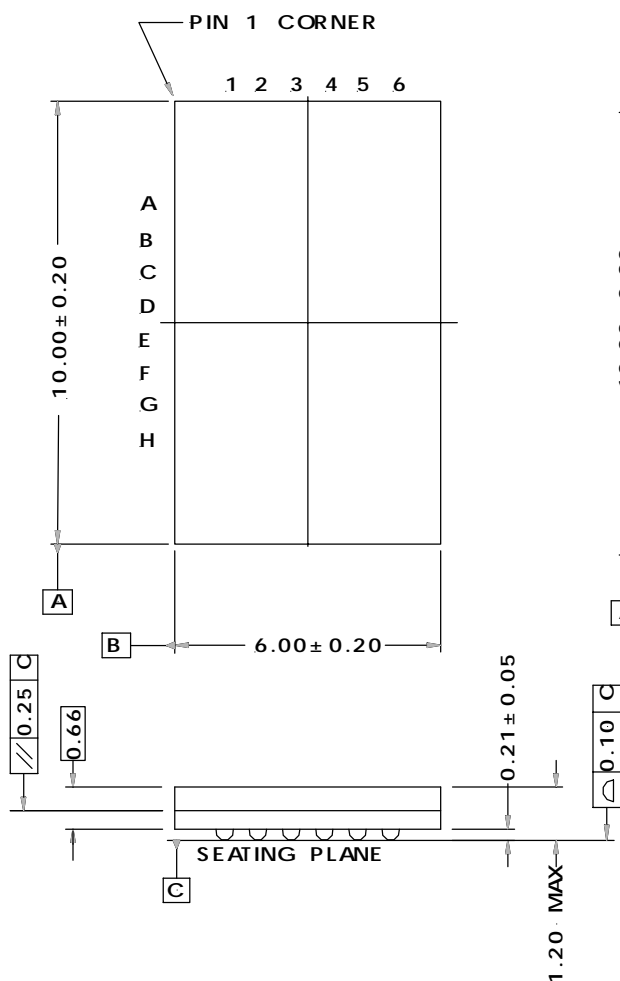
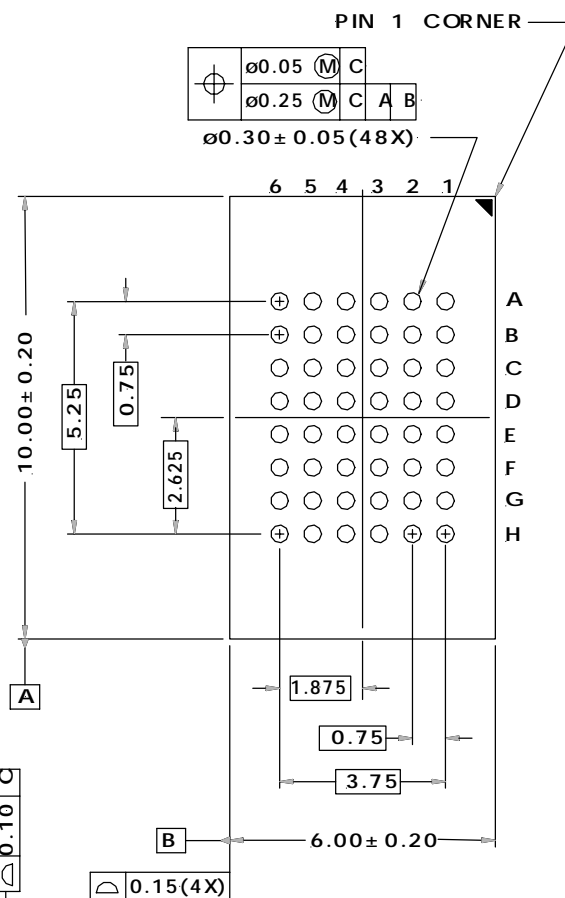
**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[11, 16]</sup>**

**Write Cycle No. 4 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[5, 17]</sup>**


**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62157CV25LL-70BAI	BA48C	48-Ball Fine Pitch BGA	Industrial
	CY62157CV30LL-70BAI			
	CY62157CV33LL-70BAI			
55	CY62157CV25LL-55BAI			
	CY62157CV30LL-55BAI			
	CY62157CV33LL-55BAI			

**Package Diagrams**
**48-Ball (6.00 mm x 10.00 mm x 1.20 mm) Fine Pitch BGA BGA48C**
**Top View**

**Bottom View**




Document Title: CY62157CV25/30/33 MoBL™ 512K x 16 STATIC RAM Document Number: 38-05014				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106184	05/10/01	HRT/MGN	New Data Sheet
*A	107241	07/24/01	MGN	Make Corrections to Advance Information. Added 55 ns bin.