PRELIMINARY

CY62256V

32K x 8 Static RAM

Features

- **Low voltage range:**
  - **2.7V – 3.6V (62256V)**
  - **2.3V – 2.7V (62256V25)**
  - **1.6V – 2.0V (62256V18)**
- **Low active power and standby power**
- **Easy memory expansion with CE and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

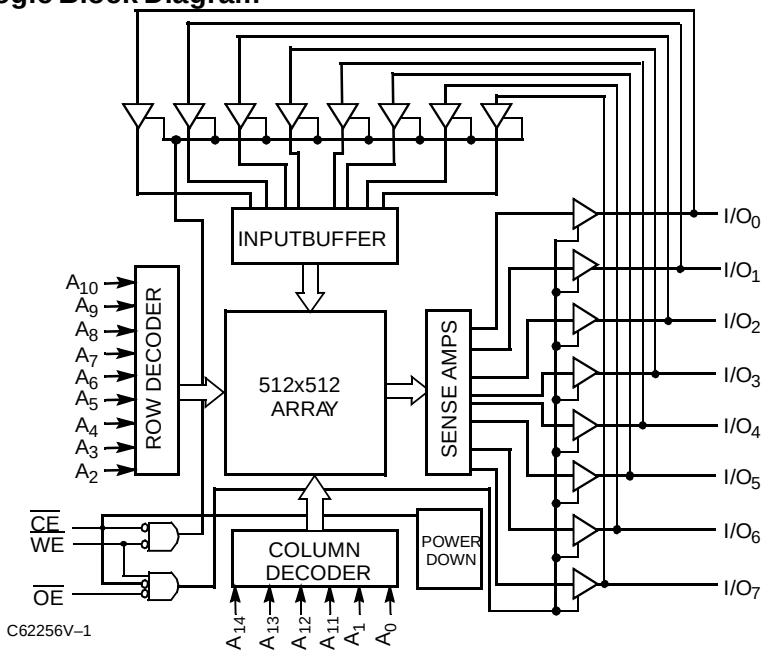
Functional Description

The CY62256V family is composed of three high-performance CMOS static RAM's organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE) and active LOW output enable (OE) and three-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected. The CY62256V family is available in the standard 450-mil-wide (300-mil body width) SOIC, TSOP, and reverse TSOP packages.

An active LOW write enable signal (WE) controls the writing/reading operation of the memory. When CE and WE inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, CE and OE active LOW, while WE remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH.

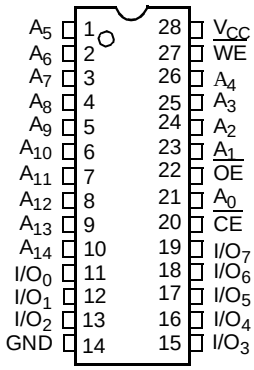
Logic Block Diagram



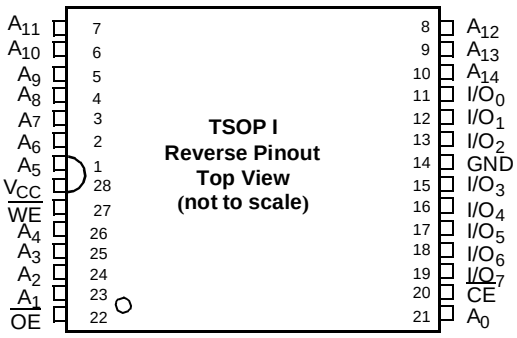
C62256V–1

Pin Configurations

SOIC
Top View

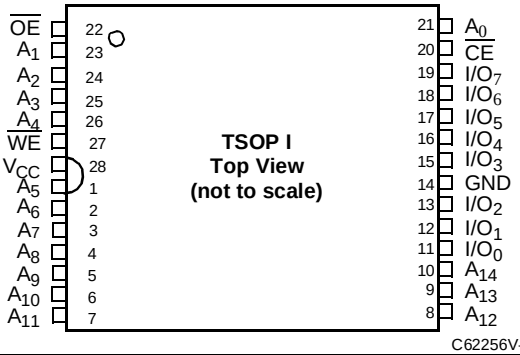


C62256V–2



TSOP I
Reverse Pinout
Top View
(not to scale)

C62256V–4



TSOP I
Top View
(not to scale)

C62256V–3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	1.6V to 3.6V
Industrial	–40°C to +85°C	1.6V to 3.6V

Note:
1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (LL Devices)			
					Operating(I_{CC})		Standby (I_{SB2})	
	Min.	Typ.	Max.		Typical	Maximum	Typical	Maximum
CY62256V	2.7V	3.0	3.6V	70 ns	11 mA	30 mA	0.1 µA	5 µA
CY62256V25	2.3V	2.5V	2.7V	100 ns	9 mA	15 mA	0.1 µA	4 µA
CY62256V18	1.6V	1.8V	2.0V	200 ns	5 mA	10 mA	0.1 µA	3 µA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62256V-70			Unit
					Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA					0.4	V
V_{IH}	Input HIGH Voltage				2.2		V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage				–0.5		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l	Std/L /LL		11	30	mA
I_{SB1}	Automatic CE Power-Down Current— TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l	Std/L /LL		100	300	µA
I_{SB2}	Automatic CE Power-Down Current— CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l	Std/ L		0.1	50	µA
				LL			5	µA
			Ind'l	LL			10	µA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62256V25-100			Unit
			Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –0.1 mA	2			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 0.1 mA			0.4	V
V_{IH}	Input HIGH Voltage		1.7		Vcc + 0.3V	V
V_{IL}	Input LOW Voltage		–0.3		0.7	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1		+1	µA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions			CY62256V25-100 Min.	CY62256V25-100 Typ.[2]	CY62256V25-100 Max.	Unit
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l	Stnd/L /LL		14	23	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l	Stnd/L /LL		75	225	µA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l	Stnd/L		0.1	40	µA
				LL			4	µA
			Ind'l	LL			8	µA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62256V18-200 Min.	CY62256V18-200 Typ.[2]	CY62256V18-200 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –0.1 mA			0.8*Vcc			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 0.1 mA					0.2	V
V_{IH}	Input HIGH Voltage				0.7*Vcc		V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage				–0.5		0.2*Vcc	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l	Stnd/L /LL		10	17	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l	Stnd/L /LL		56	165	µA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l	Stnd/L		0.1	30	µA
				LL			3	µA
			Ind'l	LL			6	µA

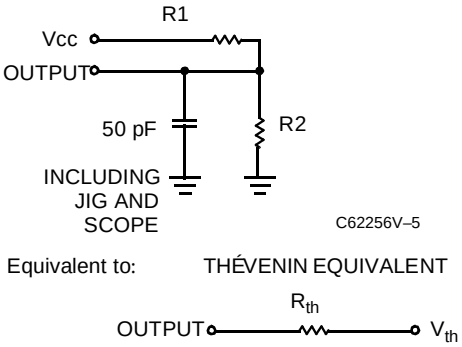
Capacitance[3]

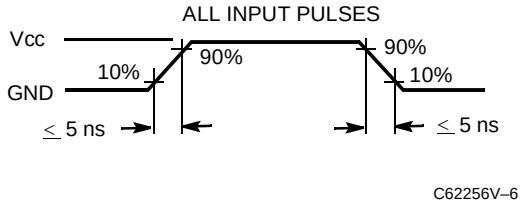
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = Vcc Typ., T_A = 25°C, and t_{AA}=70ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



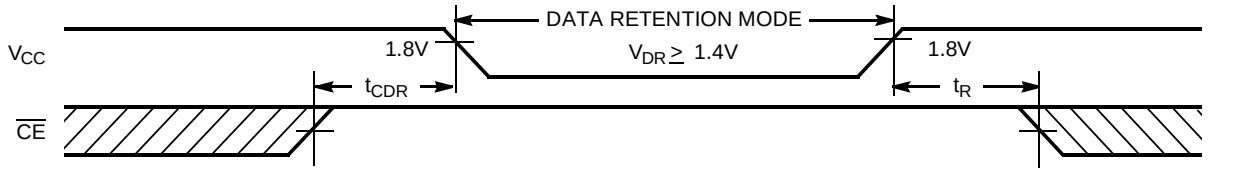


AC Test Load			
Vcc	**3.3 V**	**2.5V**	**1.8V**
R1	1103	16.6K	13.6K
R2	1554	15.4K	11.4K
RTH	645	8K	6.2K
VTH	1.75V	1.2V	0.82V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description			Conditions[4]	Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention				1.4			V
I_{CCDR}	Data Retention Current	Coml	Stnd/L	V_{CC} = 1.6 $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		0.1	30	uA
			LL				3	uA
		Ind.	LL				6	uA
t_{CDR}[3]	Chip Deselect to Data Retention Time				0			ns
t_R[3]	Operation Recovery Time				t_{RC}			ns

Data Retention Waveform

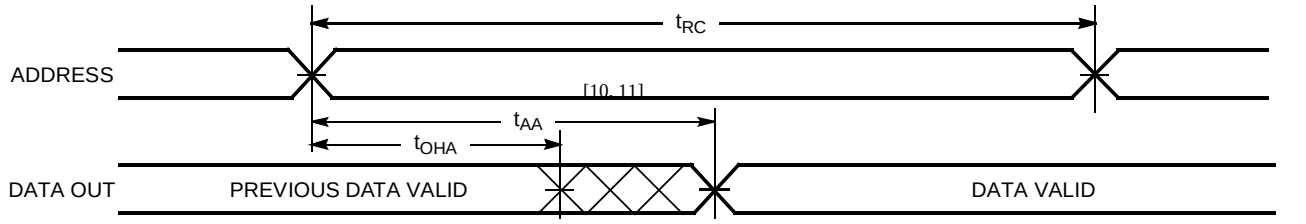


Switching Characteristics Over the Operating Range[5]

Parameter	Description	CY62256V-70		CY62256V25-100		CY62256V18-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	70		100		200		ns
t_{AA}	Address to Data Valid		70		100		200	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70		100		200	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35		75		125	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	5		5		10		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		25		50		75	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	10		10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		25		50		75	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		70		100		200	ns
WRITE CYCLE[8,9]								
t_{WC}	Write Cycle Time	70		100		200		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		90		180		ns
t_{AW}	Address Set-Up to Write End	60		90		180		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		80		160		ns
t_{SD}	Data Set-Up to Write End	30		60		100		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		25		50		100	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	10		10		10		ns

Switching Waveforms

Read Cycle No. 1[10, 11]



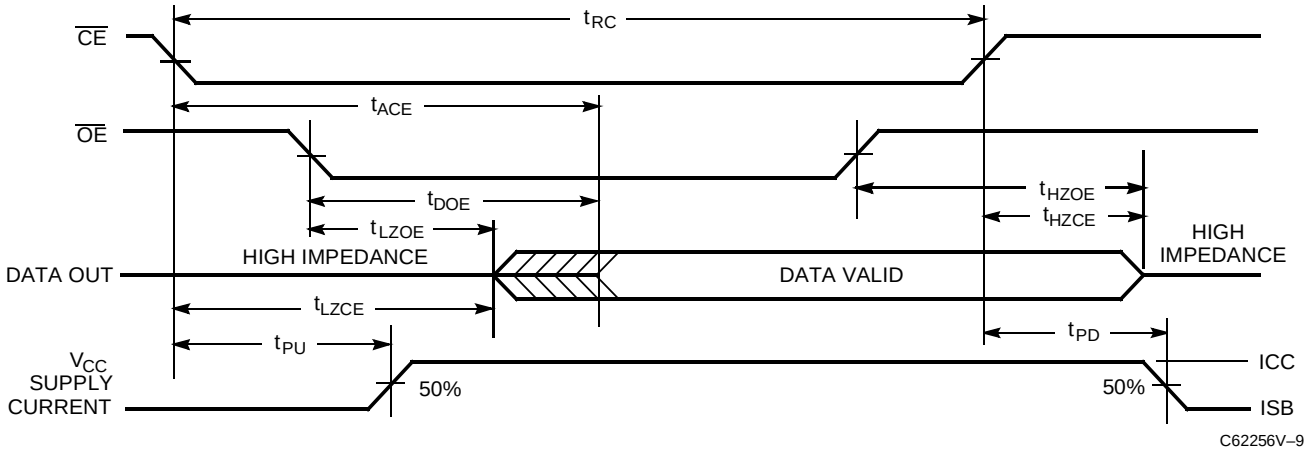
C62256V–8

Notes:

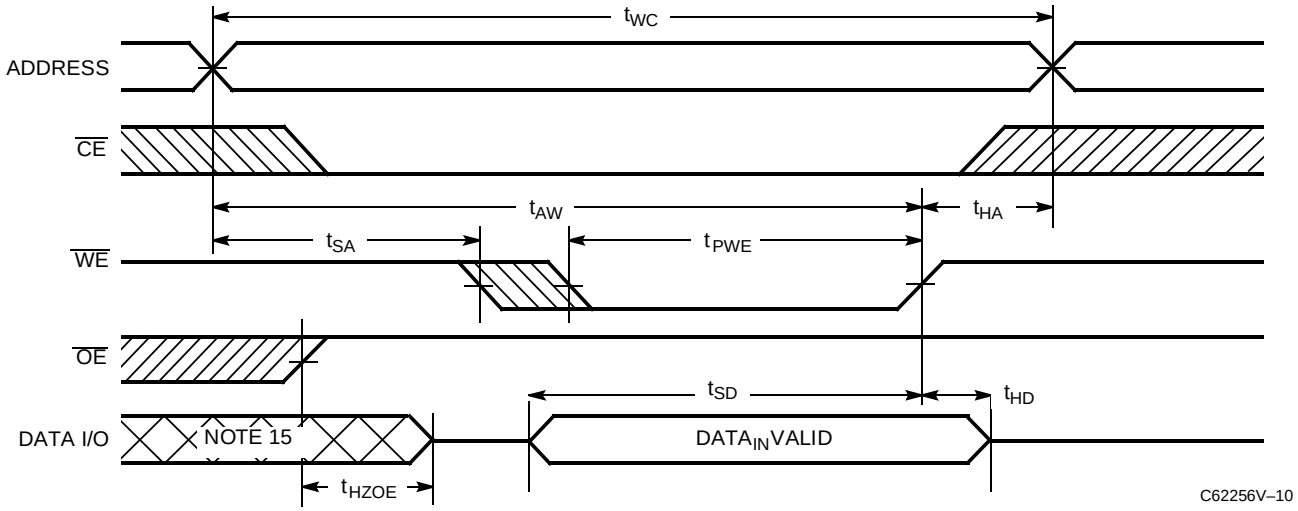
4. No input may exceed V_{CC}+0.3V.
5. Test conditions assume signal transition time of 5 ns or less timing reference levels of Vcc/2, input pulse levels of 0 to Vcc, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

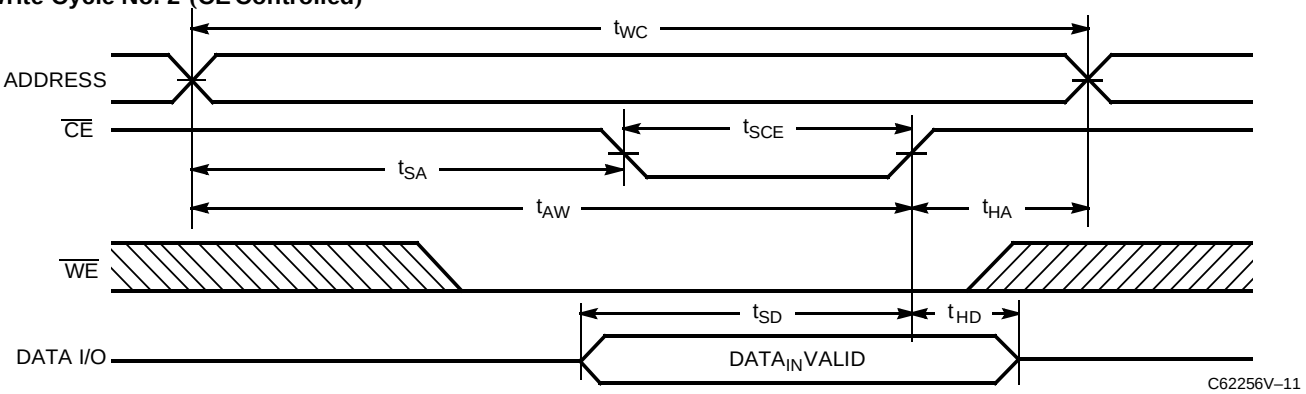
Read Cycle No. 2 [11, 12]



Write Cycle No. 1 (WE Controlled) [8, 13, 14]



Write Cycle No. 2 (CE Controlled) [8, 13, 14]

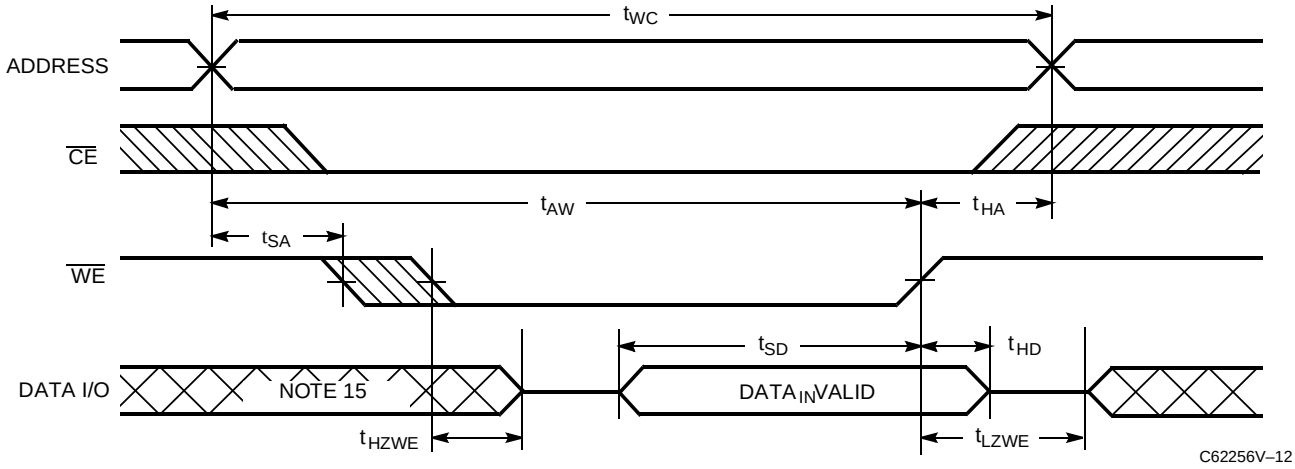


Notes:

12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

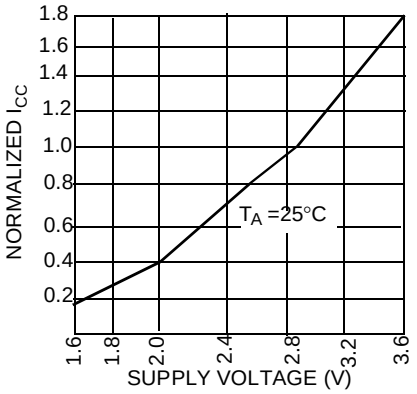
Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 14]

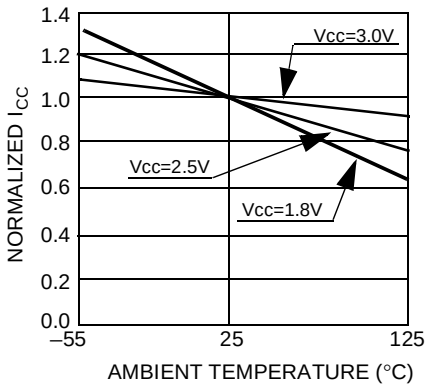


Typical DC and AC Characteristics

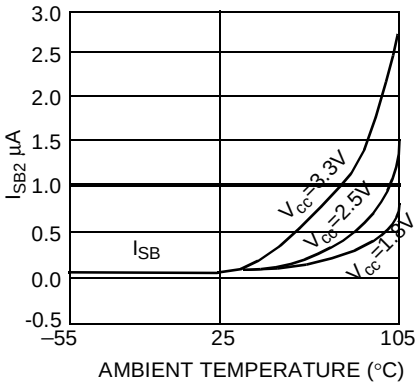
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



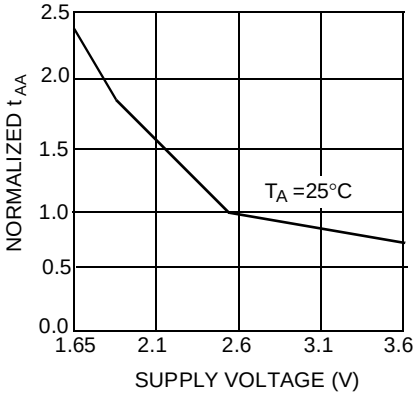
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



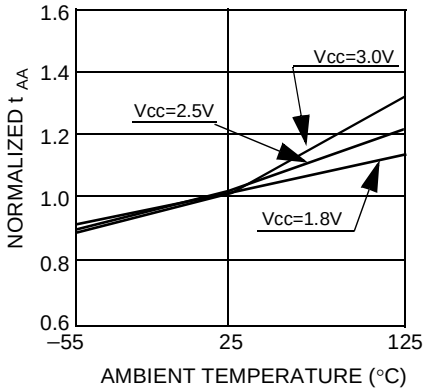
STANDBY CURRENT vs. AMBIENT TEMPERATURE



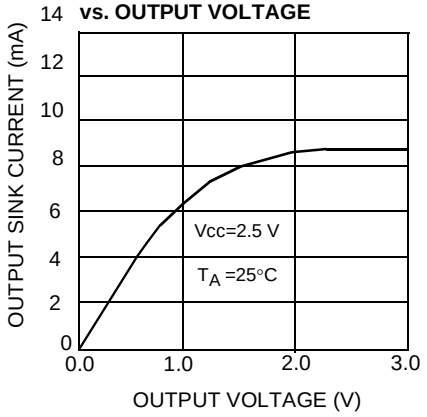
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



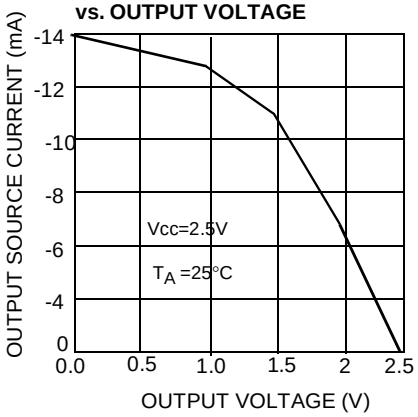
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

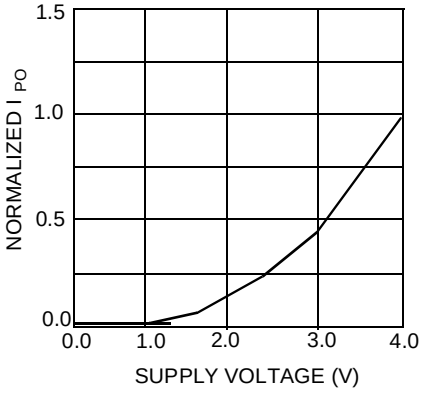


OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

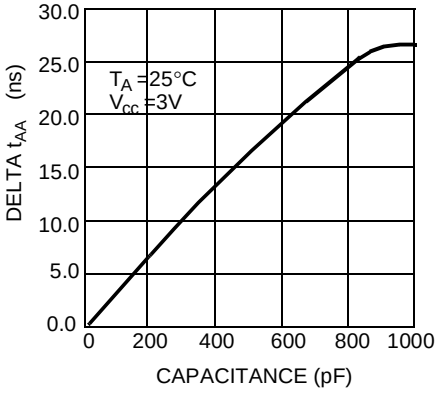


Typical DC and AC Characteristics (continued)

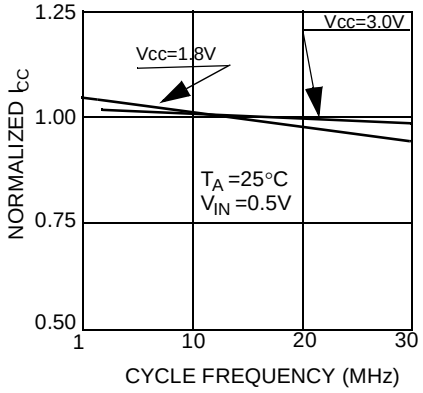
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs.CYCLE TIME



Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62256V -70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	**Commercial**
	CY62256V L-70SNC			
	CY62256V LL-70SNC			
	CY62256V -70ZRC	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V L-70ZRC			
	CY62256V LL-70ZRC			
	CY62256V -70ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256V L-70ZC			
	CY62256V LL-70ZC			
	CY62256V -70ZI	Z28	28-Lead Thin Small Outline Package	**Industrial**
	CY62256V L-70ZI			
	CY62256V LL-70ZI			
	CY62256V -70SNI	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256VL -70SNI			
	CY62256VLL -70SNI			
	CY62256V -70ZRI	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V L-70ZRI			
	CY62256V LL-70ZRI			
100	CY62256V25-100SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	**Commercial**
	CY62256V25L-100SNC			
	CY62256V25LL-100SNC			
	CY62256V25-100ZRC	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V25L-100ZRC			
	CY62256V25LL-100ZRC			
	CY62256V25-100ZC	Z28	28-Lead Thin Small Outline Package	
100	CY62256V25L-100ZC	Z28	28-Lead Thin Small Outline Package	**Commercial**
	CY62256V25LL-100ZC			
200	CY62256V18-200SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	**Commercial**
	CY62256V18L-200SNC			
	CY62256V18LL-200SNC			
	CY62256V18-200ZRC	ZR28	28-Lead Reverse Thin Small Outline Package	
	CY62256V18L-200ZRC			
	CY62256V18LL-200ZRC			
	CY62256V18-200ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256V18LL-200ZC			
200	CY62256V18L-200ZC	Z28	28-Lead Thin Small Outline Package	**Commercial**

Shaded area contains advanced information.

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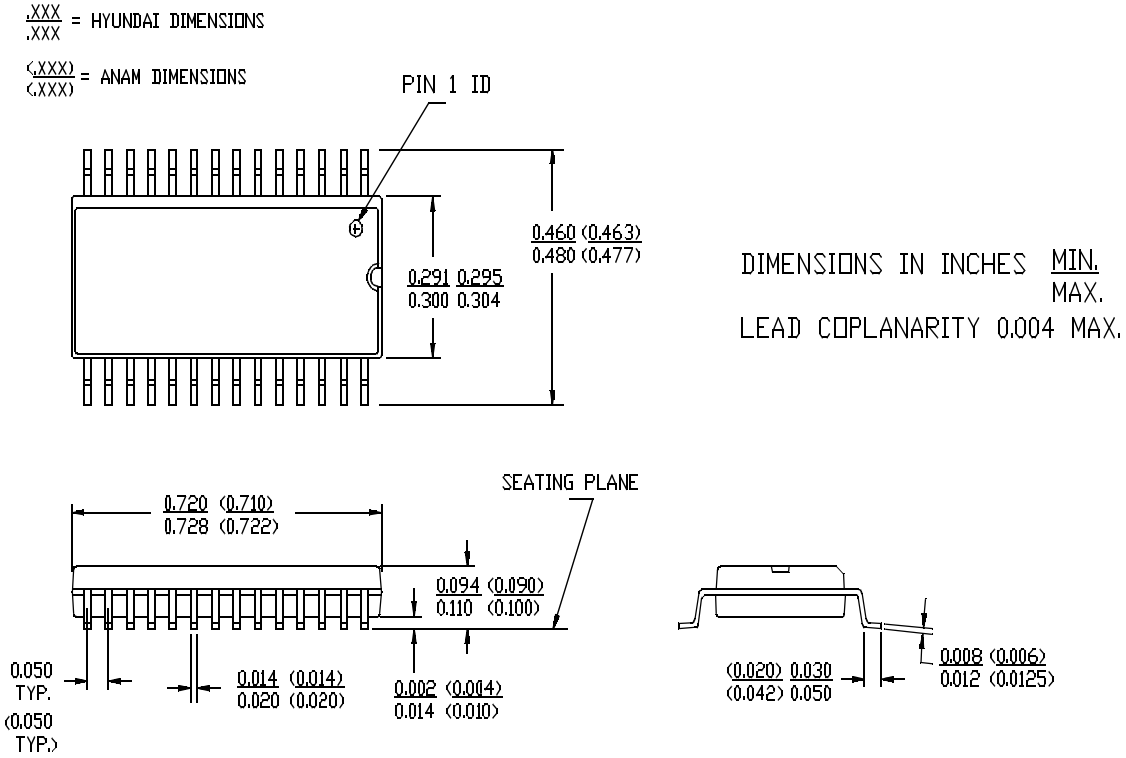
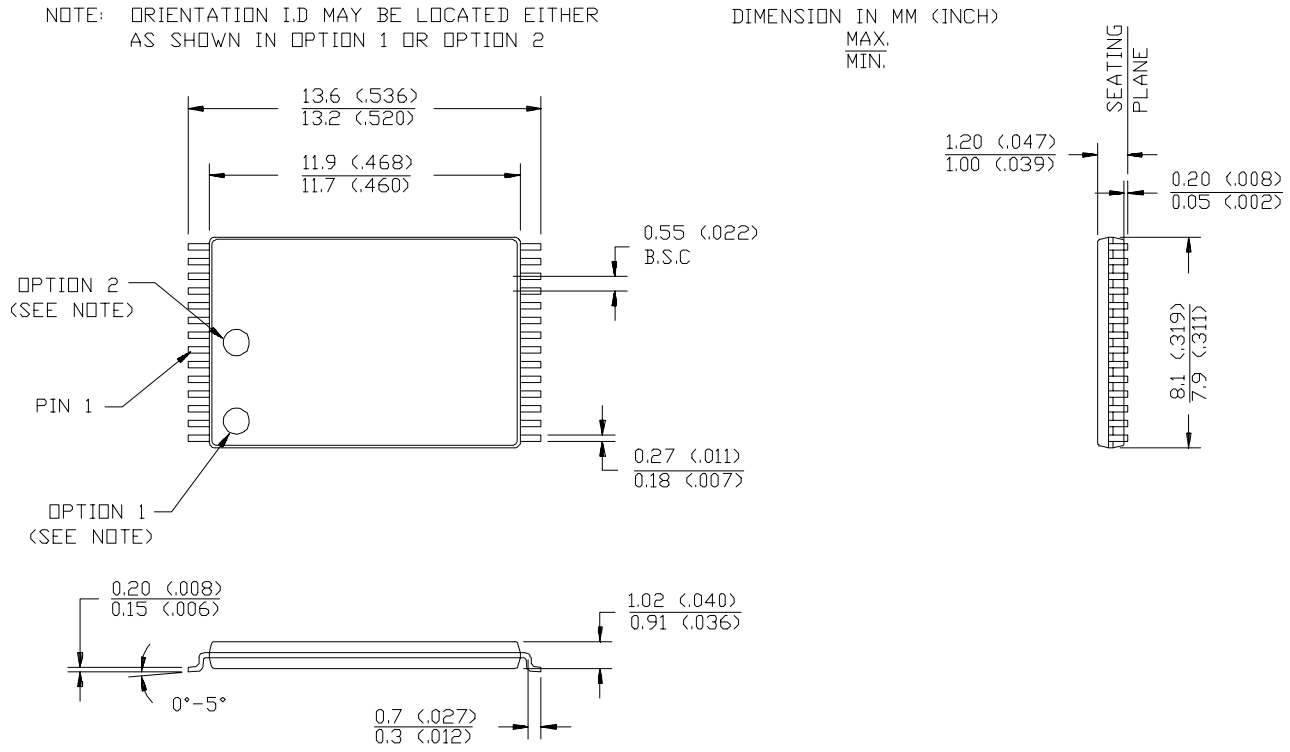
Package Diagrams

28-Lead 450-Mil (300-Mil Body Width) SOIC S22



28-Lead Reverse Thin Small Outline Package ZR28



Package Diagrams (continued)

28-Lead Thin Small Outline Package Z28