Pinout Compatibility Considerations of SRAMs

This application note discusses pinouts of SRAMs and PROMs. Included in the discussion are Motorola MCM6206D and Cypress CY7C199. Both are 32K x 8 SRAMs, but each uses a slightly different naming convention on the address inputs.

An SRAM Comparison

Most SRAMs are offered by several vendors. The data sheets of these SRAMs can vary in many ways. Some of these ways are important, like power consumption, A/C specifications, package dimensions, and pinout of critical signals. The critical signals are V_{CC}, V_{SS}, and control inputs. Other signals on the SRAM, like address and I/O, need not be numbered identically to be 100% compatible. For example, on several Cypress SRAMs, the address pin numbering is not the same as some of our competitors, yet the devices are 100% compatible.

Consider a simple example that illustrates why address pin numbering is not a problem: Assume you have a new device, the 2-bit x 4-location SRAM shown in *Figure 1*. Note that the pinout chosen by the Brand "X" 2 x 4 assigns address line 2 (A2) to pin 1, while the superior pin-out used by the Cypress device has A1 at pin 1, etc.

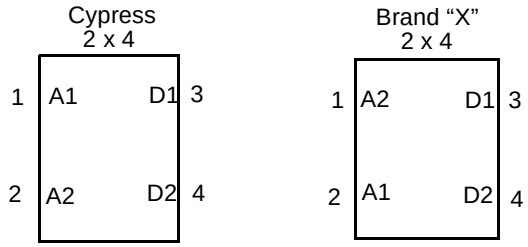

Figure 1. Example 2x4 Simplified SRAMs

Assume that your engineering staff designed a special system using Brand "X" SRAM, working only from the device's data sheet. Just as your company is about to ramp into volume production, Brand "X" sends out an End Of Life notice on the 2 x 4 SRAM.

At this point, because you have no desire to lay out a new PCB, you take a look at how the Cypress SRAMs would look in your design (*Figure 2*). In the figure, uP designates a microprocessor interfacing to the SRAM. The important thing to notice in *Figure 2* is that the data read from an address generated by the microprocessor is the same as data written to the same location earlier. With a standard SRAM, any inconsistency between the address and data line numbering does not matter because the data read is the same as the data previously written by the same processor.

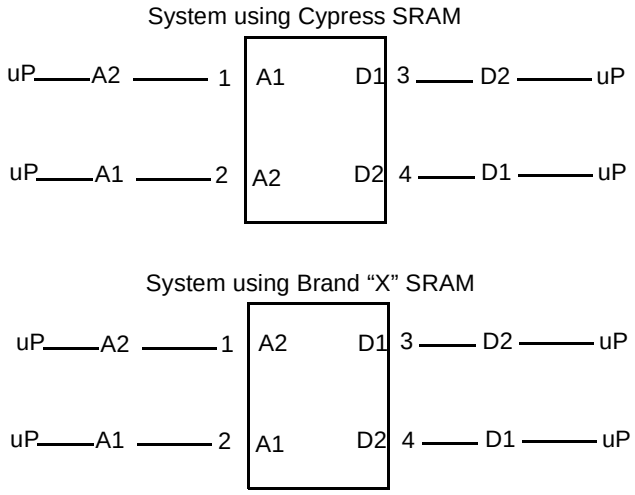

Figure 2. Example System with 2x4 SRAMs

To illustrate the point further, suppose that you write a value of 1 (uP:D1,D2 = 0,1) at location 2(uP:A2,A1 = 1,0). If you read location 2, you obtain the value 01 that was written, because the address presented to the SRAM during the read is the same as the address for the previous write. Similarly, the data read is in the same bit order as presented during the previous write to the location. So as far as the system is concerned, the two SRAM devices are identical.

Although not significant to the system, the devices could differ in where they internally store the data. In the Cypress device, the uP address of 2 (uP:A2,A1 = 1,0) could actually store the data at SRAM location 1 (Cypress:A2,A1 = 0,1). The Brand "X" RAM could physically store the data at address 2.

Because the same location is accessed for the subsequent reads, the difference in address numbering between the two devices does not matter to the system. Similarly, any numbering difference on the data lines is transparent to the system as well.

Pin Matching Example

Figure 3 shows the example of matching a Motorola MCM6206D to the Cypress CY7C199. The pinouts shown are that of a SOJ/DIP package. As described above, the addresses are scrambled differently on the Motorola and the Cypress SRAM, but the data which is written to a specific location on the Cypress RAM will be read back as the same when the same address is provided during a READ.

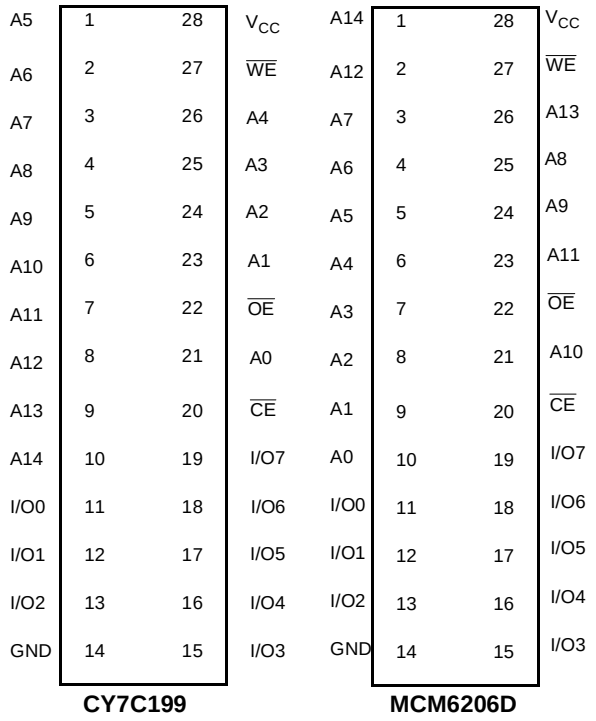

Figure 3. Pinout Comparison of MCM6206D and CY7C199

Why Have Different Addressing Names?

If the addresses used for an SRAM are irrelevant, why have different numbers or numbers at all? The reason is simple. Some customers conduct incoming tests on all integrated circuits. In order to conduct a thorough test of an SRAM, it is important to know which addresses are row and column inputs. This is important in order to conduct certain pattern sensitivity tests. Since each SRAM design is slightly different, it is important to accurately describe the function of each address input. Since Cypress (and other vendors) guarantees its SRAMs under all data sheet conditions (including all address and data patterns), this issue becomes irrelevant and a "Don't Care" for virtually all customers.

Does Address Numbering Ever Make a Difference?

Yes, for SRAMs that burst (access several memory locations with a single address), the MSB and the LSB are important in order to determine the next address in the sequence. This is relevant to Synchronous SRAMs only. To get more information on burst modes and synchronous operation, please review the application note "Understanding Burst Modes in Synchronous SRAMs."

Conclusion

The pinouts shown in the Cypress SRAM data sheets match with the block diagram shown. So the positions of the address lines may differ slightly from that of other manufacturers, but these mismatches should not matter in any application.