Third-Party Tool Support

Support for Cypress programmable logic devices is available in many software products from third-party vendors. Some companies include support for the entire design process in products that they sell. Others provide software for a portion of the design process (i.e., schematic capture, synthesis, or simulation) and interface with Cypress's *Warp*™ software tools to complete the design flow. This section will describe the design flow using these third-party software products and will describe the interface between these products and Cypress's *Warp* software.

In describing the design flow through these tools, it is useful to break the process into its major functional blocks. *Figure 1* shows these blocks. A similar figure is included for each of the third-party products, and the portions of this flow that are covered by that product are highlighted. Where applicable, the portion of the flow covered by Cypress's *Warp* software is also highlighted.

At the top of each figure are the "Text" and "Sch" blocks. These represent hardware description language (HDL) entry and schematic capture, respectively. Some tools offer design simulation at the design entry stage. This is known as "pre-synthesis" simulation, and is represented by "Simulation" block.

After design entry and simulation are complete, the design description is synthesized. The "Synthesis" block represents the translation of the design description into logic equations, and the optimization of these equations to a device architecture. The next step is device fitting, represented by the "Fitting" block. Here, the logic equations are mapped into the resources of the device. The result of "Fitting" is a file used to program the device.

The last block in the flow diagram is "Device Sim." This corresponds to simulation of the design according to its implementation in the device. Some simulators will take the timing parameters (i.e., propagation delay) of the device into account, and will provide simulation results consistent with this timing. Others will verify that the programming file is functionally consistent with the design description, but will not contain device timing information.

Finally, along the left of the diagram is the Design Flow Manager. The Design Flow Manager keeps track of the design process for the user. This module typically informs the designer which steps of the design flow have been completed and which have not. This flow manager can also be used to launch vendor tools such as *Warp* synthesis.

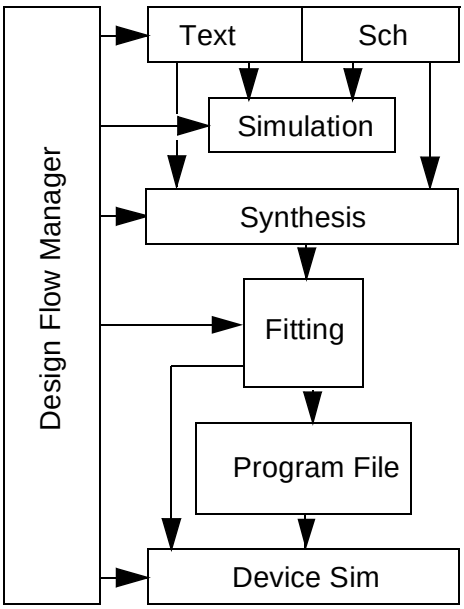

Figure 1.

Contents

Company	Product
Acugen	ATGEN
Cadence	Concept, Composer
Exemplar Logic	Galileo
Flynn Systems	FS-ATG
IsData	LOG/iC
Logical Devices	CUPL
Mentor Graphics	Design Architect
OrCAD	PLD386+
Synario Design	ABEL4/ABEL5/ABEL6
Synario Design	Synario
Synopsys	Design Compiler
ViewLogic	WorkView, PowerView

Acugen

Product

ATGEN

Device Support

Small PLDs,FLASH370i™

Input Format

JEDEC file

Required Cypress Product

Warp2®, *Warp2*Sim™, or *Warp3*®

Design Flow Description

Acugen's ATGEN software can automatically generate test vectors to be used with device programmers or with automatic test equipment (ATE) for Cypress PLDs and CPLDs. The JEDEC file output by *Warp* is read into the ATGEN software, where test vectors are generated for the design. ATGEN can output a JEDEC file with test vectors to be used on a device programmer, or a test program to be used on a tester.

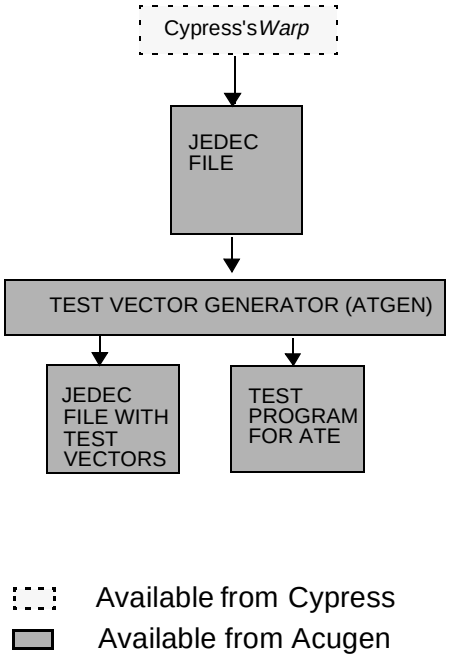

Figure 2.

Cadence Design Systems

Product

Cadence Concept or Cadence Composer

Device Support

Small PLDs, MAX340™, FLASH370i, Ultra37000™

Input Format

Schematic Entry and VHDL

Required Cypress Product

Cypress Cadence Bolt-in Kit

Design Flow Description

Both schematic and textual designs (VHDL) are supported using the Cadence Concept or Composer schematic capture tools. The *Warp* software interfaces to these tools and provides the synthesis and fitting steps of the design flow. Timing information and simulation models are then produced by *Warp* and fed back into the Cadence environment for device-level simulation. Programming files are also produced for device programming.

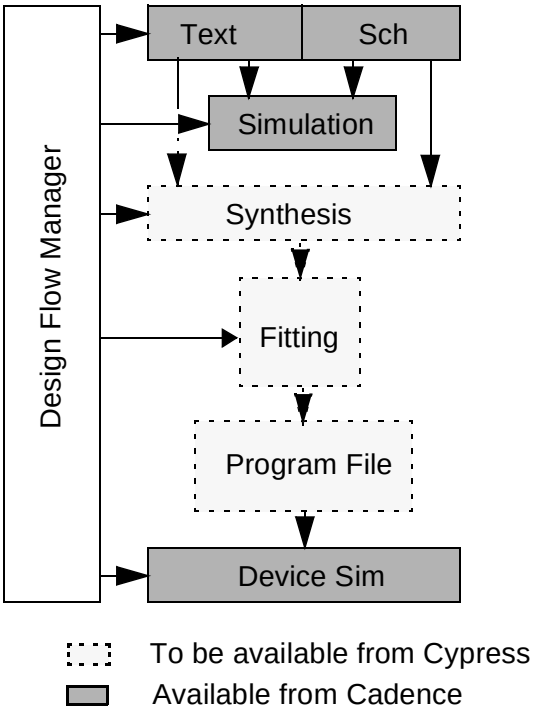

Figure 3.

Exemplar Logic

Product

Galileo

Device Support

Small PLDs, MAX340, FLASH370i, (Ultra37000)

Input Format

VHDL, Verilog, OpenABEL, Berkeley PLA, EIL, EDIF, ADL, XNF

Required Product

Warp2, *Warp2*Sim, or *Warp3*

Design Flow Description

Exemplar Logic's Galileo synthesis software accepts any of the above file formats and synthesizes the logic to any of the Cypress programmable logic devices. Galileo outputs a PLA file that can be read into any of the *Warp* tools, where device fitting and JEDEC (programming file) output occurs. Galileo can also provide timing simulation for the design once fitting has been performed.

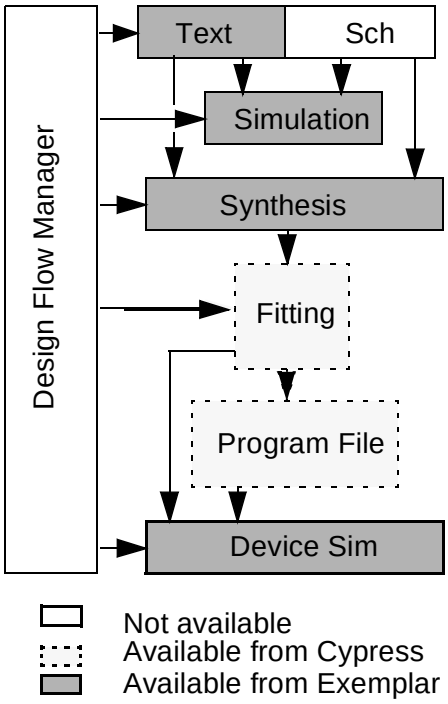

Figure 4.

Flynn Systems

Product

FS-ATG

Device Support

Small PLDs, MAX340, FLASH370i

Input Format

JEDEC file

Required Cypress Product

Warp2, *Warp2*Sim, or *Warp3*

Design Flow Description

Using FS-ATG from Flynn Systems, users can automatically generate test vectors to be used on device programmers or in-circuit testers.The JEDEC file output by *Warp* is read into the FS-ATG software, where test vectors are generated automatically. The user can enter constraints for this generator as desired. FS-ATG then outputs the JEDEC file with test vectors, to be used on a device programmer. It also outputs test vector files that can be translated for use with an in-circuit tester. This translator will take the test vectors and convert them to an automatic test equipment program.

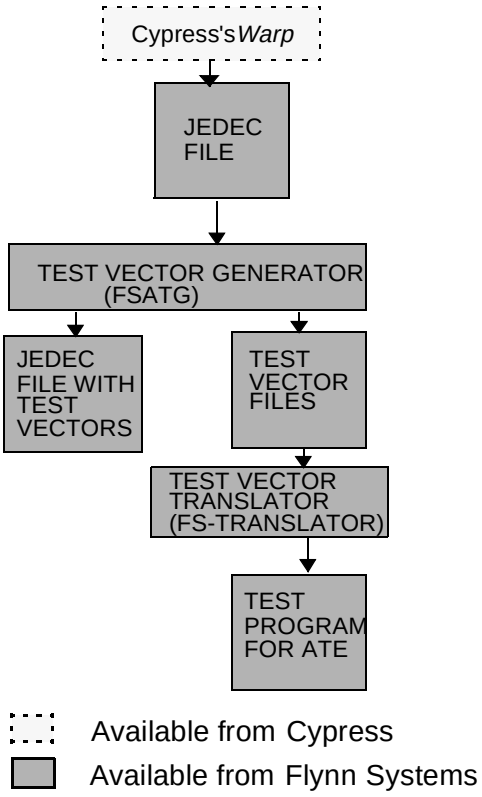

Figure 5.

IsData

Product

LOG/iC2 or LOG/iC Classic

Device Support

Small PLDs, MAX340, FLASH370i, (Ultra37000)

Input Format

LOG/iC-HDL

Required Cypress Product

Warp2, *Warp2*Sim, or *Warp3*

Design Flow Description

Design entry in LOG/iC is done using schematic capture or IsData's proprietary LOG/iC hardware description language. After design description and debugging of the source code, the design is synthesized and fit to a Cypress PLD or CPLD via the *Warp2*, *Warp2*Sim, or *Warp3* software. After synthesis and fitting, the software outputs a programming file. Simulation is also available to complete the design flow.

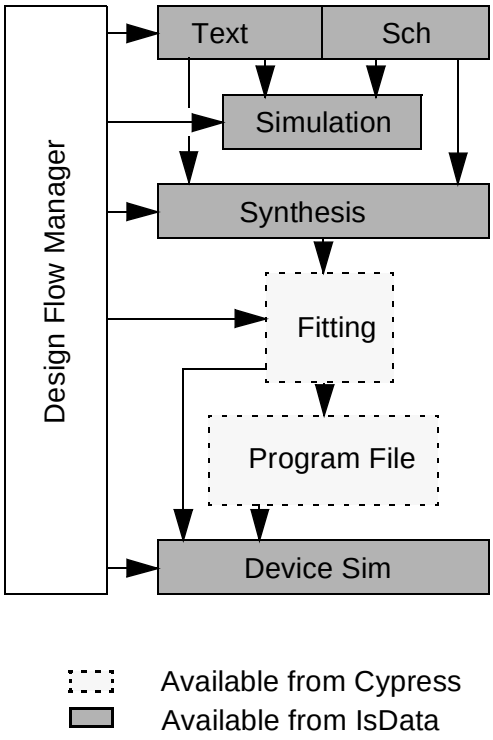

Figure 6.

Logical Devices

Product

CUPL

Device Support

Small PLDs, MAX340, FLASH370i

Input Format

CUPL-HDL

Required Cypress Product

None

Design Flow Description

Design entry is done using Logical Devices' proprietary CUPL hardware description language. Source-code simulation is used to catch design errors before the design is synthesized and fit to a Cypress device.

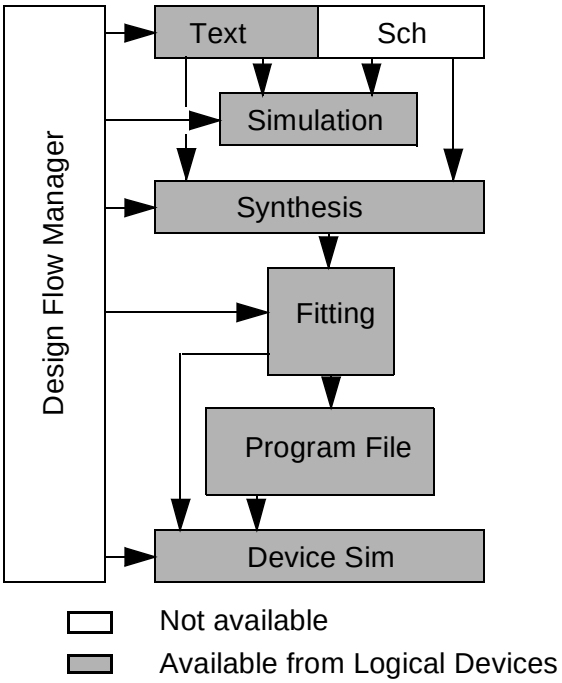

Figure 7.

Mentor Graphics

Product

Design Architect

Device Support

Small PLDs, MAX340, FLASH370i, (Ultra37000)

Input Format

Schematic Entry and VHDL

Required Cypress Product

Cypress Mentor Graphics Bolt-in Kit (CY3144)

Design Flow Description

Both schematic and textual designs (VHDL) are supported using the Mentor Design Architect schematic capture tool. The *Warp* software interfaces to this tool and provides the synthesis and fitting steps of the design flow. Timing information and simulation models are then produced by *Warp* and fed back into the Mentor environment for device-level simulation. Programming files are also produced for device programming.

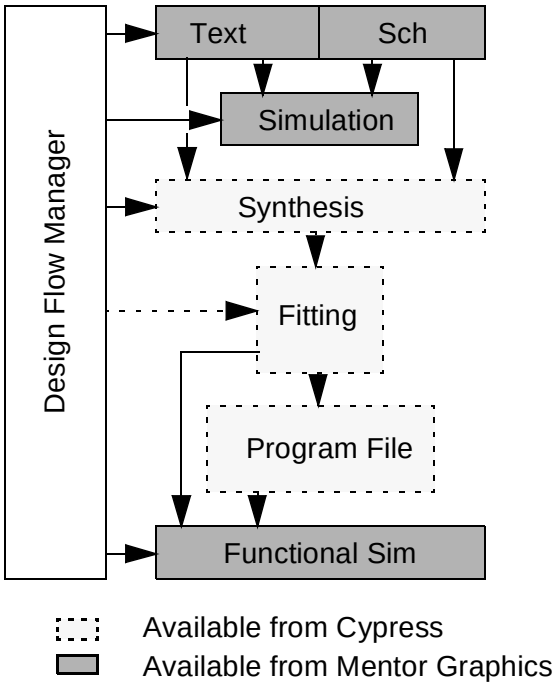

Figure 8.

OrCAD

Product

PLD386+

Device Support

Small PLDs, MAX340, FLASH370i, (Ultra37000)

Input Format

Orcad-HDL

Required Cypress Product

Warp2, *Warp2*Sim, or *Warp3*

Design Flow Description

PLD386+ interfaces to the other tools in OrCAD's design software suite to provide complete design entry, synthesis, and simulation. Designs are entered using OrCAD's proprietary design language, or by OrCAD's schematic capture software. After design description and debugging of the source code, the design is synthesized and fit to a PLD or CPLD via PLA file. PLD386+ outputs the programming file, which is also used for device timing simulation to complete the design flow.

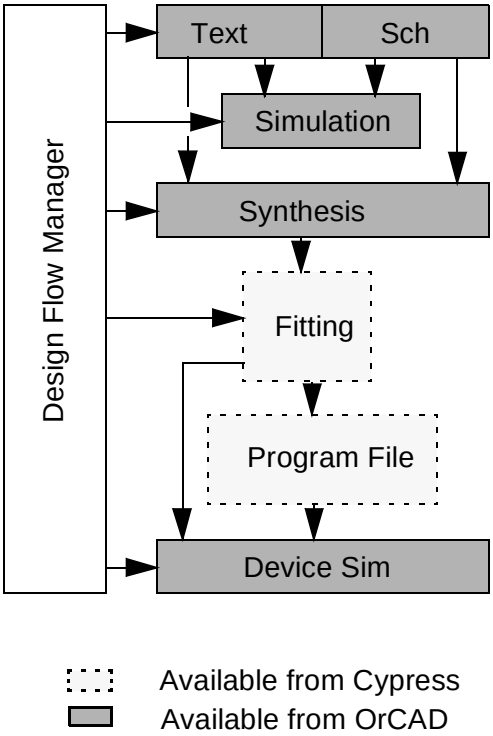

Figure 9.

Synario Design Automation

Product

ABEL4, ABEL5, and ABEL6

Device Support

Small PLDs, MAX340, FLASH370i

Input Format

ABEL-HDL

Required Product

None for Small PLDs or MAX340

Cypress ABEL Fitter Kit for FLASH370i (CY3140)

Design Flow Description

Designs entered in ABEL-HDL can first be functionally simulated using PLASIM and then go through logic optimization and minimization. The output files from ABEL will then go through fitting. The resulting output files can then be used for device-level simulation and device programming.

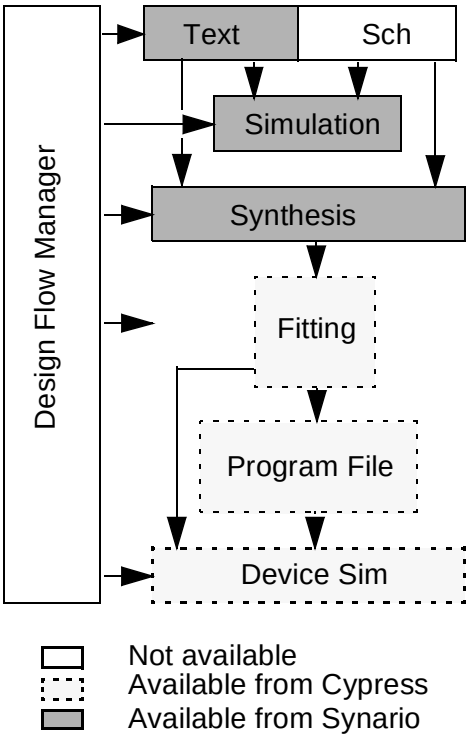

Figure 10.

Synario Design Automation

Product

Synario

Device Support

Small PLDs, MAX340, FLASH370i, (Ultra37000)

Input Format

Schematic Entry, VHDL, and ABEL-HDL

Required Product

Warp2

Design Flow Description

The user is guided through the design process by the Project Navigator. Designs can be entered in schematic entry, VHDL, or ABEL-HDL. Designs entered can be functionally simulated and then optimized by Synario. The designs will then go through fitting. The resulting output files can be used for device-level simulation and device programming.

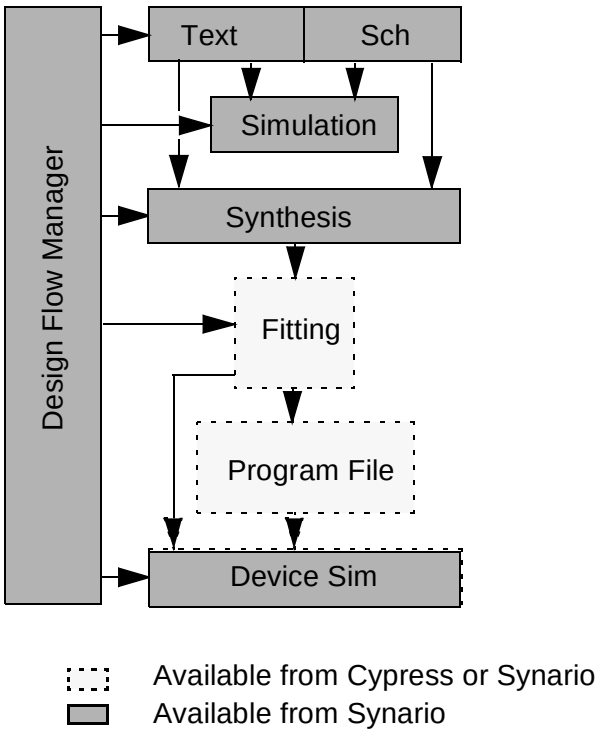

Figure 11.

Synopsys

Product

Design Compiler

Device Support

FLASH370i, Ultra37000

Input Format

VHDL and Verilog

Required Product

Cypress Synopsys Bolt-in Kit

Design Flow Description

Designs are entered in either HDL, or netlist format. It can then be functionally simulated using the VHDL System Simulator (VSS). The next step in the process is logic optimization and technology mapping. The output then goes into the *Warp* fitter, and programming and simulation files are generated for device programming and device-level simulation with VSS.

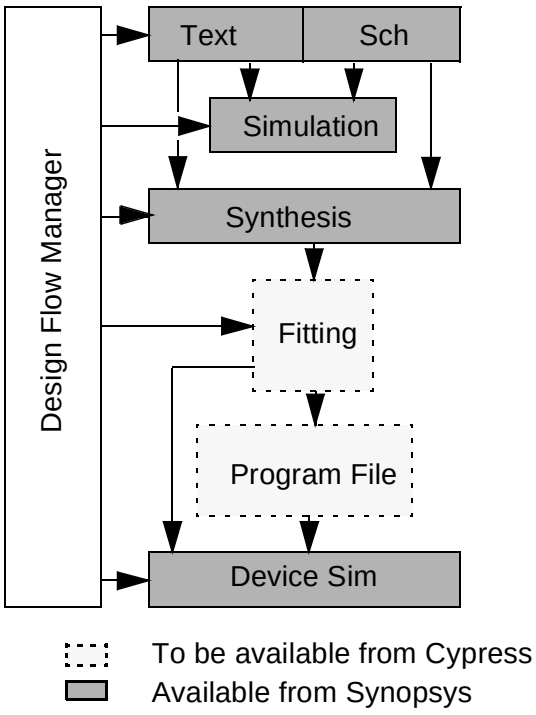

Figure 12.

ViewLogic

Product

WorkView PLUS, WorkView Office, PowerView

Device Support

Small PLDs, MAX340, FLASH370i, Ultra37000

Input Format

LPM Schematic entry, VHDL, or both

Required Cypress Product

Warp2

Design Flow Description

LPM schematics and/or VHDL files can be used for design entry. Pre-synthesis simulation is performed via SpeedWave. The design will then be exported into a VHDL file, which will go into *Warp2* for optimization and synthesis. The design will then go through fitting, resulting in a JEDEC file for device programming and timing models for device-level simulation.

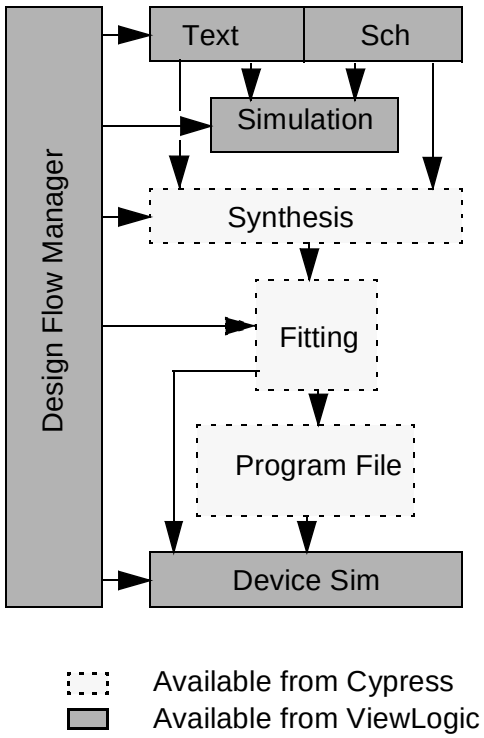

Figure 13.

Company Addresses

ACUGEN Software Inc.
427-3 Amherst Street
Suite 391
Nashua, NH 03063
(603) 881-8821

Cadence Design Systems, Inc.
555 River Oaks Parkway
San Jose, CA 95134
(408) 943-1234

Exemplar Logic
815 Atlantic Avenue
Suite 105
Alameda, CA 94501-2274
(510) 337-3700

Flynn Systems Corporation
Exit 4 Office Building
7 1/2 Harris Road
Nashua, NH 03062
(603) 891-1111

ISDATA GmbH
Haid-und-Neu-Strasse 7
D-7500 Karlsruhe 1
Germany
(0721) 69 30 92

Logical Devices Inc.
692 S. Military Trail
Deerfield Beach, FL 33442
(305) 428-6868

Mentor Graphics
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
(503) 685-8000

OrCAD
3175 NW Aloclek Dr.
Hillsboro, OR 97124
(503) 690-9881

Synario Design Automation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073
(206) 881-6444

Synopsys
700 E. Middlefield Rd.
Mountain View, CA 94043-4033
(415) 962-5000

ViewLogic Systems, Inc.
293 Boston Post Road West
Marlborough, MA 01752

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