Targeting Cypress ISR™ CPLDs with Synplify 6.0

Introduction

Cypress Semiconductor designs and manufactures a broad portfolio of In-System Reprogrammable™ (ISR™) CPLDs. The portfolio includes four major families: FLASH370i, Ultra37000, Quantum38K, and Delta39K. This application note describes how to effectively design and target all Cypress ISR CPLDs using Synplify® from Synplicity® and Cypress's *Warp*™ Release 6.0 for compilation, synthesis, and fitting.

Synplify

Synplicity's Synplify 6.0 will be used to synthesize the user's HDL (VHDL or Verilog) and target all Cypress CPLDs. The result is a VHDL structural netlist with a .vhn extension, which is brought into *Warp* for optimization and fitting. The steps involved in synthesizing a VHDL design called “cypress.vhd” are outlined below:

1. Invoke Synplify from the start menu by selecting Start/Programs/Synplicity/Synplify (*Figure 1*).
2. Create a new project by selecting File/New and select “Project”.
3. Add the HDL source file containing the design by clicking “Add” and browsing to the desired directory.

Figure 1. Synplicity After Step 3

4. Select the directory for the compilation results.
5. Set the result file using Change button next to the Result File label (in *Figure 1*). This will open up a new dialog box and create a VHDL structural netlist with a .vhn extension (*Figure 2*).
6. Type “cypress” in the File Name field and click OK
7. Click on the “Change” button next to the Target label (in *Figure 1*). This will open up a new dialog box (*Figure 3*).

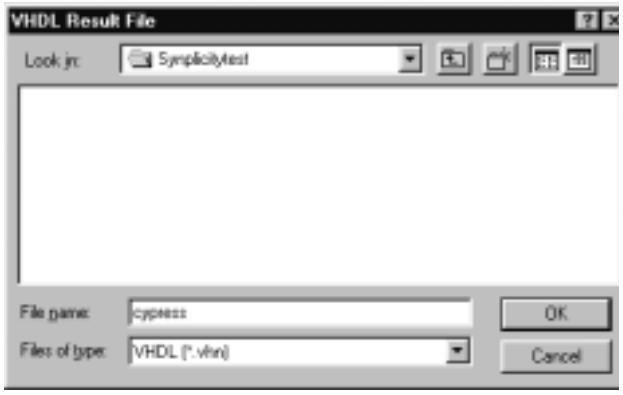

Figure 2. VHDL Result File Dialog Box

8. Select the Cypress family you want to target (Delta39K in this example). You can use the pull down menu to select other families (*Figure 3*).
9. Click Ok. This will take you back to *Figure 1*.
10. Click Run. If there are errors, these are reported and can be viewed in the log file. Otherwise you are done. All errors must be corrected in Synplicity and a netlist must be generated prior to proceeding to *Warp*.

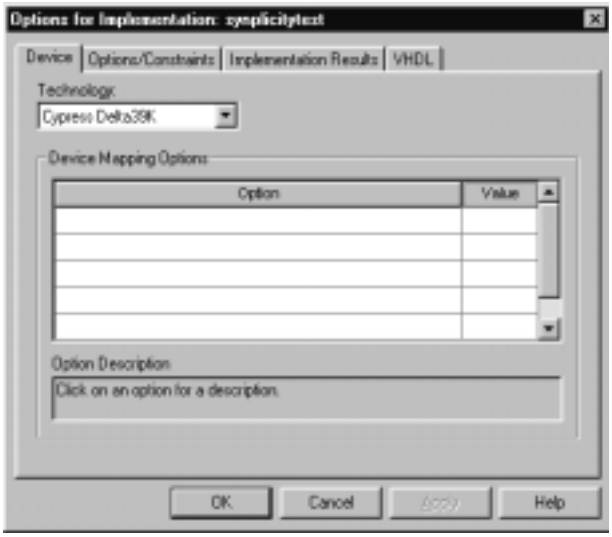

Figure 3. Options for Implementation Dialog Box

Warp

The steps involved in fitting the synthesized VHDL netlist (cypress.vhn) to a Cypress CPLD are outlined below.

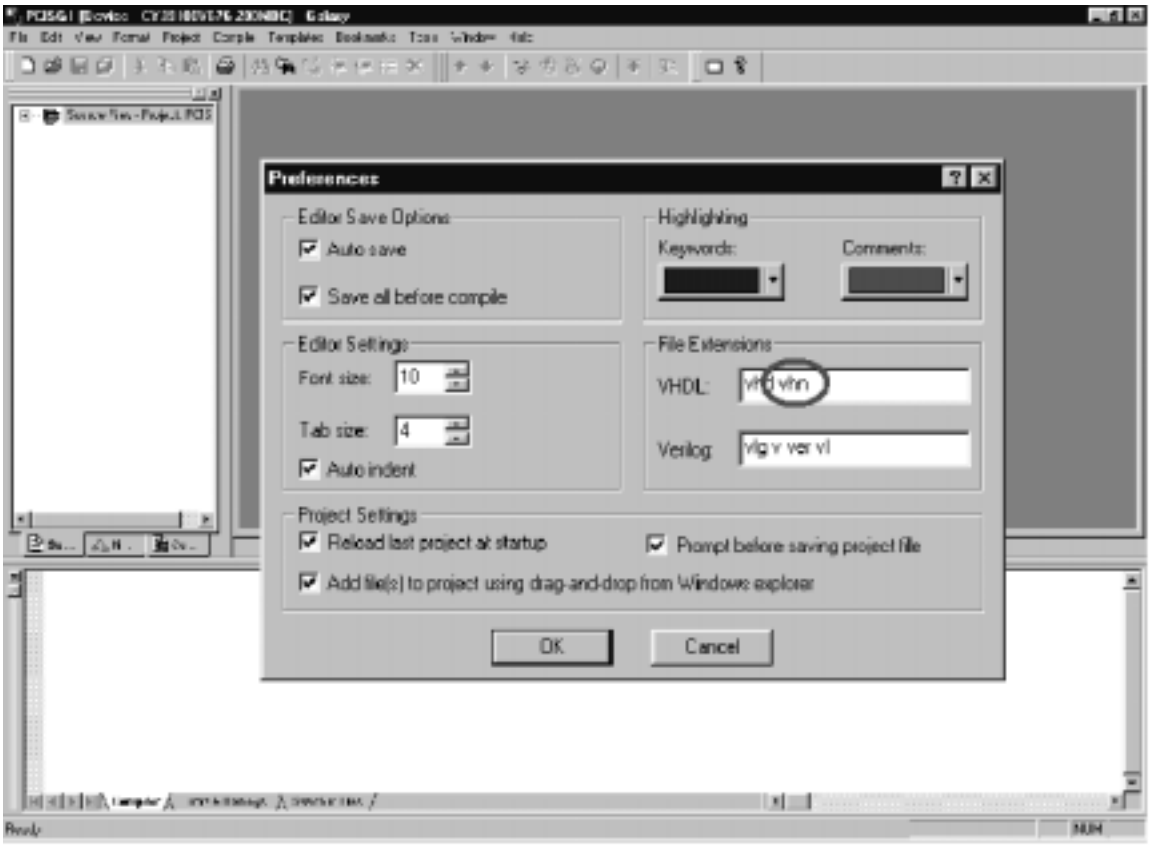

Figure 4. The Preference Dialog Box

11. Invoke *Warp* from the Start menu by selecting Start//Programs/*Warp* R6.0/Galaxy (*Figure 4*).
12. Select Edit/Preferences. Add the .vhn file extension to the VHDL field and click OK.
13. Select File/New (*Figure 4*). This will open up a new dialog box (*Figure 5*).

Figure 5. Starting a New Project Dialog Box

14. Select “Project [Target - Device]”, then click OK (*Figure 5*). This will open a new dialog box (*Figure 6*)
15. Select project type as VHDL (*Figure 6*). Note that even if you used Verilog for your design, since the Synplify output is in VHDL you must always select VHDL as the project type for *Warp*.

Figure 6. Project Information Wizard Dialog Box

16. In the Project Name dialog box, enter project name. “Synplicity” is chosen for this example.
17. In the Project Path dialog box, browse to the directory for your *Warp* project. All HDL files should be created and maintained in this directory.
18. Type “C:\Synplicitytest” and click next.
19. Click on “Browse” to find the .vhn file that you want to use in your project.

20. Add the vhn file to “Files in project directory” by clicking “Open” once you have selected the file.
21. Add the .vhn file to “Files in the Project” by highlighting the file and clicking Add (*Figure 7*).

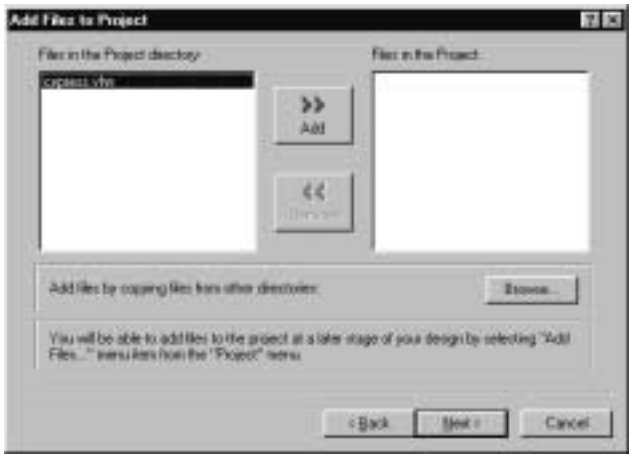

Figure 7. Add Files to Project Dialog Box

22. Click Next.

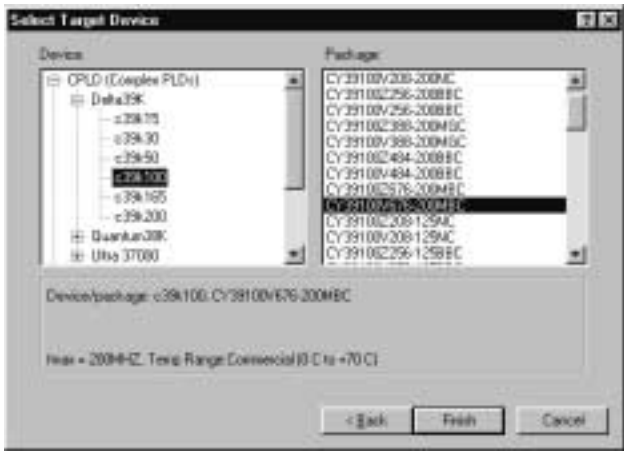

Figure 8. Select Target Device Dialog Box

23. Select a target device as shown in *Figure 8*. In the example, we chose a 100K gate (1536 Macrocell) 7.5-ns Delta39K CPLD in a 676-ball Fine-Pitch Ball Grid Array Package. Click on Delta39K, select “c39k100” in the left frame and “CY39100V676-200MBC” in the right frame, then click Finish.
24. Click Yes to save the project. This will take you back to Figure 4.
25. To compile the project Select Compile/ Project (*Figure 4*) or select the  button. A comprehensive report file of compilation, fitting, utilization and timing can be reviewed under View/Report File. The report file is broken up into 3 sections: Equations, Pinout and Timing. More information regarding the Report File can be found in the electronic documentation package included with *Warp*. Select Help/Help Topics/Contents/User's Guide/Report File for more information on the report file.
26. If satisfied with the result, you are done. Otherwise change your design or the Synplify synthesis parameters and repeat the Synplify compilation to generate a new .vhn file. Then recompile the project with the new .vhn file.

Additional Information

For more information on Cypress CPLDs, please visit the Cypress website at http://www.cypress.com/pld or contact your local sales representative. The website contains application notes, HDL reference designs and data sheets on Cypress products.

Further information on Synplify can be found at http://www.synplicity.com.