Targeting Cypress PLDs from the Cadence Environment

Introduction

The Cadence bolt-in kit is a software program that interfaces the Cadence Concept tool with *Warp*™ so that designs created in the Concept design environment can be targeted to Cypress PLD devices. The kit includes a CD containing the bolt-in software, a User's Guide in PDF format, and a CD containing the *Warp2*® software. The Concept bolt-in kit supports all of the Cypress programmable logic devices.

Design Flow

The design flow for targeting designs to Cypress programmable logic devices can be subdivided into three major stages. These stages are:

- design entry
- synthesis and fitting
- simulation

These stages are shown in *Figure 1*.

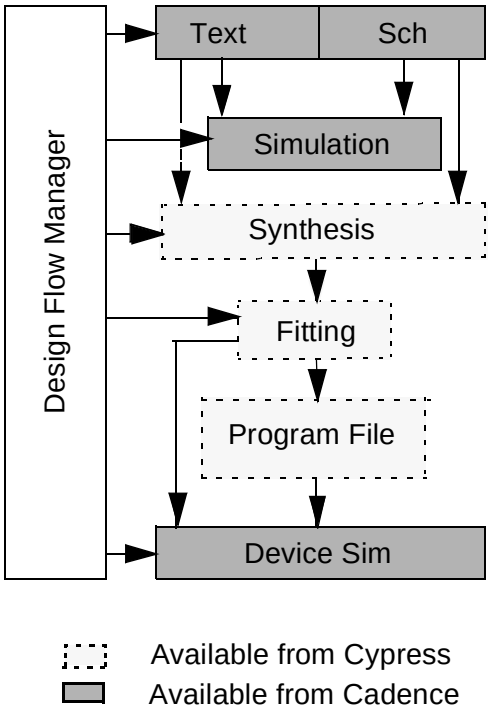

Figure 1. Cypress Cadence Design Flow

The first step in the design process is the creation of a schematic or multiple schematics in Concept using the Cypress schematic symbol library. The kit supports mixed-mode designs whereby VHDL modules can be represented by user-defined symbols in Concept. The top level schematic sheet is exported as an EDIF200 netlist and converted to an IEEE 1164 compliant VHDL file by the edif2vhdl utility included with the Cadence Concept bolt-in kit. The design can also be simulated before synthesis with the Cadence Leapfrog Simulator if the user owns the tool.

The next step is synthesis and fitting. The VHDL output of edif2vhdl is imported into *Warp*, the Cypress VHDL development system. *Warp* is a fully integrated IEEE VHDL compliant EDA tool with a user-friendly graphical user interface (GUI). The design can be compiled, synthesized, and targeted to any of the Cypress programmable logic devices. *Warp* provides the best performance results, both in area and speed, for all designs targeting Cypress programmable logic devices.

The final step is simulation after synthesis and fitting. *Warp* generates VHDL, Verilog, and EDIF netlists for various simulators. Cadence Leapfrog VHDL, Verilog-XL, and LMG SmartModels support is available for all the Cypress programmable logic devices.

Getting Started

Installation

Installation of the bolt-in software and the *Warp* software is straightforward. The installation script of the bolt-in software installs and compiles the Cypress library of components along with the pre- and post-synthesis simulation libraries. Once installed, the Cypress components will not need to be recompiled. A few lines need to be added to the .cshrc file to set environment variables.

Design Project Setup and File Management

You must have a design directory with configuration files set up before the Concept tools will work correctly with your design. Cypress provides the mkprojdir utility to automate the set-up of design directories for new designs. *Figure 2* shows the hierarchy of the files in a typical project.

A typical project has five directories under the design directory that the script creates. These directories are named projlib, rundir, work, ieee, and cypress. The projlib directory stores the VHDL entity, architecture and package files. The rundir directory is the directory from which the Concept tool is invoked. The rundir directory holds Concept design entry files, *Warp* synthesis and fitting files, Leapfrog pre- and post-synthesis simulation files, and post-synthesis Verilog-XL simulation files. The work library is the working directory for Leapfrog VHDL simulation. The IEEE and Cypress libraries hold the library of fixed components. These components such as counters and multiplexers are optimized to fit well into Cypress programmable logic devices.

Design Methodologies

There are two basic approaches to a hierarchical schematic design, a bottom-up and a top-down approach. In a bottom-up approach, the lower-level schematics are developed first, then the top-level schematic is created with the lower-level schematics added as components. The lower-level files can be either VHDL files or schematic files. VHDL de-

signs are either created within the Concept environment or copied into the project if they already exist.

In a top-down approach, the top-level schematic is created first with blocks drawn to represent lower-level VHDL or schematic files. Then the lower-level files are created. The lower-level can be either a VHDL or a schematic file. The entity and architecture component files for a VHDL design can be created using the editor or copied into the project if they already exist.

The Cadence Concept bolt-in kit's User's Guide contains six tutorials that demonstrate multiple ways to design targeting Cypress devices. These tutorials cover both the top-down and bottom-up approach to design. They also include pure schematic and VHDL along with mixed-mode designs. The tutorials walk you through the different Concept tools that work most effectively with your type of design.

Adding Synthesis Properties to Schematics

Warp supports a number of synthesis directives to control many aspects of synthesis. These directives include assigning pin numbers and part numbers, selecting optimization for speed or area, assigning power consumption levels at the logic block level, directing the slew rate of output pins, and many others. These directives are attached to the bus or wire, a symbol, or the top-level sheet.

Fitting and Synthesis

Warp, a VHDL based development system, is the synthesis engine for the Cypress Cadence Concept bolt-in kit. Therefore, the schematic created in Concept needs to be converted into VHDL code that can be synthesized in *Warp*. An EDIF200 netlist is automatically extracted by Concept. The user will then run the EDIF2VHDL tool from the design flow manager to convert it into VHDL. The resulting VHDL file is written to the sub-project directory “rundir”.

The *Warp* software is invoked by clicking on the Galaxy button on the Concept GUI. Galaxy is the graphical user interface for *Warp*. The default name for a new *Warp* project file is warp.wpr. In the Galaxy *Warp* project window, add the VHDL file to the Galaxy project. Use the “set top” button to select the top-level file. Select a Cypress programmable logic device to target with the design. Click on the “smart” compile button to compile and fit your design to the selected device. The resulting files are a JEDEC programming file and a report file. See the *Warp* documentation for more details.

Simulation

The only pre-synthesis simulator that the Cadence Concept Bolt-in Kit supports is the Cadence Leapfrog VHDL simulation environment. The pre-synthesis simulation library of Cypress devices is provided with the Cadence bolt-in kit. The library only needs to be compiled once at installation. Instructions are given in the User’s Guide of the Cadence bolt-in kit.

The Cadence Concept Bolt-in Kit supports both the Cadence Leapfrog VHDL and the Verilog-XL simulation environments among other third-party simulators for post-synthesis simulation. The post-synthesis simulation library for Cypress devices is also part of the Cadence bolt-in kit. This library also needs to be compiled only once during installation.

Sales and Technical Support

The Cypress bolt-in kit can be purchased through your local distributor or local sales office. You can also contact the Cypress Applications Hotline by sending an e-mail to pldsupport@cypress.com or by calling (408) 943-2821. You can get 24-hour support from our web site at http://www.cypress.com. The web site contains the latest information on our company, its products, technical support, application notes, white papers, Frequently Asked Questions (FAQs), and data sheets.

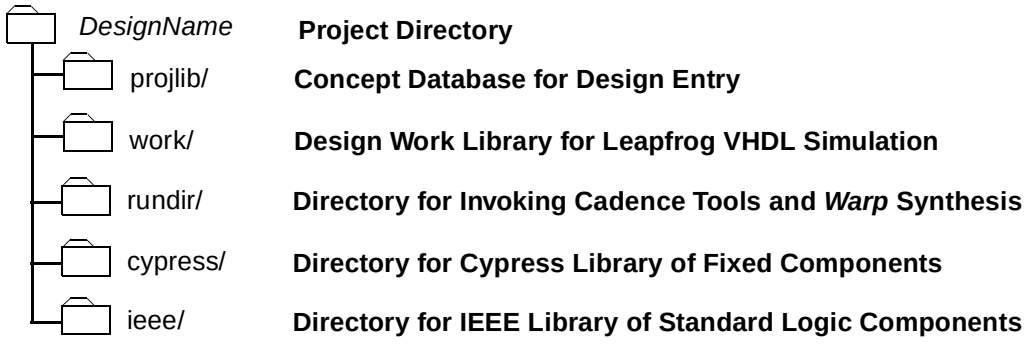

Figure 2. Directory Structure for a Typical Design