Targeting Cypress PLDs from the Leonardo Spectrum Environment

Introduction

The Exemplar Logic bolt-in software interfaces Exemplar Logic's Leonardo Spectrum with Cypress's *Warp*™ software. Designs created in Leonardo Spectrum can be targeted to Cypress PLD devices. The Cypress Exemplar Logic design flow allows you to take advantage of Exemplar Logic's powerful Leonardo Spectrum HDL synthesis tools, Cypress's automatic fitting software, and a wide variety of timing simulators.

Note: In this application note, *Warp2*® release 5.1 and Leonardo Spectrum version v1998.2d were used.

Design Flow

The Cypress Exemplar Logic design flow is shown in *Figure 1*.

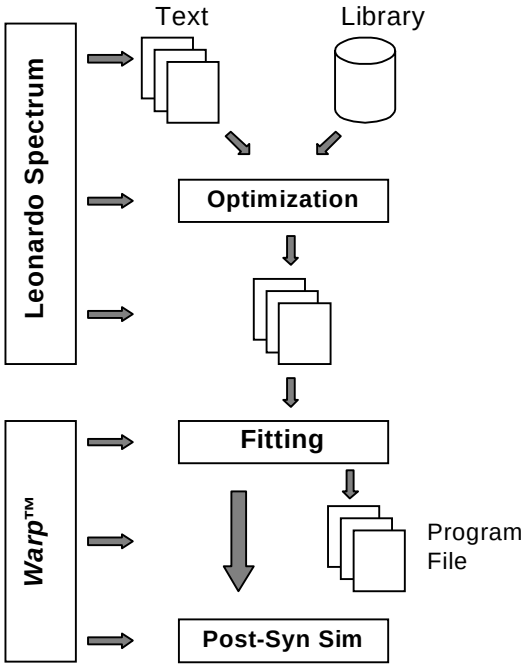

Figure 1. Cypress Exemplar Logic Design Flow

The flow starts with design entry and synthesis in Leonardo Spectrum. The output is a VHDL netlist, which *Warp* then fits into a Cypress PLD. *Warp* generates a file for device programming, and VHDL or Verilog timing models are generated for post-synthesis simulation.

Leonardo Spectrum

Exemplar Logic's Leonardo Spectrum uses flow tabs to guide users through the synthesis process. Additionally, process wizards lead users through the design flow. The three main tabs used while targeting a Cypress device are Technology, Input, and Output.

Technology

In order to perform synthesis using the Cypress libraries, you need to first select the Technology tab, as shown in *Figure 2*.

Figure 2. Loading the Cypress Library

There are two technology choices, ASIC and FPGA. CPLDs are listed by vendor under the FPGAs heading. Selecting Cypress will provide a choice of device families. Version v1998.2d supports both the FLASH370i™ and the Ultra37000™ families. After choosing a family, a pull down menu will appear for selecting the specific part. Finally, click on LOAD LIBRARY to complete the targeting of Cypress devices.

Input

The next step will be to load the design file. Select the Input tab, as shown in *Figure 3*.

Use the icon to the right of "Working Directory," to set the directory for your project. Next, click on the folder icon beneath it to add your design files. Exemplar supports

Figure 3. Input of Design Files

Figure 4. Configuring the Output File

IEEE-compliant VHDL or Verilog, EDIF, and XNF files. All files opened will appear in the “open files” window.

Finally, click on READ to have the software read the code and report any warnings or errors.

Warning: Before creating an output file, the design must first be optimized. This step can be done from within the Optimization tab. Without optimization, the resulting output file will not be complete and cause errors in *Warp*.

Output

The final step in targeting a Cypress device involves configuring the output file. Select the Output tab, as shown in *Figure 4*.

Under Format, choose VHDL. Then, give the output file a name, making sure that it has the .vhd extension.

Note: If your source file happens to be in VHDL, the software will automatically name the output file differently from your source file to avoid it being overwritten. The naming convention involves adding “_1” to the name of the file.

Version v1998.2d supports the use of a package to declare the instantiated component and the use of the explicit component name (library.package.name). Since this change in implementation of VHDL constructs is currently not compatible with *Warp*, it needs to be disabled. To turn this feature off, the Leonardo Spectrum variable

vhdl_write_component_package

can be set to false. There are several ways to set a variable:

1. Level 3: in the transcript window, type:

   set <variable name> <value>

2. Level 3 and 2 GUI: in the main window, Tools -> Variable Editor, select the variable from the list, type in the appropriate value, then hit Apply, then OK. You may need to select “Show Advance Variables.”

3. Level 3 and 2 command line option:

   set_var <variable name>=<value>

Click on WRITE to complete the synthesis of the design.

Warp

Modifications

For Solaris, before compiling in *Warp*, run the process_vhd script on the VHDL output netlist of Leonardo Spectrum. For example, if the VHDL output netlist from Galileo is called my_design.vhd, then type:

process_vhd my_design.vhd

This script fixes a minor bug that exists in the VHDL output netlist produced by the current release of Leonardo Spectrum. This bug fix consists of changing the port of TRIDATA from OUT to INOUT. When this bug is corrected in their future releases, it will no longer be necessary to run this script.

Note:

1. Note that an explanation of how to obtain all files mentioned here can be found in the Installation section.

On the PC, the user will need to edit the output VHDL file manually by searching for the line with TRIDATA and changing its port from OUT to INOUT.

Fitting

The *Warp* does not need to be created in the same directory as the Leonardo Spectrum files. Add the exported VHDL netlist to the project; a copy will then be placed in your *Warp* project directory. Even though the design was targeted to a device in Leonardo Spectrum, you will need to set up the target device again in *Warp*. *Warp* automatically fits the design into Cypress PLDs.

Post-synthesis Simulation

Warp outputs a variety of VHDL and Verilog timing simulation models. You can verify the timing and functionality of your design using your choice of any supported VHDL or Verilog simulator.

Programming

Warp generates JEDEC programming files for all Cypress devices which can be used for in-system reprogramming (ISR™) or with various device programmers.

Installation

Please note that you must have *Warp* already installed and set up on your system before you can install the Exemplar Bolt-In software.

For Unix:

1. Untar the file cyp_el.tar using the following UNIX command:

   tar -xvf cyp_el.tar

   This will create a directory called cyp_el under the current directory.

2. Run the installation script from the cyp_el directory. The installation script should automatically install the Exemplar Logic library into your existing *Warp* directory.

   Note: You might have to set the execution permission of the installation script el_install before you can run it.

3. Put the script file process_vhd in your search path.

For PC:

1. Assuming that your existing *Warp* installation is in C:\WARP, copy the files EL_GATES.VHD and EL_PKG.VHD to C:\WARP\LIB\COMMON
2. Edit the file

   C:\WARP\LIB\COMMON\ORDER

   by attaching the following two lines to the end of that file:

   EL_GATES.VHD STDLOGIC

   EL_PKG.VHDSTDLOGIC
3. Create a temporary directory on the C: drive, for example WARP_TMP.
4. The final step is to compile the library files. Run the following command from the WARP_TMP directory:

   C:\WARP\BIN\WARP.EXE -q -a -d c371

Support

The Exemplar bolt-in software can be obtained from

http://www.cypress.com/design/support/sw/thirdparty/exemplar.html

For technical support, you can contact the Cypress Applications Hotline by sending an e-mail to pldsupport@cypress.com or by calling (408) 943-2821. You can get 24-hour support from our web site at http://www.cypress.com. This web site is frequently updated with product information, technical support, application notes, white papers, Frequently Asked Questions (FAQs), and data sheets.

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