Targeting Cypress PLDs from the Synopsys FPGA Express Environment

Introduction

With the release of version 3.0, Synopsys FPGA Express has the capability to synthesize designs and output netlists targeted to the Cypress FLASH370i™ and Ultra37000™ families of CPLDs. With the use of Cypress *Warp*™ software, these netlists can then be used to fit designs to Cypress devices. To target a Synopsys FPGA Express design to a Cypress device, no extra software, libraries, or bolt-in kits are required. The basic FPGA Express software that is sold by Synopsys is all that is needed.

Design Flow

The *Warp*/FPGA Express design flow is shown in *Figure 1*.

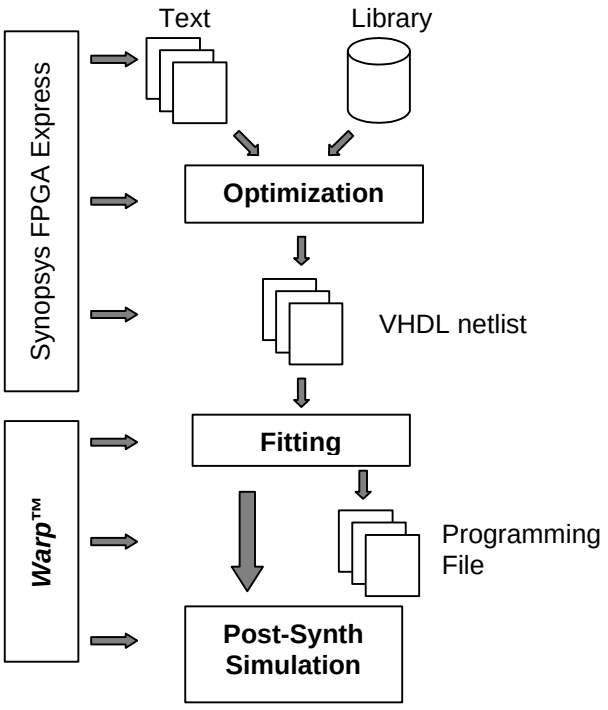

Figure 1. Warp/FPGA Express Design Flow

The flow starts with design entry and synthesis in FPGA Express using either VHDL or Verilog. The output is a VHDL netlist, which *Warp* then fits into a Cypress PLD. *Warp* generates a file for device programming, and VHDL or Verilog timing models can be generated for post-synthesis simulation.

The process from beginning to end can be broken into five steps: creating a project in FPGA Express; targeting the design to a Cypress device in FPGA Express; outputting the netlist from FPGA Express; creating a project in *Warp*; and compiling, synthesizing, and fitting the design in *Warp*.

Creating a Project in FPGA Express

When targeting a Cypress device, the creation of the project is done in exactly the same way as any other FPGA Express project. There are no Cypress-specific steps which you will need to take at this point.

Targeting the Design to a Cypress Device

Once the source code can be updated without errors, the design can be targeted to a Cypress device. Under the *Synthesis* menu, choose *Options*. This will bring up the Options dialog box as seen in *Figure 2*.

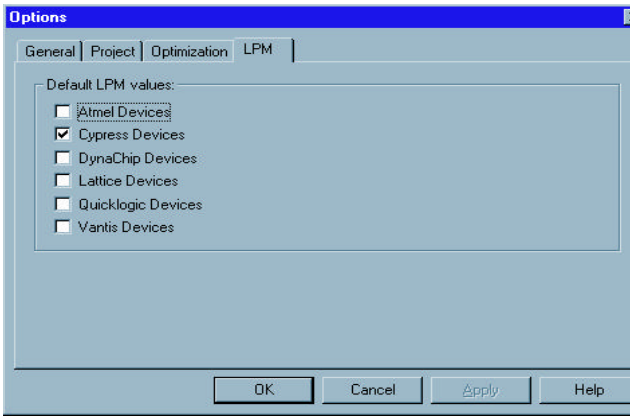

Figure 2. Options Dialog Box in FPGA Express

Using the Options dialog box, you can choose various settings which will determine how the design is synthesized. Most of these options are a matter of personal preference. The setting which directly pertains to Cypress designs is under the LPM tab. Unless there is a specific reason not to, it is recommended that the Cypress Devices box be checked. This makes FPGA Express use library components which will create smaller and faster designs. Not checking this box may cause designs, especially those involving arithmetic functions, to be synthesized in a non-optimal way.

Once all of the desired options have been set, the next step is to double-click on the file in the project which contains the top-level of the design. This will open the list of entities/modules in this file. Click on the name of the entity/module which is the top-level of the design. To synthesize the design, choose *Create Implementation* from the *Synthesis* menu item. This will bring up the Create Implementation dialog box which is seen in *Figure 3*.

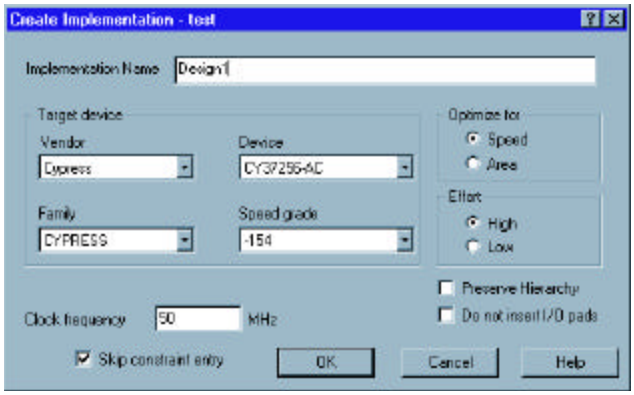

Figure 3. Create Implementation Dialog Box in FPGA Express

All of the Cypress-specific information can be found under the Target Device section. In the Vendor list box, choose Cypress. This will bring up all of the Cypress specific choices into the other list boxes. The Family option does not need to be changed since it contains only the Cypress option. The Device list box contains all of the Cypress devices which are supported by FPGA Express. Choose the appropriate device from this list. If your device is not in the list, choose one from the same family. FPGA Express does not try to fit the design to a Cypress device, so the same netlist will be created regardless of the device that is chosen. Finally, choose the appropriate device speed from the Speed Grade list box. After all of the options have been set, click the OK button to create a design implementation. This will bring up an entry in the Chips section of the project window.

Outputting the Netlist from FPGA Express

The VHDL netlist that FPGA Express outputs will be used as the source code in a new *Warp* project. Click on the optimized version of the design in the Chips section of the project window. Under the *Synthesis* menu option, choose the *Export Netlist* option. This will bring up the Export dialog box as seen in *Figure 4*.

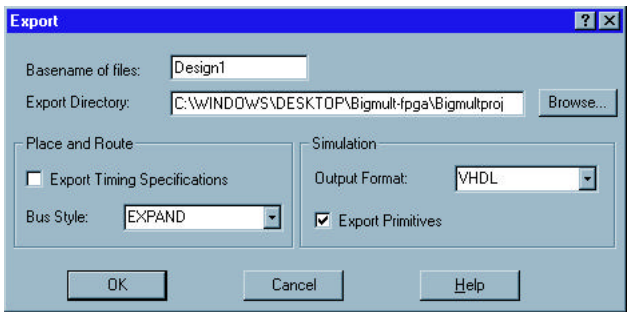

Figure 4. Export Netlist Dialog Box in FPGA Express

Under the Simulation section, the Output Format list box needs to be changed to create a file that Warp can read. Choose VHDL. All of the other fields in the dialog box will default to the appropriate values. The filename and directory can be changed as desired. When all of the fields are set, press the OK button to export the netlist. This ends the portion of the process which involves FPGA Express.

Creating a Project in *Warp*

The project directory that is created using the FPGA Express netlist is the same directory used for the *Warp* project. After launching *Warp*, go to *New* under the *File* menu and choose *Project [Target – Device].* Choose VHDL for the project type. The directory you choose must match the directory to which you output the netlist. After pressing the Next button, you will be prompted to include the appropriate files. The netlist will be in this list of files and is the only file that needs to be included. If it is not, you probably chose the wrong directory at the beginning of the process of creating a project.

The next step is to choose the desired device. It is not necessary to choose the same device chosen during the FPGA Express compilation. FPGA Express outputs a netlist which works for all FLASH370i and Ultra37000 devices. Therefore, you can use the same netlist from FPGA Express to target many different Cypress devices. This can be a time saver if you wish to test your design on various devices. The project does not have to be compiled more than once in FPGA Express. Choose Finish when you are done choosing the device.

Compiling the Design in *Warp*

To compile and fit the design in *Warp*, select *Project* from the *Compile* menu. *Warp* will proceed through the synthesizing and fitting process, outputting any errors that it finds. Some problems specific to FPGA Express netlist compilation are outlined below.

Problem: (E604) Expression type 'bit' does not match target type 'std_ulogic'

Solution: Click on the error to bring you to the appropriate line number. Change `not('1')` on the left-hand side of the equation to '0'

Problem: FPGA Express cannot handle Cypress-specific attributes.

Solution: Cypress-specific attributes such as pin_avoid and pin_numbers are not supported in FPGA Express. If you wish to use any of these options, you will have to include them in a control file when compiling your project in *Warp*.

Problem: (E465) Signal 'c1_c1ci' is floating (not driven by anything)

Solution: This signal is a clock into a component that is not needed. Do a search on the signal name c1ci. There should be a signal declaration and an instance where it is assigned to a port in a component. To eliminate the error, insert `c1ci<='0';` on a separate line just above the component declaration.

Problem: The design does not fit into the device.

Solution: Choose *Compiler Options* from the *Project* menu in *Warp*. Adjust the node cost and recompile the design. This sometimes proves successful in fitting the design. The problem could also be that the design is simply too big for the device. Select a different device and recompile. Occasionally, the netlist exported from FPGA Express is not as efficiently optimized as the one which *Warp* would create. Try creating and compiling a project in *Warp* using your original VHDL or Verilog source code to see if this will fit the desired device.

Post-synthesis Simulation

Warp outputs a variety of IEEE-standard VHDL and Verilog timing simulation models. You can verify the timing and functionality of your design using your choice of any supported VHDL or Verilog simulator.

Programming

Warp generates JEDEC programming files for all Cypress devices which can be used for in-system reprogramming (ISR™) or with various device programmers.

Support

For technical support, contact the Cypress Applications Hotline by sending an e-mail to pldsupport@cypress.com or by calling (408) 943-2821. 24-hour support is available through our web site at http://www.cypress.com. This web site is frequently updated with product information, technical support, application notes, white papers, Frequently Asked Questions (FAQs), and data sheets.