PRELIMINARY **CY7C65640**

CY7C65640
TetraHub™ High Speed USB Hub Controller

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1.0 Introducing TetraHub™

Cypress's *TetraHub*™ is a high-performance standalone Universal Serial Bus (USB) hub controller, compliant with USB Specification, Revision 2.0. Cypress's innovative *'Tetra'* architecture provides four downstream USB ports and four "Transaction Translators" (TT), making it the highest performance hub available. This self-contained device features an integrated Serial Interface Engine, hub controller, hub repeater, four transaction translators, and USB data transceivers. *TetraHub* is a fixed-function solution, requiring no firmware intervention, thereby reducing design risk and development time. *TetraHub* can improve time-to-market in a number of USB 2.0 designs, including standalone hubs, motherboard hubs, and monitor hubs.

TetraHub is a self-powered USB 2.0 hub device. Power management for all downstream ports supports power-switching and overcurrent detection with individual or ganged control. The four downstream ports support high-speed (480-MHz signaling rate), full-speed (12-MHz signaling rate), and low-speed (1.5-MHz signaling rate) devices. Four individual transaction translators have been implemented, providing full 12 MHz signaling performance to each full-speed downstream port, whereas single transaction translator designs must split the full-speed bandwidth between all USB 1.1 peripherals attached to the hub. *TetraHub* has a Serial Peripheral Interface (SPI) communication block, allowing easy implementation in a number of USB hub applications, while also allowing for user customization of vendor ID and product ID. Cypress has also integrated the 1.5kΩ pull-up resistor on the D+ line required for connect/disconnect detection on the upstream USB port. *TetraHub*™ is available in a cost-effective and space-saving 56-lead SSOP package.

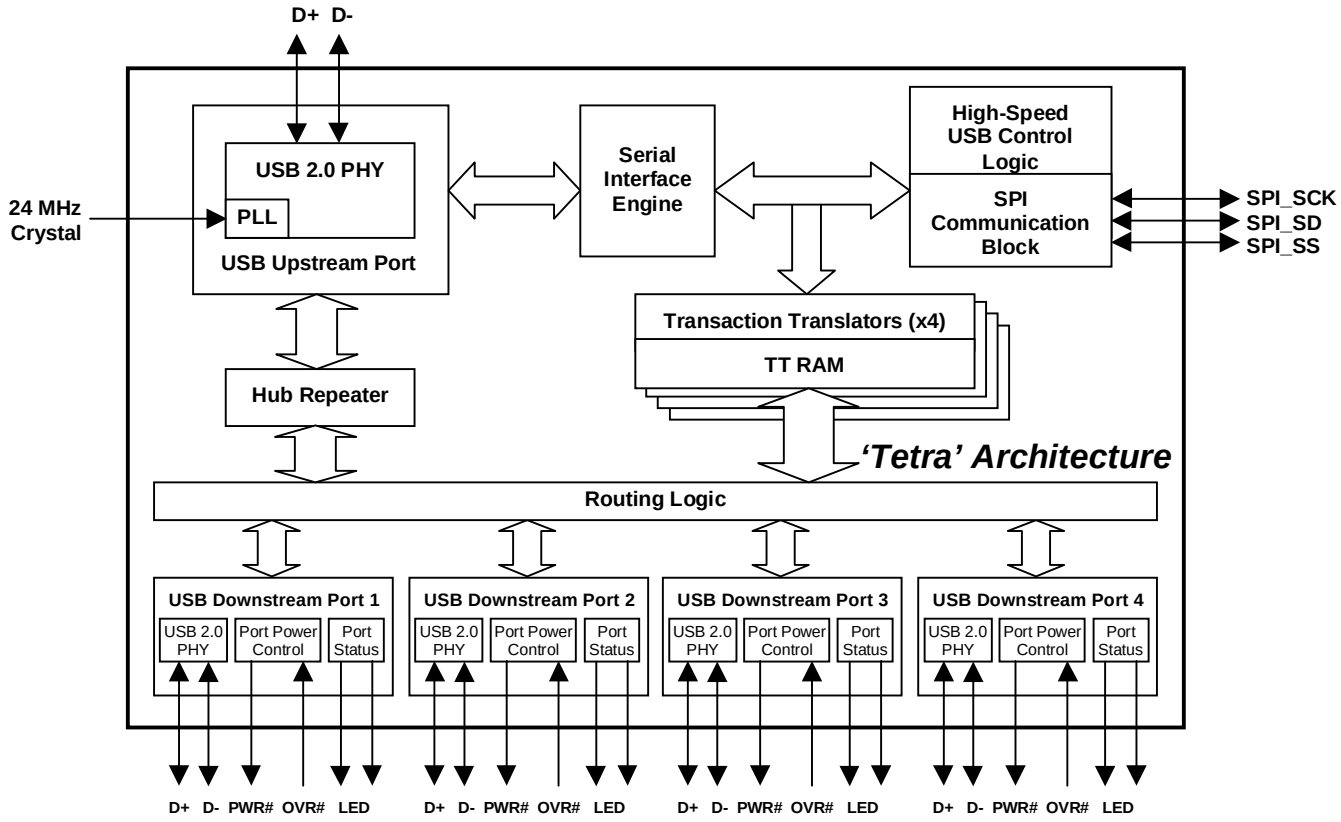


Figure 1-1. Block Diagram

2.0 TetraHub Features

- **True Single-chip integrated USB 2.0 High Speed Hub**
- **Features Transaction Translator per downstream port**
  - Highest performance design architecture (480 MHz signaling to downstream high-speed devices)
  - Provides maximum performance for downstream Full/Low-speed devices. (12 MHz signaling for full-speed devices, 1.5 MHz for low-speed devices)
- **Default configuration provides true single-chip solution, or customer configurable from external EEPROM**
- **4 Downstream Ports, each compatible with USB Low, Full and High Speed signalling**
- **24 MHz External Crystal**
- **Integrated D+ pull-up resistor on upstream USB port**
- **Serial peripheral interface**
- **Space-saving and cost-effective 56-pin SSOP package**

3.0 Applications

The Cypress TetraHub High Speed Hub Controller is ideally suited to all USB 2.0 hub applications. In particular, the TetraHub is ideal for integration with motherboards and within PC Base Units since the “Transaction Translator Per Port” (TTPP) architecture is capable of providing complete 12 MHz bandwidth to each individual downstream port. In constrast, all downstream ports of the conventional “Transaction Translator Per Hub” (TTPH) architecture must share a single 12-MHz bandwidth connection.

4.0 Functional Overview

4.1 USB Signaling Speed

Upstream, TetraHub operates at two of the three rates defined in the Universal Serial Bus Specification Revision 2.0. The speed at which the hub operates depends upon whether the upstream connection is to a high-speed configured port or a full-speed configured port. TheTetraHub operates at the same speed as the configuration of the parent port. If the parent port is configured as:

- High-speed, the TetraHub operates at high-speed or at a signaling rate of 480 MHz
- Full-speed, the TetraHub operates at full-speed or at a signaling rate of 12 MHz

Through its downstream ports, TetraHub provides signalling at all three rates defined in the Universal Serial Bus Specification Revision 2.0 based upon the downstream device characteristics:

- High-speed, with a signaling rate of at 480 MHz (only when the parent hub is high-speed configured)
- Full-speed, with a signaling rate of 12 MHz
- Low-speed, with a signaling rate of 1.5 MHz

4.2 Serial Peripheral Interface

The Serial Peripheral Interface is used by the TetraHub to obtain the Vendor ID (VID), Product ID (PID), and Device ID (DID) from an external EEPROM during powerup. If the TetraHub reads a byte with a value of ‘0xD0’ at address 0 over the SPI, then an external EEPROM is present and the VID, PID, and DID are loaded from that EEPROM. The VID, PID, and DID are stored as shown in the table below.

Table 4-1. EEPROM

Address	Value
0	0xD0
1	VID (LSB)
2	VID (MSB)
3	PID (LSB)
4	PID (MSB)
5	DID (LSB)
6	DID (MSB)

If no EEPROM is detected, it uses a single internal VID/PID/DID combination (0x04B4, 0x8613, 0x0000).

4.3 Reset

An input pin (RESET#) resets the chip. This pin has hysteresis and is active LOW. The PLL is considered stable approximately 200 µsec (BUGBUG: need to check: RGR expects 5 ms, BBX says 5 ms is not an uncommon value) after V_{CC} has reached 3.3 volts. Typically, an RC network (R=100k, C=0.1µf) is used to provide the RESET# signal.

5.0 Pin Assignments

Figure 5-1 identifies all signals for the space-saving 56-pin SSOP package. The following pages describe the functions of the individual pins.

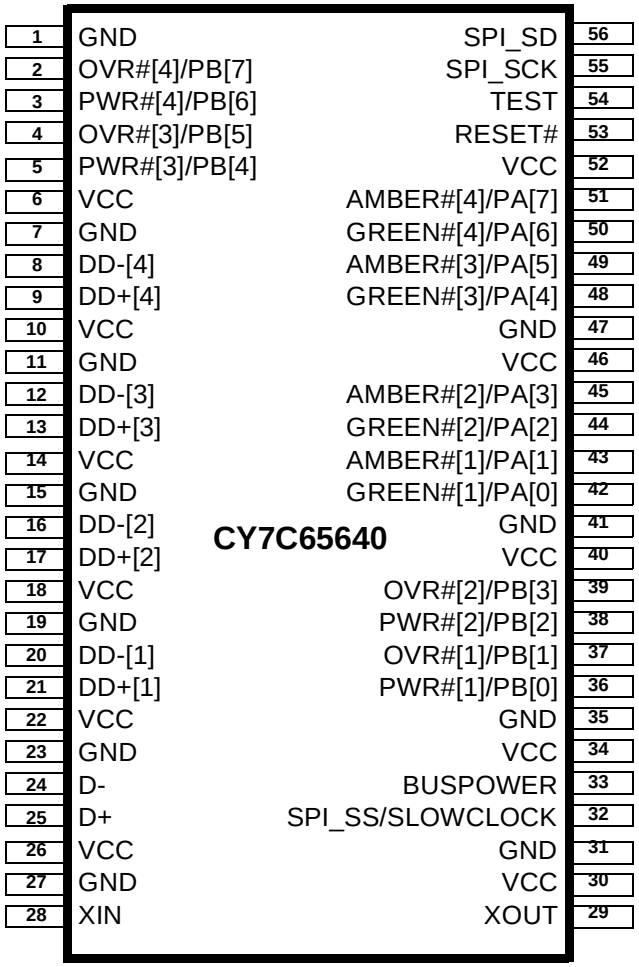


Figure 5-1. Pin Assignment

Table 5-1. CY7C65640 Pin Descriptions

Pin Number	Name	Type	Default	Description
6	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
10	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
14	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
18	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
22	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
26	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
30	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
34	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
40	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
46	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
52	VCC	Power	N/A	**V_{CC}**. This signal provides power to the chip.
1	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
7	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
11	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
15	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
19	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
23	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
27	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
31	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
35	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
41	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
47	GND	Power	N/A	**Ground**. Connect to ground with as short a path as possible.
24	D–	I/O/Z	Z	**Upstream D– Signal**. Connect to USB D– through a 24Ω resistor.
25	D+	I/O/Z	Z	**Upstream D+ Signal**. Connect to USB D+ through a 24Ω resistor.
28	XIN	Input	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and 22–33 pF capacitor to GND.
29	XOUT	Output	N/A	**Crystal Output**. Connect to a 24-MHz parallel-resonant, fundamental mode crystal and 22–33 pF capacitor to GND.
53	RESET#	Input	N/A	**Reset Input** Active low reset signal.
33	BUSPOWER	Input	N/A	**Vbus input**. Connect to upstream V_{bus}.
32	SPI_SS/ SLOW-CLOCK	I/O	N/A	**SPI Slave Select and External Oscillator**. Connect to SS pin of the EEPROM, to V_{CC} with 10 kΩ resistor, and to GND with 1 nF capacitor.
56	SPI_SD	I/O/Z	Z	**SPI Dataline**. Connect to GND with a 10 kΩ resistor and to the SPI_SD pin of the EEPROM
55	SPI_SCK	I/O/Z	1	**SPI Clock.** Connect to EEPROM SCK pin.
54	TEST	I	N/A	**Test Pin**. Connect to ground.
				DOWNSTREAM PORT 1
20	DD-[1]	I/O/Z	Z	**Downstream D– Signal**. Connect to Port1 D– through a 24Ω resistor.
21	DD+[1]	I/O/Z	Z	**Downstream D+ Signal**. Connect to Port1 D+ through a 24Ω resistor.
43	/AMBER[1]	O/Z	Z	**LED** Driver output for Amber LED for Port Indicator support. Active LOW.
42	/GREEN[1]	O/Z	Z	**LED** Driver output for Green LED for Port Indicator support. Active LOW.

Pin Number	Name	Type	Default	Description
37	/OVR[1]	I	I	**Overcurrent** condition detection input. Active LOW.
36	/PWR[1]	O/Z	Z	**Power** Switch driver output . Active LOW.
				DOWNSTREAM PORT 2
16	DD-[2]	I/O/Z	Z	**Downstream D– Signal**. Connect to Port2 D– through a 24Ω resistor.
17	DD+[2]	I/O/Z	Z	**Downstream D+ Signal**. Connect to Port2 D+ through a 24Ω resistor.
45	/AMBER[2]	O/Z	Z	**LED** Driver output for Amber LED for Port Indicator support. Active LOW.
44	/GREEN[2]	O/Z	Z	**LED** Driver output for Green LED for Port Indicator support Active LOW.
39	/OVR[2]	I	I	**Overcurrent** condition detection input. Active LOW.
38	/PWR[2]	O/Z	Z	**Power** Switch driver output. Active LOW.
				DOWNSTREAM PORT 3
12	DD-[3]	I/O/Z	Z	**Downstream D– Signal**. Connect to Port3 D– through a 24Ω resistor.
13	DD+[3]	I/O/Z	Z	**Downstream D+ Signal**. Connect to Port3 D+ through a 24Ω resistor.
49	/AMBER[3]	O/Z	Z	**LED** Driver output for Amber LED for Port Indicator support. Active LOW.
48	/GREEN[3]	O/Z	Z	**LED** Driver output for Green LED for Port Indicator support. Active LOW.
4	/OVR[3]	I	I	**Overcurrent** condition detection input. Active LOW.
5	/PWR[3]	O/Z	Z	**Power** Switch driver output . Active LOW.
				DOWNSTREAM PORT 4
8	DD-[4]	I/O/Z	Z	**Downstream D– Signal**. Connect to Port4 D– through a 24Ω resistor.
9	DD+[4]	I/O/Z	Z	**Downstream D+ Signal**. Connect to Port4 D+ through a 24Ω resistor.
51	/AMBER[4]	O/Z	Z	**LED** Driver output for Amber LED for Port Indicator support. Active LOW.
50	/GREEN[4]	O/Z	Z	**LED** Driver output for Green LED for Port Indicator support. Active LOW.
2	/OVR[4]	I	I	**Overcurrent** condition detection input. Active LOW.
3	/PWR[4]	O/Z	Z	**Power** Switch driver output . Active LOW.

6.0 Absolute Maximum Ratings

Storage Temperature .....–65°C to +150°C
Ambient Temperature with Power Supplied .....0°C to +70°C
Supply Voltage to Ground Potential .....–0.5V to +4.0V
DC Input Voltage to Any Pin ..... –0.5V to Vcc+0.5V
DC Voltage Applied to Outputs in High Z State ..... -0.5V to Vcc+0.5V
Power Dissipation ..... TBD mW
Static Discharge Voltage ..... >2000V
Latch-up Current ..... >TBD mA
Max Output Sink Current ..... TBD mA

7.0 Operating Conditions

T_A (Ambient Temperature Under Bias) .....0°C to +70°C
Supply Voltage .....+3.0V to +3.6V
Ground Voltage 0V
F_{OSC} (Oscillator or Crystal Frequency) .....24 MHz ± 0.05%, parallel resonant, fundamental mode

8.0 DC Characteristics

Parame-ter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage		2		5.25	V
V_{IL}	Input Low Voltage		–0.5		0.8	V
I_I	Input Leakage Current	$0< V_{IN} < V_{CC}$			±10	µA
V_{OH}	Output Voltage High	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current High				4	mA
I_{OL}	Output Current Low				4	mA
C_{IN}	Input Pin Capacitance				10	pF
I_{SUSP}	Suspend Current			TBD	500	µA
I_{CC}	Supply Current	Operating, upstream bus connected			TBD	mA
USB Transceiver						
RpH	Output Impedance (HIGH state)		41	45	49	Ω
RpL	Output Impedance (LOW state)		41	45	49	Ω
Ii	Input Leakage Current	V_{CC} = 3.6V; V_I = 5.5V or GND; not for IO pins		±0.1	±5	µA
Ioz	Three-State Output OFF-State Current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			±10	µA

9.0 AC Electrical Characteristics

9.1 USB Transceivers

Both the upstream USB transceiver and all four downstream transceivers are fully compliant with the requirements of the USB Specification, Rev 2.0.

9.2 Serial Peripheral Interface

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
	Clock Rise/Fall Time		-		500	ns
	Clock Frequency		-		600	MHz
	Data Set-up Time		50		-	ns
	Hold Time		100			ns

10.0 Ordering Information

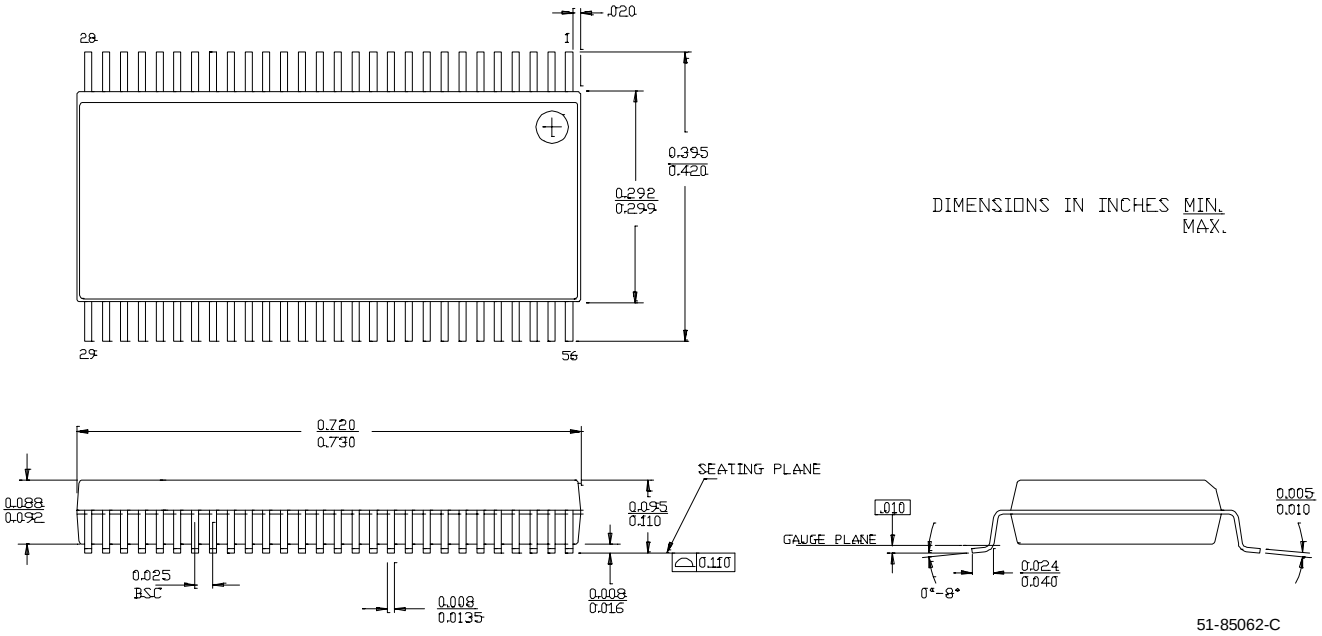
Ordering Code	Package Type
CY7C65640-PVC	56 SSOP
CY3688	TetraHub™ Evaluation Kit

Document #: 38-01109-**

11.0 Package Diagrams

The TetraHub is available in a space-saving 56-pin SSOP package

56-Lead Shrunk Small Outline Package O56



12.0 Document Revision History

Document Title: High Speed (480 MBS) USB HUB Controller IC Document Number: 38-01109				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	3063	12/4/00	CKK	New Data Sheet