CY7C68013
EZ-USB *FX2* USB Microcontroller
High-Speed USB Peripheral Controller

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1.0 EZ-USB FX2 Features

Cypress's EZ-USB FX2 is the world's first USB 2.0 integrated microcontroller. By integrating the USB 2.0 transceiver, SIE, enhanced 8051 microcontroller and a programmable peripheral interface in a single chip, Cypress has created a very cost-effective solution that provides superior time-to-market advantages. The ingenious architecture of FX2 results in data transfer rates of 56 Mbytes per second, the maximum allowable USB 2.0 bandwidth, while still using a low-cost 8051 microcontroller in a package as small as a 56 SSOP. Because it incorporates the USB 2.0 transceiver, the FX2 is more economical providing a smaller footprint solution than USB 2.0 SIE or external transceiver implementations. With EZ-USB FX2, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application specific functions and decreasing development time to ensure USB compatibility. The General Programmable Interface (GPIF) and Master / Slave Endpoint FIFO (8 or 16 bit data bus) provides an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA and most DSP/processors.

Three packages are defined for the family: 56 SSOP, 100 TQFP, and 128 TQFP.

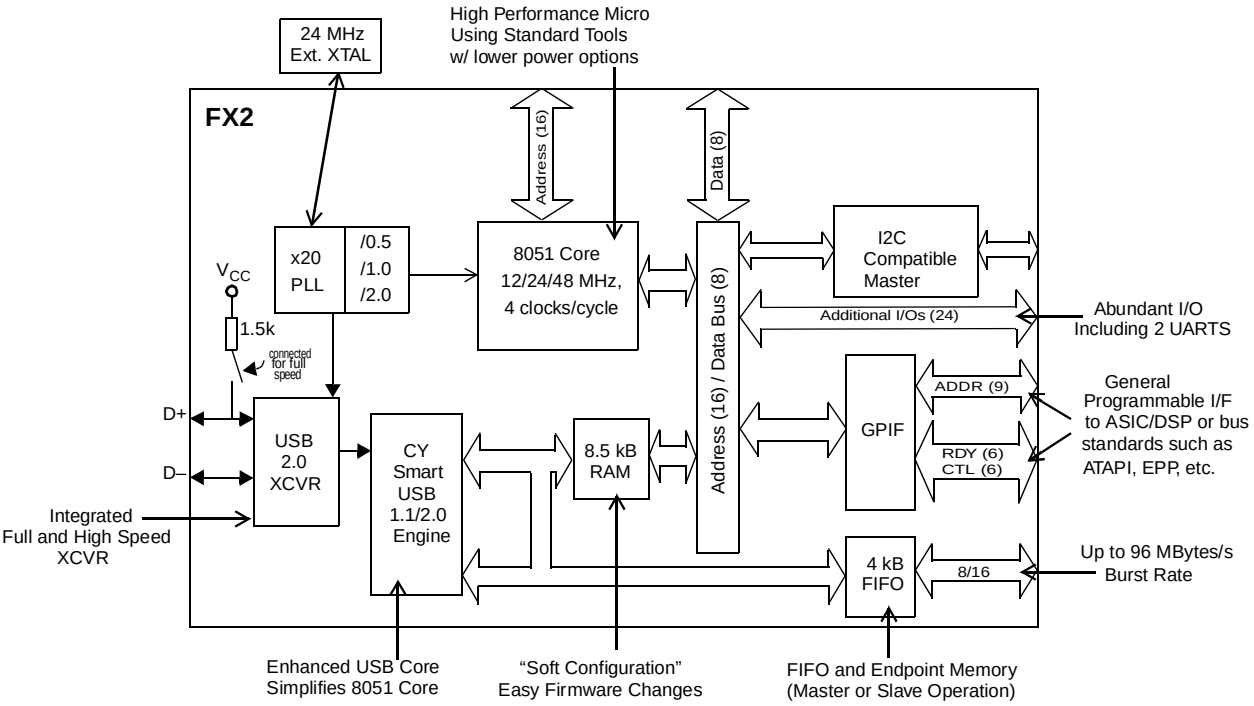

Figure 1-1. Block Diagram

- **Single-chip integrated USB 2.0 Transceiver, Serial Interface Engine (SIE), and Enhanced 8051 Microprocessor**
- **Soft: 8051 runs from internal RAM, which is:**
  - **Downloaded via USB, or**
  - **Loaded from EEPROM**
- **4 programmable BULK / INTERRUPT / ISOCHRONOUS**
- **8- or 16-bit external data interface**
- **General Programmable Interface (GPIF)**
  - **Allows direct connection to most parallel interfaces; 8- and 16-bit**
  - **Programmable waveform descriptors and configuration registers to define waveforms**
  - **Supports multiple Ready (RDY) inputs and Control (CTL) outputs**
- **Integrated, industry standard 8051 with enhanced features:**
  - **Up to 48-MHz clock rate**
  - **Four clocks per instruction cycle**
  - **Two UARTS**

  - Three counter/timers
  - Expanded interrupt system
  - Two data pointers
- 3.3-volt operation
- Smart Serial Interface Engine (SIE)
- Vectored USB interrupts
- Separate data buffers for the SETUP and DATA portions of a CONTROL transfer
- Integrated I^2C Compatible controller, runs at 100 or 400 kHz
- 48-MHz, 24-MHz, or 12-MHz 8051 operation
- Four integrated FIFOs
  - Brings glue and FIFOs inside for lower system cost
  - Automatic conversion to and from 16-bit buses
  - Master or Slave operation
  - FIFOs can use externally supplied clock or asynchronous strobes
  - Easy interface to ASIC and DSP ICs
- Special Autovectors for FIFO and GPIF interrupts
- Up to 40 general purpose I/Os
- Three package options—128-pin TQFP, 100-pin TQFP, and 56-pin SSOP

2.0 Applications

- DSL Modems
- ATA Interface
- Memory Card Readers
- Legacy Conversion Devices
- Cameras
- Scanners
- Home PNA
- Wireless LAN
- MP3 Players
- Networking

3.0 Functional Overview

3.1 USB Signaling Speed

FX2 operates at two of the three rates defined in the Universal Serial Bus Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbits/s
- High speed, with a signaling bit rate of 480 Mbits/s

FX2 does not support the low-speed signaling mode of 1.5 Mbits/s.

3.2 8051 Microprocessor

The 8051 microprocessor embedded in the FX2 family has 256 bytes of register RAM, an expanded interrupt system, 3 timer/counters and 2 UARTs.

3.2.1 8051 Clock Frequency

FX2 has an on-chip oscillator circuit that uses an external 24-MHz (±100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500 µW drive level
- 27–33 pF (5% tolerance) load capacitors

An on-chip PLL multiplies the 24-MHz oscillator up to 480 MHz, as required by the transceiver/PHY, and internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 48 MHz. If an EEPROM is connected and certain EEPROM configuration bits are set, the 8051 can also run at 24 MHz or 12 MHz. The 8051 clock rate is set at boot time, as the EEPROM

is read before the 8051 is out of reset. This rate cannot be modified once the 8051 is running. The 8051 may examine internal register bits to determine the frequency at which it is operating.

The CLKOUT pin, which can be three-stated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency—48, 24, or 12 MHz.

3.2.2 UARTs

FX2 contains two standard 8051 UARTS, addressed via Special Function Register (SFR) bits. The UART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230-KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48, 24, 12 MHz) such that it always presents the correct frequency for 230-KBaud operation.

NOTE: 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a “1”, for UART0 and/or UART1, respectively.

3.2.3 Special Function Registers (SFR)

Certain 8051 SFR addresses are populated to provide fast access to critical FX2 functions. These SFR additions are shown in *Table 3-1*. Bold type indicates non-standard, enhanced 8051 registers.

The two SFR rows that end with “0” and “8” contain bit-addressable registers. The four I/O ports A–D use the SFR addresses used in the standard 8051 for ports 0–3, which are not implemented in FX2.

Because of the faster and more efficient SFR addressing, the FX2 I/O ports are not addressable in external RAM space (using the MOVX instruction).

3.3 I^2C Compatible Bus

FX2 supports the I^2C compatible bus as a master only at 100/400 kbits/s. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to 3.3V, even if no I^2C compatible device is connected.

3.4 Buses

All packages: 8- or 16-bit “FIFO” bidirectional data bus, multiplexed on I/O ports B and D.

128-pin package: adds 16-bit output-only 8051 address bus, 8-bit bidirectional data bus.

Table 3-1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1			
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**APTR1H**	**EPSTAT**	**EP01STAT**	RCAP2L			
B	TL1	**APTR1L**	**EP24FLGS**	**GPIFTRIG**	RCAP2H			
C	TH0	**AUTODAT1**	**EP68FLGS**		TL2			
D	TH1	**APTR2H**		**SGLDATH**	TH2			
E	**CKCON**	**APTR2L**		**SGLDATLX**				
F	***SPC_FNC***	**AUTODAT2**	**APTRSETUP**	**SGLDATLNOX**				

3.5 USB Boot Methods

During the power-up sequence, internal logic checks the I^2C compatible port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0), or it boot-loads the EEPROM contents into internal RAM (0xC2). If no EEPROM is detected, FX2 enumerates using internally stored descriptors. The default ID values for FX2 are VID/PID/DID (0x04B4, 0x8613, 0x0000).

NOTE: The I^2C compatible bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

3.6 Interrupt System

3.6.1 INT2 Interrupt Request & Enable Registers

FX2 implements an autovector feature for INT2 and INT4. There are 27 INT2 (USB) vectors, and 14 INT4 (FIFO/GPIF) vectors. See FX2 TRM for more details.

3.7 Reset and Wakeup

3.7.1 Reset Pin

An input pin (RESET#) resets the chip. This pin has hysteresis and is active LOW. The internal PLL stabilizes approximately 200 µs after V_{CC} has reached 3.3 volts. Typically, an external RC network (R=100k, C=0.1 µF) is used to provide the RESET# signal.

3.7.2 Wake Up Pins

The 8051 puts itself and the rest of the chip into a power-down mode by setting PCON.0=1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic, the oscillator restarts and after the PLL stabilizes, and the 8051 receives a wakeup interrupt. This applies whether or not FX2 is connected to the USB.

The FX2 exits the power down (USB suspend) state using one of the following methods:

- USB bus signals resume
- External logic asserts the WAKEUP pin
- External logic asserts the PA3/WU2 pin

The second wakeup pin, WU2, can also be configured as a general purpose I/O pin. This allows a simple external R-C network to be used as a periodic wakeup source.

3.8 Program/Data RAM

3.8.1 Size

The FX2 has 8 kbytes of internal program/data RAM, where PSEN#/RD# signals are internally ORed to allow the 8051 to access it as both program and data memory. No USB control registers appear in this space.

Two memory maps are shown in the following diagrams:

Figure 3-1. Internal Code Memory, EA=0

Figure 3-2. External Code Memory, EA=1

3.8.2 Internal Code Memory, EA=0

This mode implements the internal 8 kbytes block of RAM (starting at 0) as combined code and data memory. When external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This allows the user to connect a 64-kbyte memory without requiring address decodes to keep clear of internal memory spaces.

Only the **internal** 8kbytes and **scratch pad** 0.5 kbytes RAM spaces have the following access:

- USB download
- USB upload
- SetupData Pointer
- I^2C compatible interface boot load

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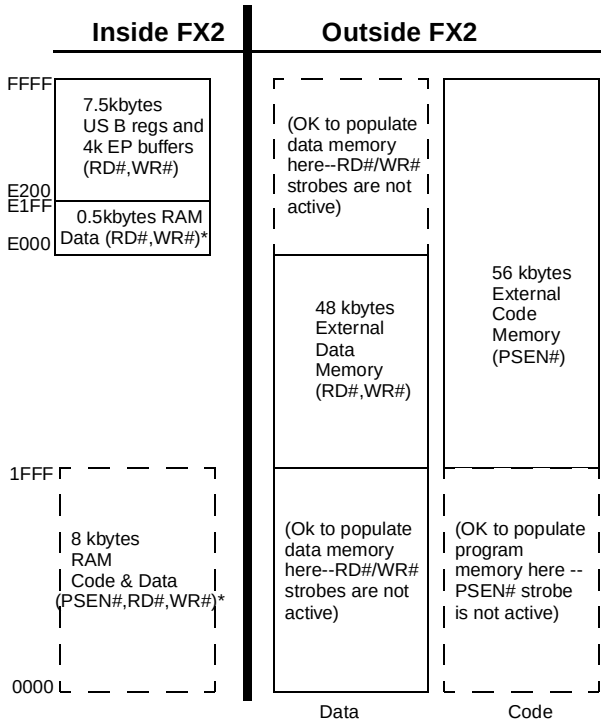
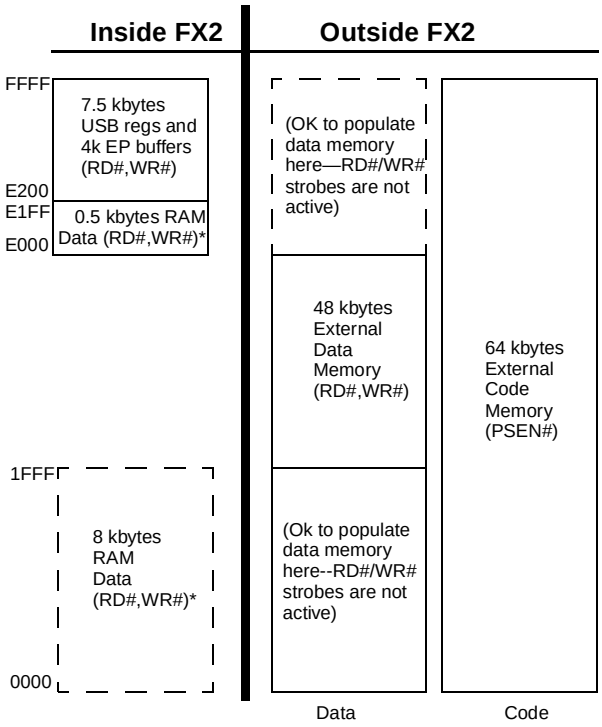


*SUDPTR, USB upload/download, I^2C compatible interface boot access

Figure 3-1. Internal Code Memory, EA=0

3.8.3 External Code Memory, EA=1

The bottom 8 kbytes of program memory is external, and therefore the bottom 8 kbytes of internal RAM is accessible only as data memory.



*SUDPTR, USB upload/download, I^2C compatible interface boot access

Figure 3-2. External Code Memory, EA=1

3.9 Register Addresses

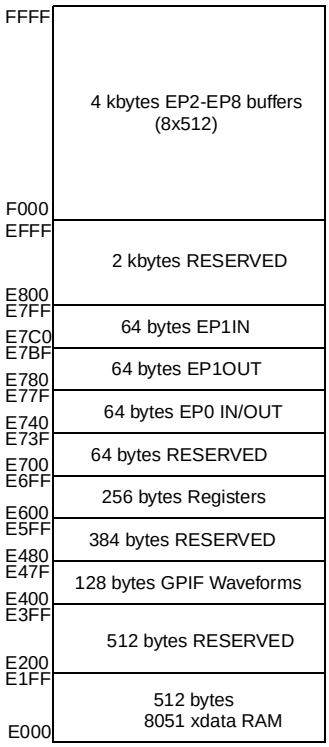


Figure 3-3. Data RAM

3.10 Endpoint RAM

3.10.1 Size

- 3x64 bytes (Endpoints 0 and 1)
- 8x512 bytes (Endpoints 2,4,6,8)

3.10.2 Organization

- EP0 Bidirectional endpoint zero, 64-byte buffer.
- EP1IN, EP1OUT 64-byte buffers, bulk or interrupt
- EP2,4,6,8 Eight 512-byte buffers, bulk, interrupt, or isochronous. EP2 & 6 can be either double, triple, or quad buffered. For High-Speed endpoint configuration options see *Figure 3-4*.

3.10.3 Setup Data Buffer

A separate 8-byte buffer at 0xE6B8-0xE6BF holds the SETUP data from a CONTROL transfer.

3.10.4 Endpoint Configurations (High speed mode)

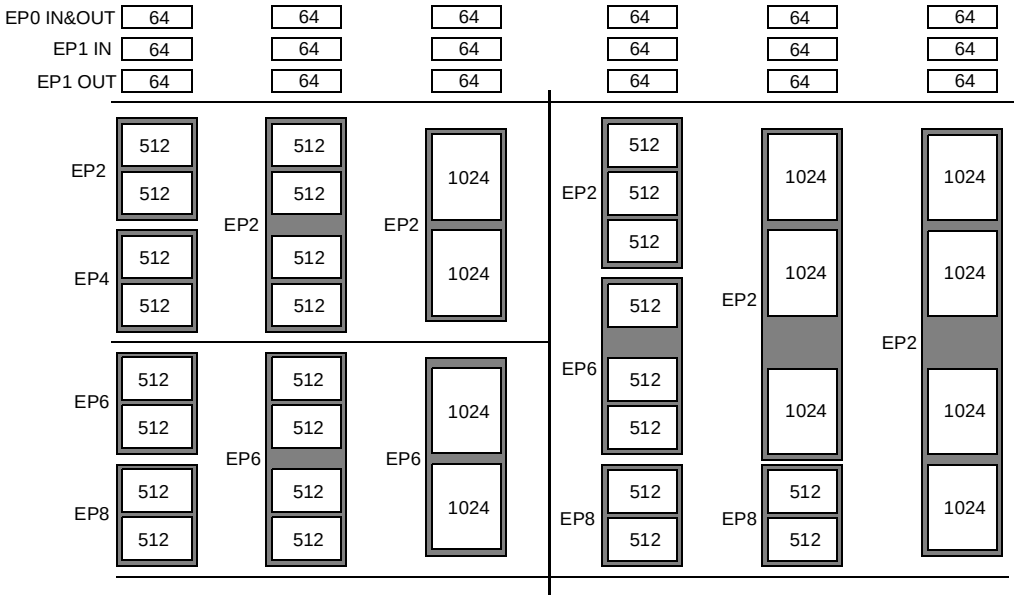


Figure 3-4. Endpoint Configuration

Endpoints 0 and 1 are the same for every configuration. Endpoint zero is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT. To the left of the vertical line, the user may pick different configurations for EP2&4 and EP6&8, since none of the 512 byte buffers are combined between these endpoint groups. An example endpoint configuration would be:

EP2—1024 double buffered; EP6—512 quad buffered.

To the right of the vertical line, buffers are shared between EP2-8, and therefore only entire columns may be chosen.

3.10.5 Default Full-Speed Alternate Settings

Table 3-2. Default Full-Speed Alternate Settings

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	64 bulk	64 int	64 int
ep1in	0	64 bulk	64 int	64 int
ep2	0	64 bulk out (2x)	64 int out (2x)	64 iso out (2x)
ep4	0	64 bulk out (2x)	64 bulk out (2x)	64 bulk out (2x)
ep6	0	64 bulk in (2x)	64 int in (2x)	64 iso in (2x)
ep8	0	64 bulk in (2x)	64 bulk in (2x)	64 bulk in (2x)

NOTE: “0” means “not implemented”

NOTE: “2x” means “double buffered”

3.10.6 Default High-Speed Alternate Settings

Table 3-3. Default High-Speed Alternate Settings

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	512 bulk*	64 int	64 int
ep1in	0	512 bulk*	64 int	64 int
ep2	0	512 bulk out (2x)	512 int out (2x)	512 iso out (2x)
ep4	0	512 bulk out (2x)	512 bulk out (2x)	512 bulk out (2x)
ep6	0	512 bulk in (2x)	512 int in (2x)	512 iso in (2x)
ep8	0	512 bulk in (2x)	512 bulk in (2x)	512 bulk in (2x)

NOTE: "0" means "not implemented"

NOTE: "2x" means "double buffered"

*Note: Even though these buffers are 64 bytes, they are reported as 512 for USB 2.0 compliance. The user must never transfer packets larger than 64 bytes to EP1.

3.11 External FIFO interface

3.11.1 Architecture

The FX2 slave FIFO architecture has eight 512-byte blocks in the endpoint RAM which directly serve as FIFO memories, and are controlled by FIFO control signals (such as IFCLK, SLRD, SLWR, SLOE, PKTEND, and flags).

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms, the GPIF for internally generated control signals, or the slave FIFO interface for externally controlled transfers.

3.11.2 Master/Slave Control Signals

The FX2 endpoint FIFOS are implemented as eight physically distinct 256x16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains, the USB(SIE) domain and the 8051-I/O Unit domain. This switching is done virtually instantaneously, giving essentially zero transfer time between "USB FIFOS" and "Slave FIFOS." Since they are physically the same memory, no bytes are actually transferred between buffers.

At any given time, some RAM blocks are filling/emptying with USB data under SIE control, while other RAM blocks are available to the 8051 and/or the I/O control unit. The RAM blocks operate as single-port in the USB domain, and dual-port in the 8051-I/O domain. The blocks can be configured as single, double, triple, or quad buffered as previously shown.

The I/O control unit implements either an internal-master (M for master) or external-master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) can be used as flag inputs from an external FIFO or other logic if desired. The GPIF can be run from either an internally derived clock or externally supplied clock (IFCLK), at a rate that transfers data up to 96 Megabytes/s (48 MHz).

In Slave (S) mode, the FX2 accepts either an internally derived clock or externally supplied clock (IFCLK, max. frequency 48 MHz) and SLRD, SLWR, SLOE, PKTEND signals from external logic. Each endpoint can individually be selected for byte or word operation by an internal configuration bit, and a Slave FIFO Output Enable signal SLOE enables data of the selected width. External logic must insure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in synchronous mode.

3.11.3 GPIF and FIFO clock rates

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock, of up to 48 MHz, feeding the IFCLK pin can be used as the interface clock. IFCLK can be configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired.

3.12 GPIF

The GPIF is a flexible 8- or 16-bit parallel interface driven by a user-programmable finite state machine. It allows the CY7C68013 to perform local bus mastering, and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general purpose ready inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a ready input (or multiple inputs) must be before proceeding. The GPIF vector can be programmed to advance a FIFO to the next data value, advance an address, etc. A sequence of the GPIF vectors make up a single waveform that will be executed to perform the desired data move between the CY7C68013 and the external design.

3.12.1 Six Control OUT Signals

The 100- and 128-pin packages bring out all six Control Output pins (CTL0-CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals, CTL0–CTL2. CTLx waveform edges can be programmed to make transitions as fast as once per clock (20.8 ns using a 48-MHz clock).

3.12.2 Six Ready IN Signals

The 100- and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56-pin package brings out two of these signals, RDY0–1.

3.12.3 Nine GPIF Address OUT signals

Nine GPIF address lines are available in the 100- and 128-pin packages, GPIFADR[8..0]. The GPIF address lines allow indexing through up to a 512 byte block of RAM. If more address lines are needed, I/O port pins can be used.

3.12.4 Long Transfer Mode

In master mode, the 8051 appropriately sets two FIFO transaction count registers (EPxTCH and EPxTCL, where x is either 2, 4, 6, or 8) for unattended transfers of up to 65,536 bytes. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions complete.

3.13 USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 8 kbytes RAM and of the internal 512 bytes scratch pad RAM via a vendor specific command. This capability is normally used when “soft” downloading user code and is available only to and from internal RAM, whether the 8051 is held in reset or running. The available RAM spaces are 8 kbytes from 0x0000-0x1FFF (code/data) and 512 bytes from 0xE000-0xE1FF (scratch pad RAM).

Note: A “loader” running in internal RAM can be used to transfer downloaded data to external memory.

3.14 Autopointer Access

FX2 provides two identical autopointers. They are similar to the internal 8051 data pointers, but with an additional feature: they can optionally increment a pointer address after every memory access. This capability is available to and from both internal and external RAM. The autopointers are available in SFRs and external FX2 registers, under control of a mode bit (APTRSETUP). When using the SFR autopointer registers the available RAM spaces are internal only: 8 kbytes from 0x0000-0x1FFF and 512 bytes from 0xE000-0xE1FF. Using the external FX2 autopointer access (at 0xE67B-0xE67C) allows the autopointer to access all RAM, internal and external to the part. Also, the autopointers can point to any FX2 register or endpoint buffer space. When autopointer access to external memory is enabled, location 0xE67B and 0xE67C in XDATA and PDATA space cannot be used.

3.15 I^2C Compatible Controller

FX2 has one I^2C compatible port that is driven by two internal controllers, one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051, once running, uses to control external I^2C compatible devices. The I^2C compatible port operates in master mode only.

3.15.1 I^2C Compatible Port Pins

The I^2C compatible pins SCL and SDA must have external 2.2-kΩ pull-up resistors. External EEPROM device address pins must be configured properly. See *Figure 3-4* for configuring the device address pins.

Table 3-4. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00*	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1

* This EEPROM does not have address pins

3.15.2 I²C Compatible Interface Boot Load Access

At power-on reset the I²C compatible interface boot loader will load the VID/PID/DID and up to 8 kbytes of program/data. The available RAM spaces are 8 kbytes from 0x0000-0x1FFF and 512 bytes from 0xE000-0xE1FF. The 8051 will be in reset. I²C compatible interface boot loads only occur after power-on reset.

3.15.3 I²C Compatible Interface General Purpose Access

The 8051 can control peripherals connected to the I²C compatible bus using the I2CTL and I2DAT registers. FX2 provides I²C compatible master control only, it is never an I²C compatible slave.

4.0 Pin Assignments

Figure 4-1 identifies all signals for the three package types. The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 128-, 100-, and 56-pin packages.

The 56-pin package is the lowest-cost version. The signals on the left edge of the 56-pin package in *Figure 4-1* are common to all versions in the FX2 family. Three modes are available in all package versions: Port, GPIF master, and Slave FIFO. These modes define the signals on the right edge of the diagram. The 8051 selects the interface mode using the IFCONFIG[1:0] register bits. Port mode is the power-on default configuration.

The 100-pin package adds functionality to the 56-pin package by adding these pins:

- PORTC or alternate GPIFADR[7...0] address signals
- PORTE or alternate GPIFADR8 address signals and 7 more 8051 signals
- 3 GPIF Control signals
- 4 GPIF Ready signals
- Nine 8051 signals (two UARTS, three timer inputs, INT4,and INT5#)
- BKPT, RD#, WR#

The 128-pin package is the full version, adding the 8051 address and data buses plus control signals. Note that two of the required signals, RD# and WR#, are present in the 100-pin version. In the 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from/writes to PORTC.

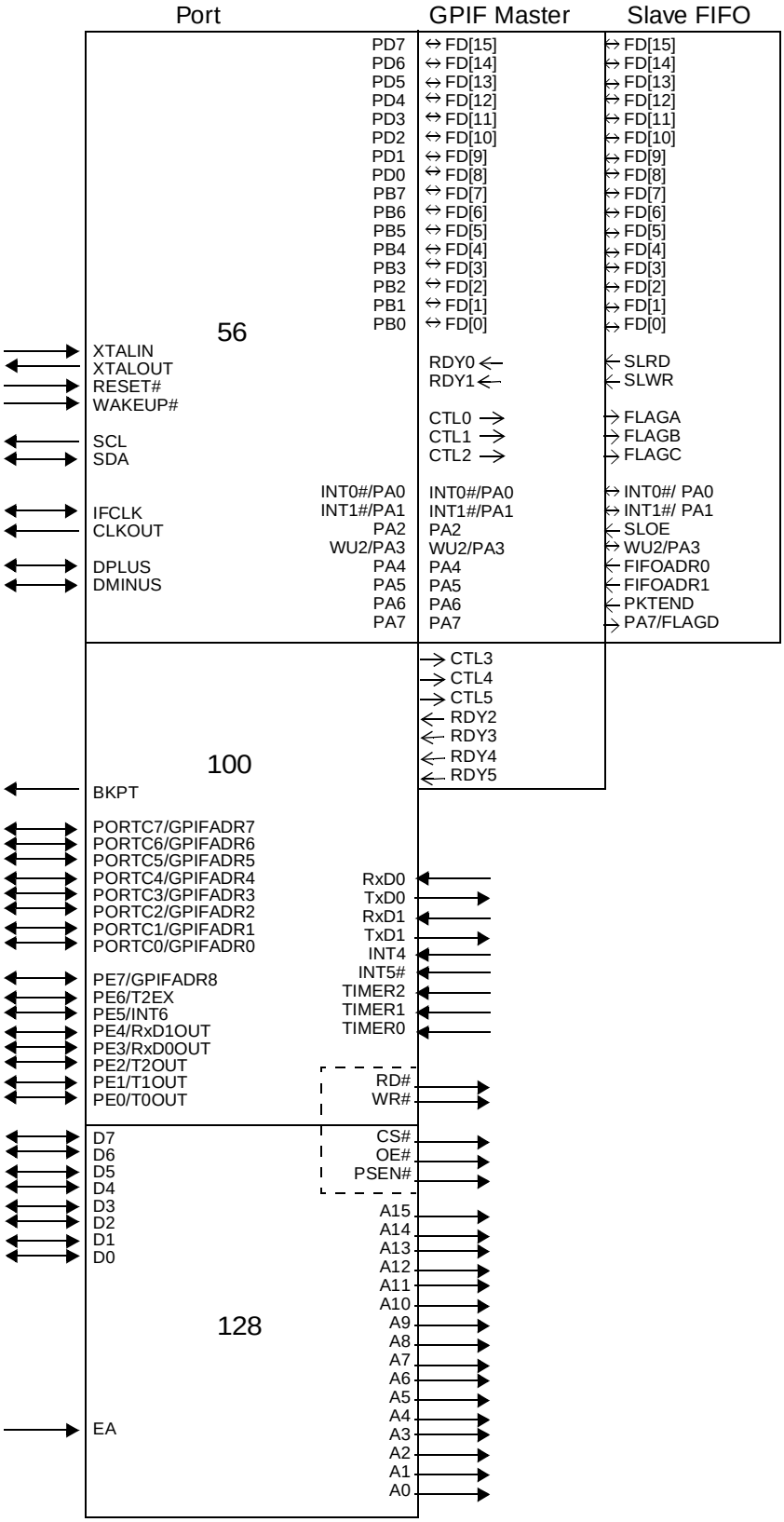


Figure 4-1. Signals

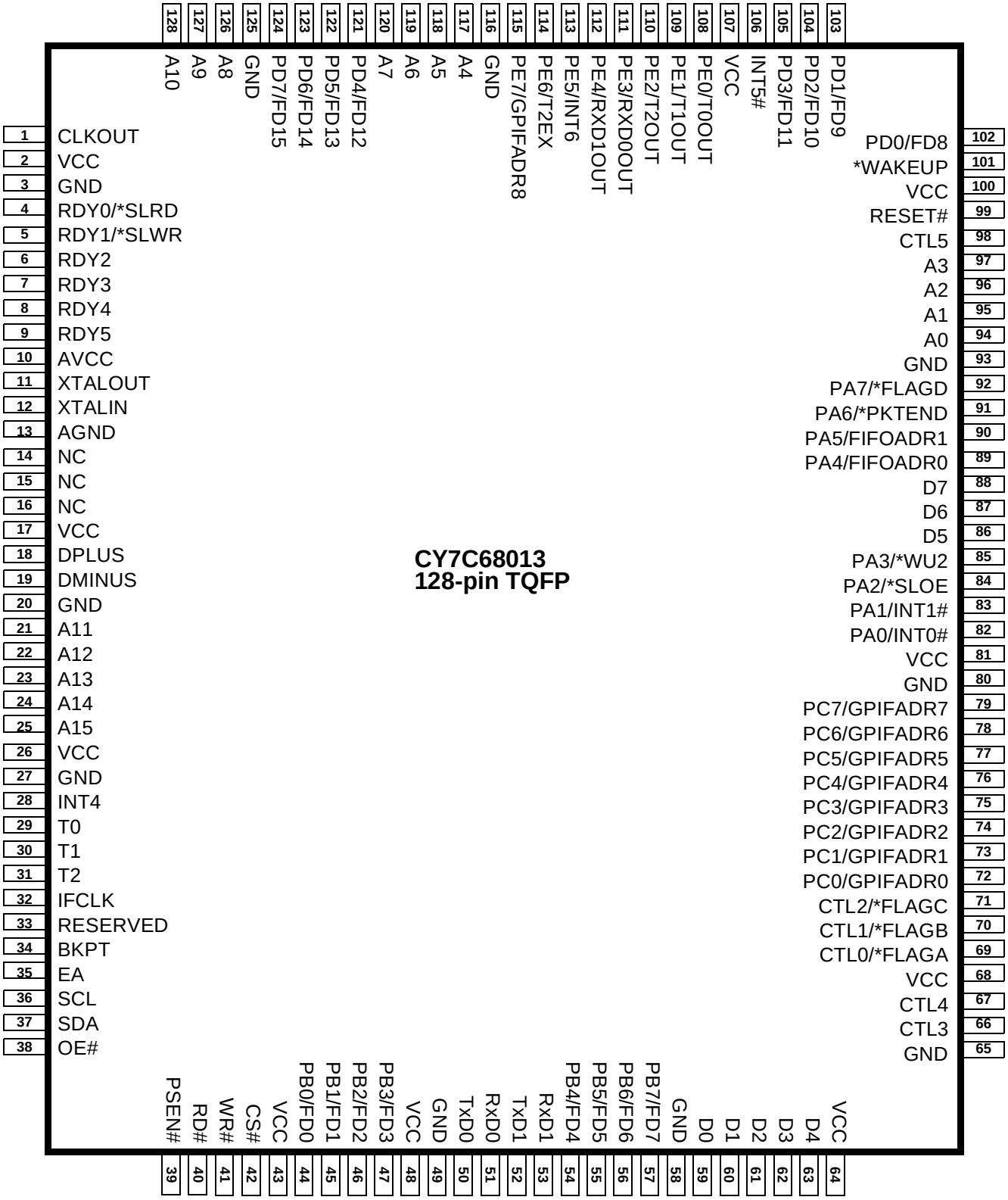


Figure 4-2. CY7C68013 128-pin TQFP Pin Assignment

* denotes programmable polarity.

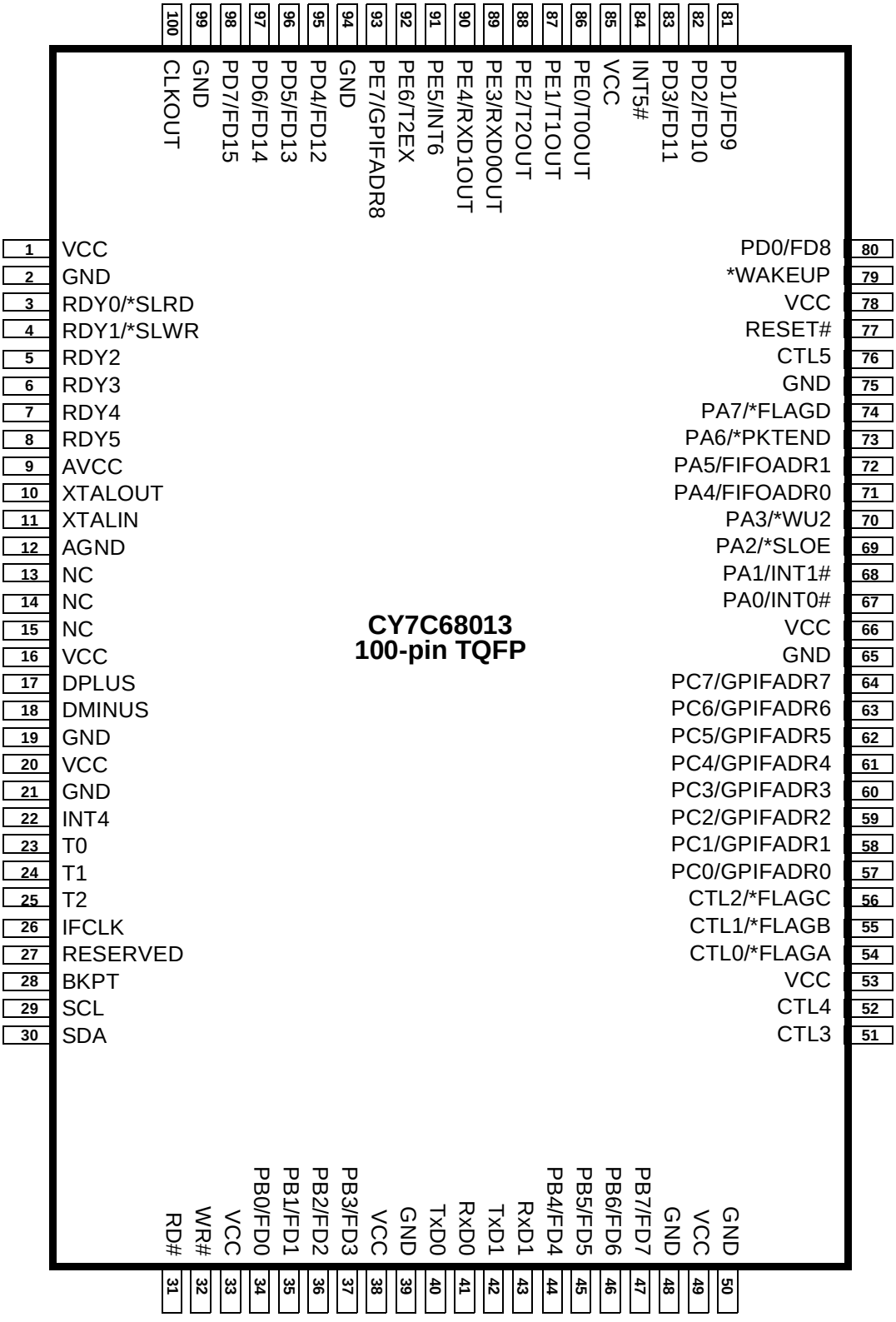


Figure 4-3. CY7C68013 100-pin TQFP Pin Assignment

* denotes programmable polarity.

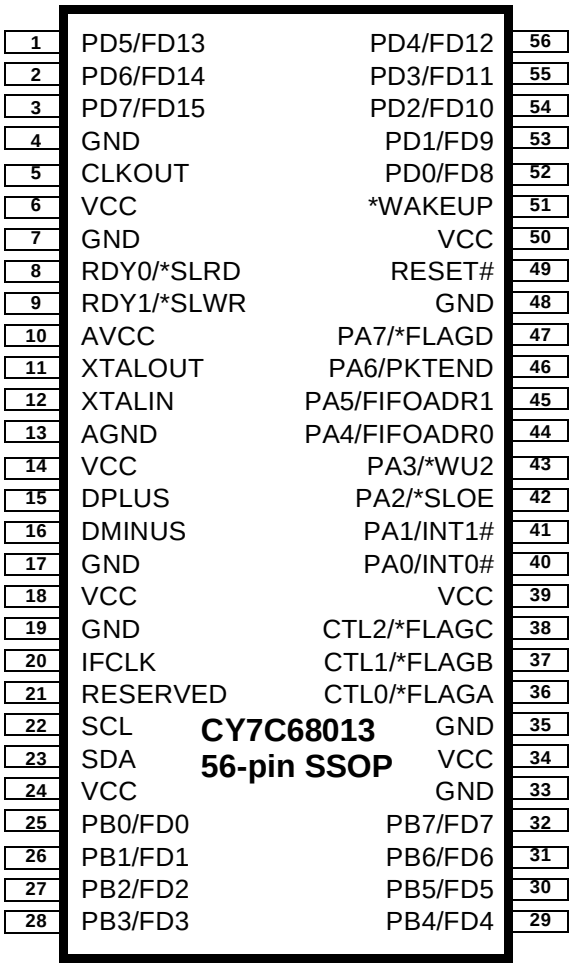


Figure 4-4. CY7C68013 56-pin SSOP Pin Assignment

* denotes programmable polarity.

4.1 CY7C68013 Pin Descriptions

Table 4-1. FX2 Pin Descriptions

128	100	56	Name	Type	Default	Description
10	9	10	AVCC	Power	N/A	**Analog V_{CC}**. This signal provides power to the analog section of the chip.
13	12	13	AGND	Power	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
19	18	16	USBD–	I/O/Z	Z	**USB D– Signal**. Connect to the USB D– signal.
18	17	15	USBD+	I/O/Z	Z	**USB D+ Signal**. Connect to the USB D+ signal.
94			A0	Output	L	**8051 Address Bus**. This bus is driven at all times. When the 8051 is addressing internal RAM it reflects the internal address.
95			A1	Output	L	
96			A2	Output	L	
97			A3	Output	L	
117			A4	Output	L	
118			A5	Output	L	
119			A6	Output	L	
120			A7	Output	L	
126			A8	Output	L	
127			A9	Output	L	
128			A10	Output	L	
21			A11	Output	L	
22			A12	Output	L	
23			A13	Output	L	
24			A14	Output	L	
25			A15	Output	L	
59			D0	I/O/Z	Z	**8051 Data Bus**. This bidirectional bus is high-impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is active only for external bus accesses, and is driven LOW in suspend.
60			D1	I/O/Z	Z	
61			D2	I/O/Z	Z	
62			D3	I/O/Z	Z	
63			D4	I/O/Z	Z	
86			D5	I/O/Z	Z	
87			D6	I/O/Z	Z	
88			D7	I/O/Z	Z	
39			PSEN#	Output	H	**Program Store Enable**. This active-LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x2000-0xFFFF when the EA pin is LOW, or from 0x0000-0xFFFF when the EA pin is HIGH.
34	28		BKPT	Output	L	**Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN=1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12/24/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register.
99	77	49	RESET#	Input	N/A	**Active LOW Reset**. Resets the entire chip. This pin is normally tied to V_{CC} through a 100K resistor, and to GND through a 0.1-µF capacitor.

Table 4-1. FX2 Pin Descriptions (continued)

128	100	56	Name	Type	Default	Description
35			EA	Input	N/A	**External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x1FFF. If EA=0 the 8051 fetches this code from its internal RAM. IF EA=1 the 8051 fetches this code from external memory.
12	11	12	XIN	Input	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and 20-pF capacitor to GND.
11	10	11	XOUT	Output	N/A	**Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and 20-pF capacitor to GND.
1	100	5	CLKOUT	O/Z	48 MHz	12-, 24- or 48-MHz clock, phase locked to the 24-MHz input clock. Output frequency is set by an external EEPROM bit (Config3.2). If no EEPROM is connected to the I^2C compatible port (but the required pull-up resistors are present), the 8051 defaults to 48-MHz operation. The 8051 may three-state this output by setting CPUCS.1=1. The CLKOUT pin may be inverted by setting the boot EEPROM bit CONFIG0.1=1.
Port A						
82	67	40	PA0 or INT0#	I/O/Z	I (PA0)	Multiplexed pin whose function is selected by: PORTACFG.0 **PA0** is a bidirectional IO port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
83	68	41	PA1 or INT1#	I/O/Z	I (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 **PA1** is a bidirectional IO port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0).
84	69	42	PA2 or SLOE	I/O/Z	I (PA2)	Multiplexed pin whose function is selected by two bits: IFCONFIG[1:0]. **PA2** is a bidirectional IO port pin. **SLOE** is an input-only output enable with programmable polarity (FIFOPOLAR.4) for the slave FIFOs connected to FD[0..7] or FD[0..15].
85	70	43	PA3 or WU2	I/O/Z	I (PA3)	Multiplexed pin whose function is selected by: WAKEUP.7 and OEA.3 **PA3** is a bidirectional I/O port pin. **WU2** is an alternate source for **USB Wakeup,** enabled by WU2EN bit (WAKEUP.1) and polarity set by WU2POL (WAKEUP.4). If the 8051 is in suspend and WU2EN=1, a transition on this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Asserting this pin inhibits the chip from suspending, if WU2EN=1.
89	71	44	PA4 or FIFOADR0	I/O/Z	I (PA4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PA4** is a bidirectional I/O port pin. **FIFOADR0** is an input-only address select for the slave FIFOs connected to FD[0..7] or FD[0..15].
90	72	45	PA5 or FIFOADR1	I/O/Z	I (PA5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PA5** is a bidirectional I/O port pin. **FIFOADR1** is an input-only address select for the slave FIFOs connected to FD[0..7] or FD[0..15].

Table 4-1. FX2 Pin Descriptions (continued)

128	100	56	Name	Type	Default	Description
91	73	46	PA6 or PKTEND	I/O/Z	I (PA6)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. **PA6** is a bidirectional I/O port pin. **PKTEND** is an input-only packet end with programmable polarity (FIFOPOLAR.5) for the slave FIFOs connected to FD[0..7] or FD[0..15].
92	74	47	PA7 or FLAGD	I/O/Z	I (PA7)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. **PA7** is a bidirectional I/O port pin. **FLAGD** is a programmable slave-FIFO output status flag signal.
Port B						
44	34	25	PB0 or FD[0]	I/O/Z	I (PB0)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB0** is a bidirectional I/O port pin. **FD[0]** is the bidirectional FIFO/GPIF data bus.
45	35	26	PB1 or FD[1]	I/O/Z	I (PB1)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB1** is a bidirectional I/O port pin. **FD[1]** is the bidirectional FIFO/GPIF data bus.
46	36	27	PB2 or FD[2]	I/O/Z	I (PB2)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB2** is a bidirectional I/O port pin. **FD[2]** is the bidirectional FIFO/GPIF data bus.
47	37	28	PB3 or TXD1 or FD[3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB3** is a bidirectional I/O port pin. **FD[3]** is the bidirectional FIFO/GPIF data bus.
54	44	29	PB4 or FD[4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB4** is a bidirectional I/O port pin. **FD[4]** is the bidirectional FIFO/GPIF data bus.
55	45	30	PB5 or FD[5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB5** is a bidirectional I/O port pin. **FD[5]** is the bidirectional FIFO/GPIF data bus.
56	46	31	PB6 or FD[6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB6** is a bidirectional I/O port pin. **FD[6]** is the bidirectional FIFO/GPIF data bus.
57	47	32	PB7 or FD[7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB7** is a bidirectional I/O port pin. **FD[7]** is the bidirectional FIFO/GPIF data bus.
PORT C						
72	57		PC0 or GPIFADR0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by PORTCCFG.0 **PC0** is a bidirectional I/O port pin. **GPIFADR0** is a GPIF address output pin.
73	58		PC1 or GPIFADR1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by PORTCCFG.1 **PC1** is a bidirectional I/O port pin. **GPIFADR1** is a GPIF address output pin.
74	59		PC2 or GPIFADR2	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by PORTCCFG.2 **PC2** is a bidirectional I/O port pin. **GPIFADR2** is a GPIF address output pin.

Table 4-1. FX2 Pin Descriptions (continued)

128	100	56	Name	Type	Default	Description
75	60		PC3 or GPIFADR3	I/O/Z	I (PC3)	Multiplexed pin whose function is selected by PORTCCFG.3 **PC3** is a bidirectional I/O port pin. **GPIFADR3** is a GPIF address output pin.
76	61		PC4 or GPIFADR4	I/O/Z	I (PC4)	Multiplexed pin whose function is selected by PORTCCFG.4 **PC4** is a bidirectional I/O port pin. **GPIFADR4** is a GPIF address output pin.
77	62		PC5 or GPIFADR5	I/O/Z	I (PC5)	Multiplexed pin whose function is selected by PORTCCFG.5 **PC5** is a bidirectional I/O port pin. **GPIFADR5** is a GPIF address output pin.
78	63		PC6 or GPIFADR6	I/O/Z	I (PC6)	Multiplexed pin whose function is selected by PORTCCFG.6 **PC6** is a bidirectional I/O port pin. **GPIFADR6** is a GPIF address output pin.
79	64		PC7 or GPIFADR7	I/O/Z	I (PC7)	Multiplexed pin whose function is selected by PORTCCFG.7 **PC7** is a bidirectional I/O port pin. **GPIFADR7** is a GPIF address output pin.
PORT D						
102	80	52	PD0 or FD[8]	I/O/Z	I (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[8]** is the bidirectional FIFO/GPIF data bus.
103	81	53	PD1 or FD[9]	I/O/Z	I (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[9]** is the bidirectional FIFO/GPIF data bus.
104	82	54	PD2 or FD[10]	I/O/Z	I (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[10]** is the bidirectional FIFO/GPIF data bus.
105	83	55	PD3 or FD[11]	I/O/Z	I (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[11]** is the bidirectional FIFO/GPIF data bus.
121	95	56	PD4 or FD[12]	I/O/Z	I (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[12]** is the bidirectional FIFO/GPIF data bus.
122	96	1	PD5 or FD[13]	I/O/Z	I (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[13]** is the bidirectional FIFO/GPIF data bus.
123	97	2	PD6 or FD[14]	I/O/Z	I (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[14]** is the bidirectional FIFO/GPIF data bus.
124	98	3	PD7 or FD[15]	I/O/Z	I (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus.
Port E						
108	86		PE0 or T0OUT	I/O/Z	I (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87		PE1 or T1OUT	I/O/Z	I (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active-HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.

Table 4-1. FX2 Pin Descriptions (continued)

128	100	56	Name	Type	Default	Description
110	88		PE2 or T2OUT	I/O/Z	I (PE2)	Multiplexed pin whose function is selected by the PORTECFG.2 bit. **PE2** is a bidirectional I/O port pin. **T2OUT** is the active-HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows.
111	89		PE3 or RXD0OUT	I/O/Z	I (PE3)	Multiplexed pin whose function is selected by the PORTECFG.3 bit. **PE3** is a bidirectional I/O port pin. **RXD0OUT** is an active-HIGH signal from 8051 UART0. If RXD0OUT is selected and UART0 is in Mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1.
112	90		PE4 or RXD1OUT	I/O/Z	I (PE4)	Multiplexed pin whose function is selected by the PORTECFG.4 bit. **PE4** is a bidirectional I/O port pin. **RXD1OUT** is an active-HIGH output from 8051 UART1. When RXD1OUT is selected and UART1 is in Mode 0, this pin provides the output data for UART1 only when it is in sync mode. In Modes 1, 2, and 3, this pin is HIGH.
113	91		PE5 or INT6	I/O/Z	I (PE5)	Multiplexed pin whose function is selected by the PORTECFG.5 bit. **PE5** is a bidirectional I/O port pin. **INT6** is the 8051 INT5 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH.
114	92		PE6 or T2EX	I/O/Z	I (PE6)	Multiplexed pin whose function is selected by the PORTECFG.6 bit. **PE6** is a bidirectional I/O port pin. **T2EX** is an active-high input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON.
115	93		PE7 or GPIFADR8	I/O/Z	I (PE7)	Multiplexed pin whose function is selected by the PORTECFG.7 bit. **PE7** is a bidirectional I/O port pin. **GPIFADR8** is a GPIF address output pin.
4	3	8	RDY0 or SLRD	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY0** is a GPIF input signal. **SLRD** is the input-only read strobe with programmable polarity (FIFOPOLAR.3) for the slave FIFOs connected to FDI[0..7] or FDI[0..15].
5	4	9	RDY1 or SLWR	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY1** is a GPIF input signal.. **SLWR** is the input-only write strobe with programmable polarity (FIFOPOLAR.2) for the slave FIFOs connected to FDI[0..7] or FDI[0..15].
6	5		RDY2	Input	N/A	**RDY2** is a GPIF input signal.
7	6		RDY3	Input	N/A	**RDY3** is a GPIF input signal.
8	7		RDY4	Input	N/A	**RDY4** is a GPIF input signal.
9	8		RDY5	Input	N/A	**RDY5** is a GPIF input signal.
69	54	36	CTL0 or FLAGA	Output	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL0** is a GPIF control output. **FLAGA** is a programmable slave-FIFO output status flag signal. Defaults to PRGFLAG for the FIFO selected by the FIFOADR[1:0] pins.

Table 4-1. FX2 Pin Descriptions (continued)

128	100	56	Name	Type	Default	Description
70	55	37	CTL1 or FLAGB	Output	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL1** is a GPIF control output. **FLAGB** is a programmable slave-FIFO output status flag signal. Defaults to FULL for the FIFO selected by the FIFOADR[1:0] pins.
71	56	38	CTL2 or FLAGC	Output	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL2** is a GPIF control output. **FLAGC** is a programmable slave-FIFO output status flag signal. Defaults to EMPTY for the FIFO selected by the FIFOADR[1:0] pins.
66	51		CTL3	Output	H	**CTL3** is a GPIF control output.
67	52		CTL4	Output	H	**CTL4** is a GPIF control output.
98	76		CTL5	Output	H	**CTL5** is a GPIF control output.
32	26	20	IFCLK	I/O/Z	Z	Interface Clock, used for synchronously clocking data into or out of the slave FIFOs. IFCLK also serves as a timing reference for all slave FIFO control signals and GPIF. When internal clocking, ICONFIG.7=1, is used the IFCLK pin can be configured to output 30/48 MHz by bits IFCONFIG.5 and IFCONFIG.6 and may be inverted by setting the bit IFCONFIG.4=1.
28	22		INT4	Input	N/A	**INT4** is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH.
106	84		INT5#	Input	N/A	**INT5#** is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW.
31	25		T2	Input	N/A	**T2** is the active-HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2=1. When C/T2=0, Timer2 does not use this pin.
30	24		T1	Input	N/A	**T1** is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit.
29	23		T0	Input	N/A	**T0** is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit.
53	43		RXD1	Input	N/A	**RXD1**is an active-HIGH input signal for 8051 UART1, which provides data to the UART in all modes.
52	42		TXD1	Output	H	**TXD1**is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode.
51	41		RXD0	Input	N/A	**RXD0** is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes.
50	40		TXD0	Output	H	**TXD0** is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode.
42			CS#	Output	H	**CS#** is the active-LOW chip select for external memory. If the CS# signal is used, it should be externally pulled up to V_{CC} to ensure that the chip select is inactive (HIGH) at power-on.
41	32		WR#	Output	H	**WR#** is the active-LOW write strobe output for external memory. If the WR# signal is used, it should be externally pulled up to V_{CC} to ensure that the write strobe is inactive at power-on.
40	31		RD#	Output	H	**RD#** is the active-LOW read strobe output for external memory. If the RD# signal is used, it should be externally pulled up to V_{CC} to ensure that the read strobe is inactive at power-on.

Table 4-1. FX2 Pin Descriptions (continued)

128	100	56	Name	Type	Default	Description
38			OE#	Output	H	**OE#** is the active-LOW output enable for external memory. If the OE# signal is used, it should be externally pulled up to V_{CC} to ensure that the output enable is inactive at power-on.
33	27	21	Reserved	Input	N/A	Reserved. Connect to ground.
101	79	51	WAKEUP	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	SCL	OD	Z	**Clock** for the **I^2C compatible interface.** Connect to V_{CC} with a 2.2K resistor, **even if no I^2C comptiable peripheral is attached.**
37	30	23	SDA	OD	Z	**Data** for **I^2C compatible interface**. Connect to V_{CC} with a 2.2K resistor, **even if no I^2C compatible peripheral is attached.**
2	1	6	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
17	16	14	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
26	20	18	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
43	33	24	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
48	38	34	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
64	49	39	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
68	53	50	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
81	66		V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
100	78		V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
107	85		V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
3	2	4	GND	Ground	N/A	Ground.
20	19	7	GND	Ground	N/A	Ground.
27	21	17	GND	Ground	N/A	Ground.
49	39	19	GND	Ground	N/A	Ground.
58	48	33	GND	Ground	N/A	Ground.
65	50	35	GND	Ground	N/A	Ground.
80	65	48	GND	Ground	N/A	Ground.
93	75		GND	Ground	N/A	Ground.
116	94		GND	Ground	N/A	Ground.
125	99		GND	Ground	N/A	Ground.
14	13		NC	N/A	N/A	No-connect. This pin must be left open.
15	14		NC	N/A	N/A	No-connect. This pin must be left open.
16	15		NC	N/A	N/A	No-connect. This pin must be left open.

5.0 Register Summary

FX2 register bit definitions are described in the FX2 TRM in greater detail.

Table 5-1. FX2 Register Summary

Hex	Size	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	Access
E400	128	**GPIF Waveform Data**		D7	D6	D5	D4	D3	D2	D1	D0		
E480	384	reserved											
		General Configuration											
E600	1	CPUCS	Control & Status	0	0	PORTCSTB	CLKSPD1	CLKSPD0	CLKINV	CLKOE	8051RES	00010001	rrrrrrbr
E601	1	IFCONFIG	Interface Configuration	IFCLKSRC	3048MHZ	IFCLKOE	IFCLKPOL	ASYNC	GSTATE	IFCFG1	IFCFG0	11000000	RW
E602	1	FLAGSAB	FIFO FLAGA and FLAGB Assignments	FLAGB3	FLAGB2	FLAGB1	FLAGB0	FLAGA3	FLAGA2	FLAGA1	FLAGA0		
E603	1	FLAGSCD	FIFO FLAGC and FLAGD Assignments	FLAGD3	FLAGD2	FLAGD1	FLAGD0	FLAGC3	FLAGC2	FLAGC1	FLAGC0		
E604	1	FIFORESET	Restore FIFOS to default state	x	x	x	x	x	x	x	x	xxxxxxxx	W
E605	1	BREAKPT	Breakpoint	0	0	0	0	BREAK	BPPULSE	BPEN	0	xxx0xx00	RW
E606	1	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW
E607	1	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW
E608	1	UART230	230 Kbaud clock for T0,T1,T2	0	0	0	0	0	0	230UART1	230UART0	00000000	RW
E609	1	FIFOPOLAR	FIFO polarities	0	0	PKTEND	OE	RD	WR	EF	FF	00000000	RW
E60A	1	REVID	Chip Revision	rv7	rv6	rv5	rv4	rv3	rv2	rv1	rv0	00000000	R
	5	spare											
		Endpoint Configuration											
E610	1	EP1OUTCFG	Endpoint 1-OUT Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	RW
E611	1	EP1INCFG	Endpoint 1-IN Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	RW
E612	1	EP2CFG	Endpoint 2 Configuration	VALID	dir	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	10100010	RW
E613	1	EP4CFG	Endpoint 4 Configuration	VALID	dir	TYPE1	TYPE0	0	0	0	0	10100000	RW
E614	1	EP6CFG	Endpoint 6 Configuration	VALID	dir	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	11100010	RW
E615	1	EP8CFG	Endpoint 8 Configuration	VALID	dir	TYPE1	TYPE0	0	0	0	0	11100000	RW
	2	spare											
E618	1	EP2FIFCFG	Endpoint 2 FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLE-NIN	0	WORDWIDE	00000101	RW
E619	1	EP4FIFCFG	Endpoint 4 FIFO configuration	0	INFM2	OEP2	AUTOOUT	AUTOIN	ZEROLE-NIN	0	WORDWIDE	00000101	RW
E61A	1	EP6FIFCFG	Endpoint 6 FIFO configuration	0	INFM3	OEP3	AUTOOUT	AUTOIN	ZEROLE-NIN	0	WORDWIDE	00000101	RW
E61B	1	EP8FIFCFG	Endpoint 8 FIFO configuration	0	INFM4	OEP4	AUTOOUT	AUTOIN	ZEROLE-NIN	0	WORDWIDE	00000101	RW
	4	spare											
E620	1	EP2PKTLENH	Endpoint 2 Packet Length H (IN only)	0	0	0	0	0	PL10	PL9	PL8	00000010	RW
E621	1	EP2PKTLENL	Endpoint 2 Packet Length L (IN only)	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
E622	1	EP4PKTLENH	Endpoint 4 Packet Length H (IN only)	0	0	0	0	0	0	PL9	PL8	00000010	RW
E623	1	EP4PKTLENL	Endpoint 4 Packet Length L (IN only)	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
E624	1	EP6PKTLENH	Endpoint 6 Packet Length H (IN only)	0	0	0	0	0	PL10	PL9	PL8	00000010	RW
E625	1	EP6PKTLENL	Endpoint 6 Packet Length L (IN only)	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
E626	1	EP8PKTLENH	Endpoint 8 Packet Length H (IN only)	0	0	0	0	0	0	PL9	PL8	00000010	RW
E627	1	EP8PKTLENL	Endpoint 8 Packet Length L (IN only)	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW
	8	spare											
E630	1	EP2PFH	EP2 Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	10000010	RW
E631	1	EP2PFL	EP2 Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E632	1	EP4PFH	EP4 Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10000010	RW
E633	1	EP4PFL	EP4 Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E634	1	EP6PFH	EP6 Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	10000010	RW
E635	1	EP6PFL	EP6 Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E636	1	EP8PFH	EP8 Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10000010	RW
E637	1	EP8PFL	EP8 Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
	8	spare											
E640	1	EP2ISOINPKTS	EP2 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	RW
E641	1	EP4ISOINPKTS	EP4 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	RW
E642	1	EP6ISOINPKTS	EP6 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	RW

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	Access
E643	1	EP8ISOINPKTS	EP8 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	RW
	4	spare											
E648	1	INPACKETEND	Force IN Packet End	0	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	RW
E649	7	spare											
		Interrupts											
E650	1	EP2FLAGIE	Endpoint 2 Flag Interrupt Enable	0	0	0	0	0	PF	EF	FF	00000000	RW
E651	1	EP2FLAGIRQ	Endpoint 2 Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW
E652	1	EP4FLAGIE	Endpoint 4 Flag Interrupt Enable	0	0	0	0	0	PF	EF	FF	00000000	RW
E653	1	EP4FLAGIRQ	Endpoint 4 Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW
E654	1	EP6FLAGIE	Endpoint 6 Flag Interrupt Enable	0	0	0	0	0	PF	EF	FF	00000000	RW
E655	1	EP6FLAGIRQ	Endpoint 6 Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW
E656	1	EP8FLAGIE	Endpoint 8 Flag Interrupt Enable	0	0	0	0	0	PF	EF	FF	00000000	RW
E657	1	EP8FLAGIRQ	Endpoint 8 Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	RW
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW
E659	1	IBNIRQ	IN-BULK-NAK Interrupt Request	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00xxxxxx	RW
E65A	1	EPINGNIE	Endpoint Ping NAK Interrupt Enable	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW
E65B	1	EPINGNIRQ	Endpoint Ping NAK Interrupt Request	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW
E65C	1	USBIE	USB Int Enables	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW
E65D	1	USBIRQ	USB Interrupt Requests	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	xxxxxxxx	RW
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E65F	1	EPIRQ	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E660	1	GPIFIE	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW
E661	1	GPIFIRQ	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	000000xx	RW
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E663	1	USBERRIRQ	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E664	1	ERRCTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	00000100	RW
E665	1	CLRERCT	Clear Error Counter EC[3..0]	x	x	x	x	x	x	x	x	xxxxxxxx	W
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	0	I2V3	I2V2	I2V1	I2V0	0	0	00000000	RW
E667	1	INT4IVEC	Interrupt 4 (FIFOS & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	00000000	RW
E668	1	INTSETUP	Interrupt 2&4 Setup	0	0	0	0	AV2EN	0	INT4IN	AV4EN	00000000	RW
E669	7	spare											
		Input/Output											
E670	1	PORTACFG	I/O PORTA Alternate Configuration	FLAGD	0	0	0	0	0	INT1	INT0	00000000	RW
E671	1	PORTCCFG	I/O PORTC Alternate Configuration	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
E672	1	PORTECFG	I/O PORTE Alternate Configuration	GPIFA8	T2EX	INT6	RxD1OUT	RxD0OUT	T2OUT	T1OUT	T0Out	00000000	RW
E673	5	spare											
E678	1	I2CS	Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbrrrrr
E679	1	I2DAT	Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW
E67A	1	I2CTL	I2C Compatible Control	0	0	0	0	0	0	STOPIE	400kHz	00000000	RW
E67B	1	AUTODATA1	Autoptr1 MOVX access	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E67C	1	AUTODATA2	Autoptr2 MOVX access	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E67D	3	spare											
		USB Control											
E680	1	USBCS	USB Control & Status	HSM	0	0	0	DisCon	NOSYN-SOF	ReNum	SIGRSUME	00000100	rrrrbbbb
E681	1	SUSPEND	Put chip into suspend	x	x	x	x	x	x	x	x	xxxxxxxx	W
E682	1	WAKEUP	Wakeup source and polarity	WU2	WU	WU2POL	WUPOL	0	DPEN	WU2EN	WUEN	00000101	
E683	1	TOGCTL	Toggle Control	Q	S	R	IO	EP3	EP2	EP1	EP0	xxxxxxxx	rbbbbbbb
E684	1	USBFRAMEH	USB Frame count H	0	0	0	0	0	FC10	FC9	FC8	xxxxxxxx	R
E685	1	USBFRAMEL	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxxx	R
E686	1	MICROFRAME	Microframe count, 0-7	0	0	0	0	0	MF2	MF1	MF0	xxxxxxxx	R
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	xxxxxxxx	R
E688	2	spare											
		Endpoints											
E68A	1	EP0BCH	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxxx	RW
E68B	1	EP0BCL	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E68C	1	spare											
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E68E	1	spare											
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	Access
E690	1	EP2BCH	Endpoint 2 Byte Count H	0	0	0	0	0	0	BC9	BC8	xxxxxxxx	RW
E691	1	EP2BCL	Endpoint 2 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E692	2	spare											
E694	1	EP4BCH	Endpoint 4 Byte Count H	0	0	0	0	0	0	0	BC8	xxxxxxxx	RW
E695	1	EP4BCL	Endpoint 4 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E696	2	spare											
E698	1	EP6BCH	Endpoint 6 Byte Count H	0	0	0	0	0	0	BC9	BC8	xxxxxxxx	RW
E699	1	EP6BCL	Endpoint 6 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69A	2	spare											
E69C	1	EP8BCH	Endpoint 8 Byte Count H	0	0	0	0	0	0	0	BC8	xxxxxxxx	RW
E69D	1	EP8BCL	Endpoint 8 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69E	2	spare											
E6A0	1	EP0CS	Endpoint Control and Status	HSNAK	0	0	0	0	0	BUSY	STALL	10000000	RW
E6A1	1	EP1OUTCS	Endpoint 1 OUT Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	RW
E6A2	1	EP1INCS	Endpoint 1 IN Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	RW
E6A3	1	EP2CS	Endpoint 2 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	RW
E6A4	1	EP4CS	Endpoint 4 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	RW
E6A5	1	EP6CS	Endpoint 6 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	RW
E6A6	1	EP8CS	Endpoint 8 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	RW
E6A7	1	EP2FLAGS	Endpoint 2 Flags	0	0	0	0	0	PF	EF	FF	00000011	R
E6A8	1	EP4FLAGS	Endpoint 4 Flags	0	0	0	0	0	PF	EF	FF	00000011	R
E6A9	1	EP6FLAGS	Endpoint 6 Flags	0	0	0	0	0	PF	EF	FF	00000110	R
E6AA	1	EP8FLAGS	Endpoint 8 Flags	0	0	0	0	0	PF	EF	FF	00000110	R
E6AB	1	EP2FIFOBCH	EP2 FIFO total byte count H	0	0	0	BC12	BC11	BC10	BC9	BC8	00000000	R
E6AC	1	EP2FIFOBCL	EP2 FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6AD	1	EP4FIFOBCH	EP4 FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R
E6AE	1	EP4FIFOBCL	EP4 FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6AF	1	EP6FIFOBCH	EP6 FIFO total byte count H	0	0	0	0	BC11	BC10	BC9	BC8	00000000	R
E6B0	1	EP6FIFOBCL	EP6 FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6B1	1	EP8FIFOBCH	EP8 FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R
E6B2	1	EP8FIFOBCL	EP8 FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6B3	1	SUDPTRH	Setup Data Pointer high address byte	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW
E6B4	1	SUDPTRL	Setup Data Pointer low address byte	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW
E6B5	1	SUDPTRAUTO	Setup Data Pointer Auto Mode	0	0	0	0	0	0	0	SDPAUTO	00000001	RW
	2	spare											
E6B8	8	**SETUP Data**	8 bytes of SETUP data	D7	D6	D5	D4	D3	D2	D1	D0		
		GPIF											
E6C0	1	WFSELECT	Waveform Selector	SINGLE-WR 0-3		SINGLERD 0-3		FIFOWR 0-3		FIFORD 0-3		11100100	RW
E6C1	1	IDLE_CS	GPIF Done, GPIF IDLE drive mode	DONE	0	0	0	0	0	0	IDLEDRV	10000000	RW
E6C2	1	IDLE_CTLOUT	Inactive Bus, CTL states	0	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	11111111	RW
E6C3	1	CTLOUTCFG	CTL OUT pin drive	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6C4	1	GPIFADRL	GPIF Address L	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
E6C5	1	GPIFADRH	GPIF Address H	0	0	0	0	0	0	0	GPIFA8	00000000	RW
	10	spare											
E6D0	1	EP2TCH	EP2 GPIF Transaction Count High	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW
E6D1	1	EP2TCL	EP2 GPIF Transaction Count Low	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000000	RW
E6D2	1	EP2FLGSEL	EP2 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6D3	1	EP2PFSTOP	Stop GPIF EP2 transaction on prog. flag	0	0	0	0	0	0	0	EP2PF	00000000	RW
E6D4	1	EP2TRIG	EP2 FIFO Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	spare											
E6D8	1	EP4TCH	EP4 GPIF Transaction Count High	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW
E6D9	1	EP4TCL	EP4 GPIF Transaction Count Low	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000000	RW
E6DA	1	EP4FLGSEL	EP4 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6DB	1	EP4PFSTOP	Stop GPIF EP4 transaction on prog. flag	0	0	0	0	0	0	0	EP4PF	00000000	RW
E6DC	1	EP4TRIG	EP4 FIFO Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	spare											
E6E0	1	EP6TCH	EP6 GPIF Transaction Count High	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW
E6E1	1	EP6TCL	EP6 GPIF Transaction Count Low	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000000	RW
E6E2	1	EP6FLGSEL	EP6 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0	Default	Access
E6E3	1	EP6PFSTOP	Stop GPIF EP6 transaction on prog. flag	0	0	0	0	0	0	0	EP6PF	00000000	
E6E4	1	EP6TRIG	EP6 FIFO Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	spare											
E6E8	1	EP8TCH	EP8 GPIF Transaction Count High	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW
E6E9	1	EP8TCL	EP8GPIF Transaction Count Low	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000000	RW
E6EA	1	EP8FLGSEL	EP8 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6EB	1	EP8PFSTOP	Stop GPIF EP8 transaction on prog. flag	0	0	0	0	0	0	0	EP8PF	00000000	
E6EC	1	EP8TRIG	EP8 FIFO Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	spare											
E6F0	1	SGLDATH	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW
E6F1	1	SGLDATLX	Read/Write GPIF Data L & trigger transac	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E6F2	1	SGLDATLNOX	Read GPIF Data L, no transac trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
E6F3	1	READY	Internal RDY, Sync/Async, RDY pin states	INTRDY	SAS	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	00xxxxxx	bbrrrrrr
E6F4	1	ABORT	Abort GPIF cycles	x	x	x	x	x	x	x	x	xxxxxxxx	W
E6F5	3	spare											
E6F8	1	Reserved		0	0	0	0	0	0	0	0	00000000	RW
E6F9	1	Reserved		0	0	0	0	0	0	0	0	00000000	RW
E6FA	1	Reserved		0	0	0	0	0	0	0	0	00000000	RW
E6FB	1	Reserved		0	0	0	0	0	0	0	0	00000000	RW
E6FC	1	Reserved		0	0	0	0	0	0	0	0	xxxxxxxx	RW
E6FD	1	Reserved		0	0	1	0	0	0	1	1	00100011	RW
E6FE	1	Reserved		0	0	0	0	0	0	0	0	xxxxxxxx	R
E6FF	1	spare											
E700	64	unavailable											
		Endpoint Buffers											
E740	64	EP0BUF	EP0 IN-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E780	64	EP10UTBUF	EP1-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E7C0	64	EP1INBUF	EP1-IN buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
	2048	Reserved											RW
F000	1024	EP2BUF	512/1024-byte EP2 buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F400	1024	EP4BUF	512 byte EP4 buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F800	1024	EP6BUF	512/1024-byte EP6 buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
FC00	1024	EP8BUF	512 byte EP8 buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
xxxx		**I2C Compatible Configuration Byte**		OVRCHRP	DISCON	0	0	CPUFREQ1	CPUFREQ0	CKOUTINV	400KHZ	00001000	n/a

R = all bits read-only
W = all bits write-only

r = read-only bit
w = write only bit
b = both read/write bit

6.0 Absolute Maximum Ratings

Storage Temperature .....–65°C to +150°C
Ambient Temperature with Power Supplied .....0°C to +70°C
Supply Voltage to Ground Potential .....–0.5V to +4.0V
DC Input Voltage to Any Pin..... TBD
DC Voltage Applied to Outputs in High Z State..... –0.5V to V_{CC}+0.5V
Power Dissipation..... TBD mW
Static Discharge Voltage ..... >2000V
Latch-up Current ..... >TBD mA
Max Output Current, per IO port ..... 10 mA
Max Output Current, all five IO ports (128- and 100-pin packages) ..... 50 mA

7.0 Operating Conditions

T_A (Ambient Temperature Under Bias).....0°C to +70°C
Supply Voltage .....+3.0V to +3.6V
Ground Voltage 0V
F_{OSC} (Oscillator or Crystal Frequency) ..... 24 MHz ± 100 ppm

8.0 DC Characteristics

Table 8-1. DC Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage		2		5.25	V
V_{IL}	Input Low Voltage		–0.5		0.8	V
I_I	Input Leakage Current	0< V_{IN} < V_{CC}			±10	µA
V_{OH}	Output Voltage High	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current High				4	mA
I_{OL}	Output Current Low				4	mA
C_{IN}	Input Pin Capacitance				10	pF
I_{SUSP}	Suspend Current	includes 1.5k internal pull-up		250	400	µA
I_{CC}	Supply Current	8051 running, connected to USB		128	TBD	mA

Table 8-2. USB Transceiver

USB 1.1/2.0 compliant.

9.0 AC Electrical Characteristics

9.1 USB Transceiver

USB 2.0 compliant in full and high speed.

9.2 Program Memory Read

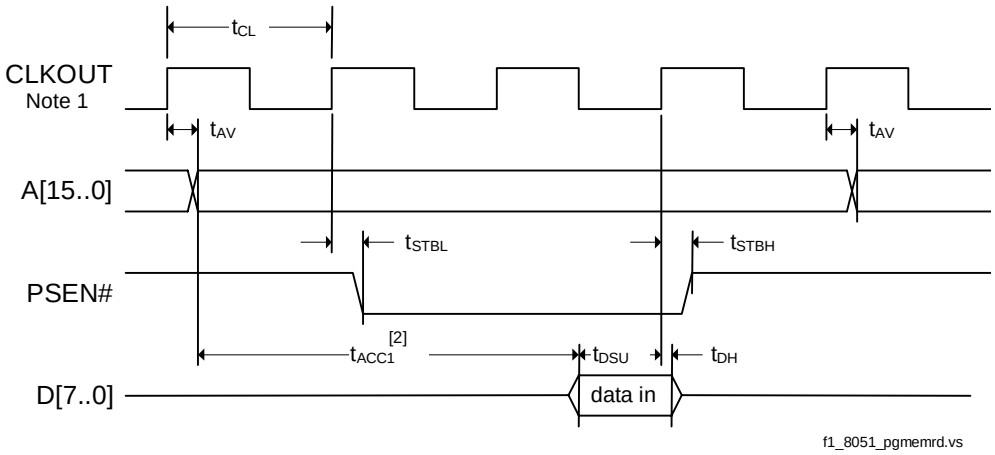


Figure 9-1. Program Memory Read Timing Diagram

Table 9-1. Program Memory Read Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		20.83		ns	48 MHz
			41.66		ns	24 MHz
			83.2		ns	12 MHz
t_{AV}	Delay from Clock to Valid Address	0		11	ns	
t_{STBL}	Clock to PSEN Low	0		6.3	ns	
t_{STBH}	Clock to PSEN High	0		6.3	ns	
t_{DSU}	Data Set-up to Clock			4	ns	
t_{DH}	Data Hold Time	0			ns	

Notes:

1. CLKOUT is shown with positive polarity.
2. t_{ACC1} is computed from the above parameters as follows:
   t_{ACC1}(24 MHz) = 3*t_{CL} – t_{AV} –t_{DSU} = 106 ns
   t_{ACC1}(48 MHz) = 3*t_{CL} – t_{AV} – t_{DSU} = 44 ns

9.3 Data Memory Read

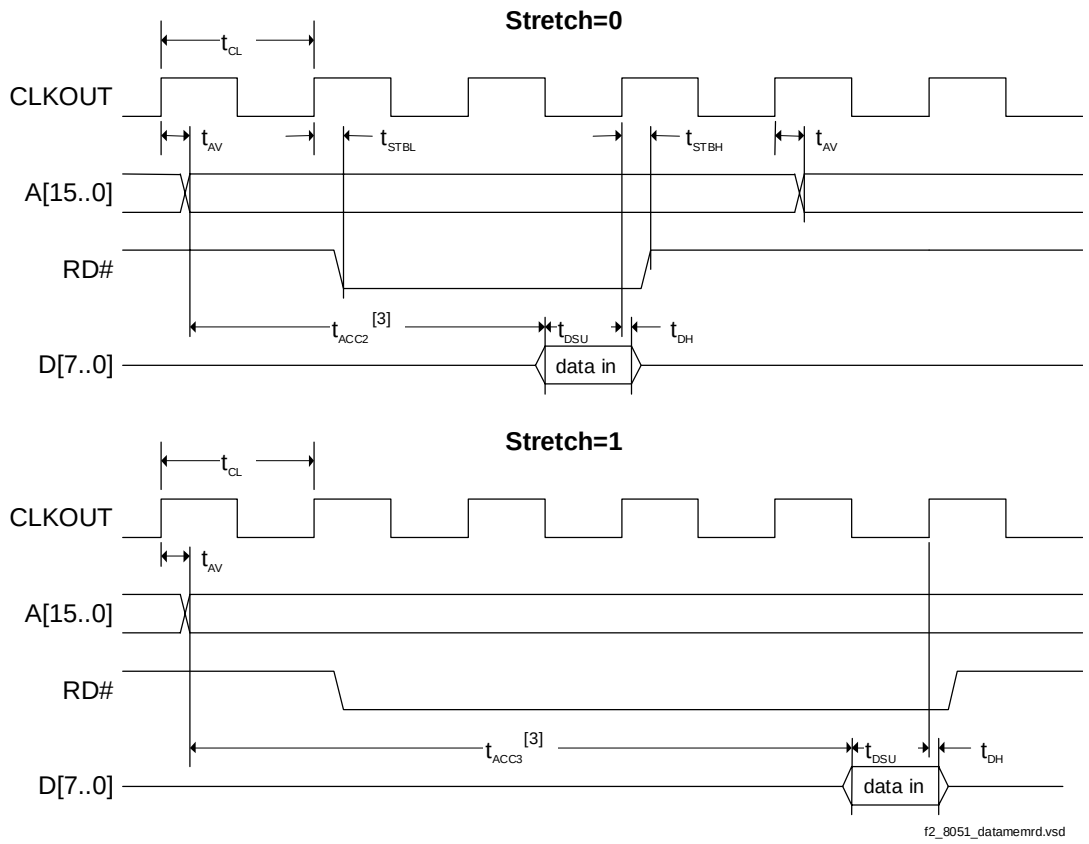


Figure 9-2. Data Memory Read Timing Diagram

Table 9-2. Data Memory Read Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		20.83		ns	48 MHz
			41.66		ns	24 MHz
			83.2		ns	12 MHz
t_{AV}	Delay from Clock to Valid Address	0		11	ns	
t_{STBL}	Clock to RD Low	0		9.3	ns	
t_{STBH}	Clock to RD High	0		9.3	ns	
t_{DSU}	Data Set-up to Clock			4	ns	
t_{DH}	Data Hold Time	0			ns	

Note:

3. t_{ACC2} and t_{ACC3} are computed from the above parameters as follows:
   t_{ACC2}(24 MHz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 106 ns
   t_{ACC2}(48 MHz) = $3*t_{CL} - t_{AV} - t_{DSU}$ = 44 ns

   t_{ACC3}(24 MHz) = $5*t_{CL} - t_{AV} - t_{DSU}$ = 188 ns
   t_{ACC3}(48 MHz) = $5*t_{CL} - t_{AV} - t_{DSU}$ = 85 ns

9.4 Data Memory Write

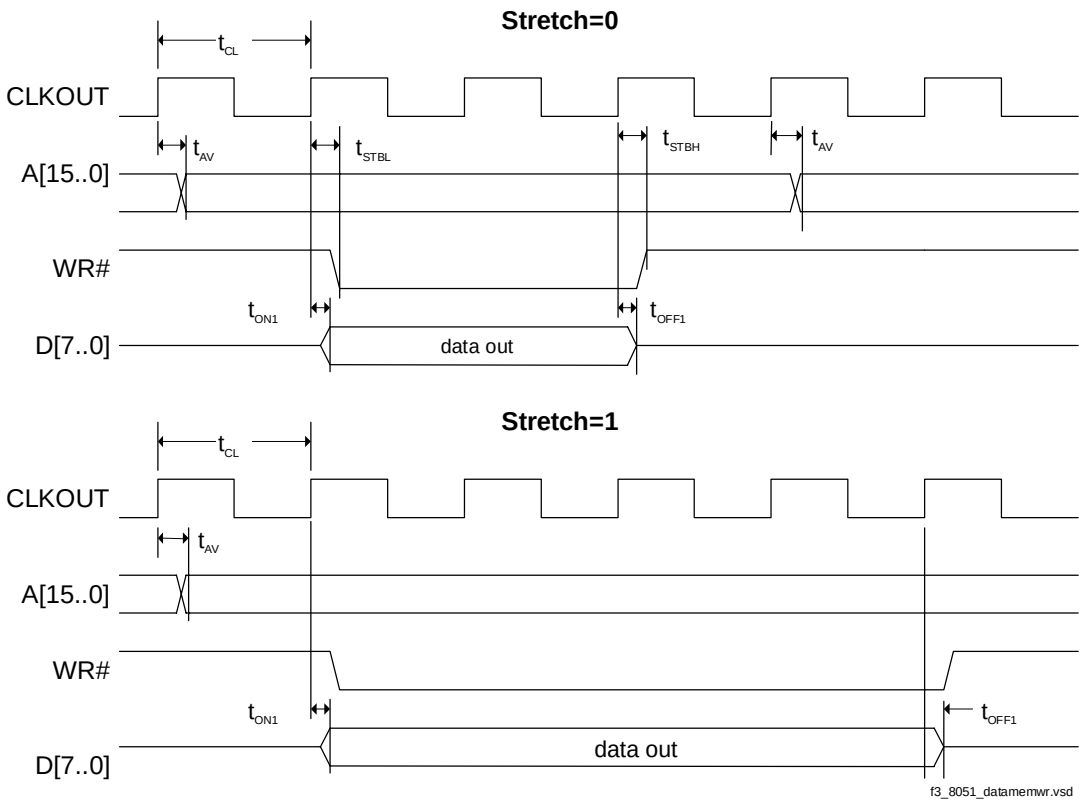


Figure 9-3. Data Memory Write Timing Diagram

Table 9-3. Data Memory Write Parameters

Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	11	ns	
t_{STBL}	Clock to WR Pulse Low	0	10.2	ns	
t_{STBH}	Clock to WR Pulse High	0	10.2	ns	
t_{ON1}	Clock to Data Turn-on	0	10.8	ns	
t_{OFF1}	Clock to Data Hold Time	2	10.8	ns	

9.5 GPIF Synchronous Signals

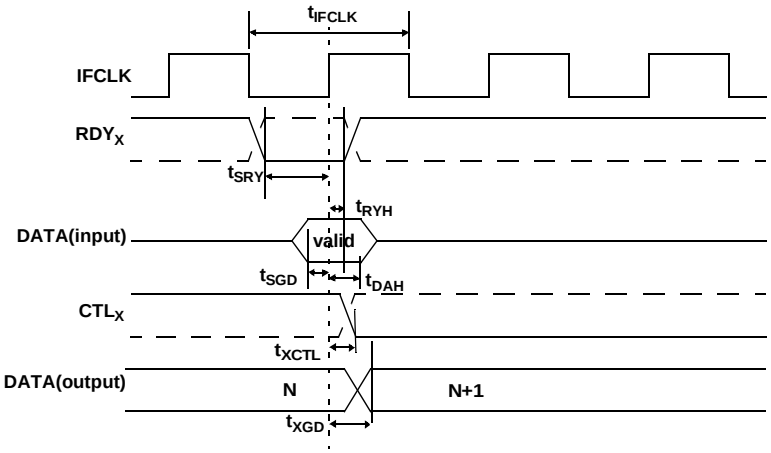


Figure 9-4. GPIF Synchronous Signals Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-4. GPIF Synchronous Signals Parameters[4, 5]

Parameter	Description	Min.	Max.	Unit
t_{SRY}	RDY_X to Clock Set-up Time	17.2		ns
t_{RYH}	Clock to RDY_X	0		ns
t_{SGD}	GPIF Data to Clock Set-up Time	5.2		ns
t_{DAH}	GPIF Data Hold Time	0		ns
t_{XGD}	Clock to GPIF Data Output Propagation Delay		10	ns
t_{XCTL}	Clock to CTL_X Output Propagation Delay		6	ns

Notes:
4. GPIF asynchronous RDY_x signals have a minimum set-up time of 50 ns when using internal 48-MHz IFCLK.
5. IFCLK must not exceed 48 MHz.

9.6 Slave FIFO Synchronous Read

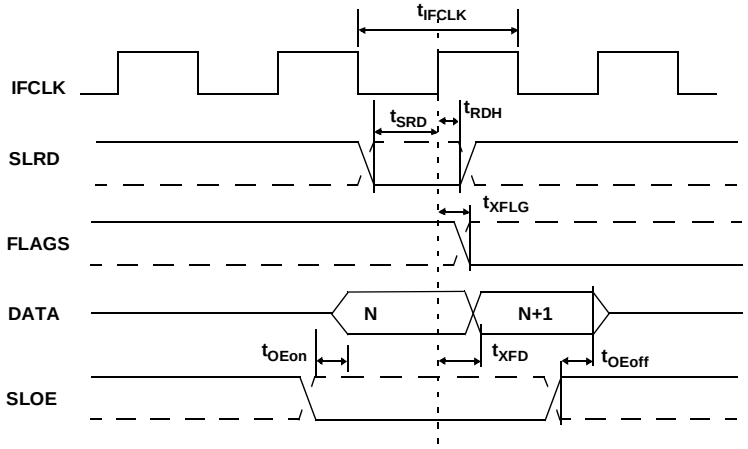


Figure 9-5. Slave FIFO Synchronous Read Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-5. Slave FIFO Synchronous Read Parameters[5]

Parameter	Description	Min.	Max.	Unit
t_{SRD}	SLRD to Clock Set-up Time	17.2		ns
t_{RDH}	Clock to SLRD Hold Time	0		ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid		7.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold		7.5	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay		5.3	ns
t_{XFD}	Clock to FIFO Data Output Propagation Delay		9.9	ns

9.7 Slave FIFO Asynchronous Read

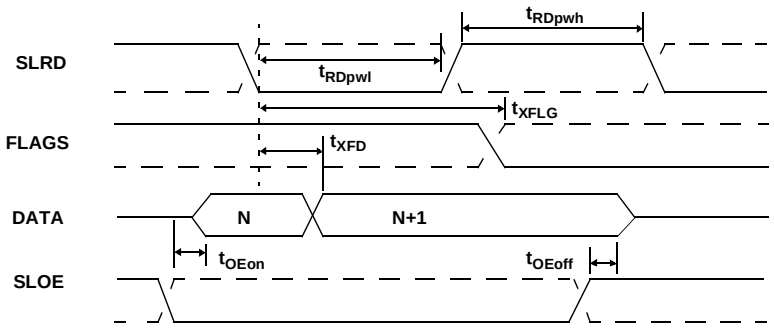


Figure 9-6. Slave FIFO Asynchronous Read Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-6. Slave FIFO Asynchronous Read Parameters[6]

Parameter	Description	Min.	Max.	Unit
t_{RDpwl}	SLRD Pulse Width Low	50		ns
t_{RDpwh}	SLRD Pulse Width High	50		ns
t_{XFLG}	SLRD to FLAGS Output Propagation Delay		70	ns
t_{XFD}	SLRD to FIFO Data Output Propagation Delay		11.2	ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid		7.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold		7.5	ns

Note:

6. Slave FIFO asynchronous parameter values are using internal IFCLK setting at 48 MHz.

9.8 Slave FIFO Synchronous Write

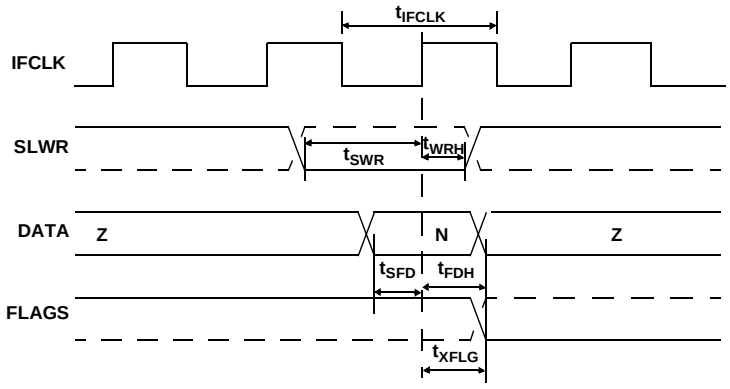


Figure 9-7. Slave FIFO Synchronous Write Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-7. Slave FIFO Synchronous Write Parameters[5]

Parameter	Description	Min.	Max.	Unit
t_{SWR}	SLWR to Clock Set-up Time	10.4		ns
t_{WRH}	Clock to SLWR Hold Time	0		ns
t_{SFD}	FIFO Data to Clock Set-up Time	5.1		ns
t_{FDH}	Clock to FIFO Data Hold Time	0		ns
t_{XFLG}	Clock to FLAGS Output Propagation Time		5.3	ns

9.9 Slave FIFO Asynchronous Write

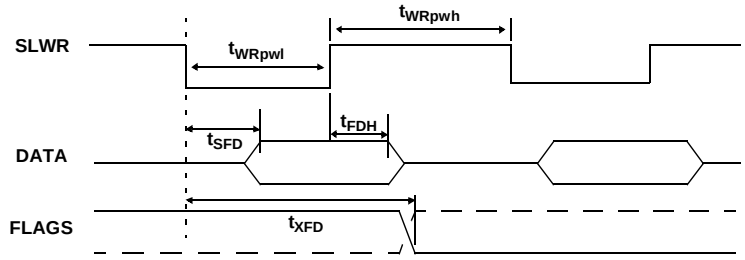


Figure 9-8. Slave FIFO Asynchronous Write Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-8. Slave FIFO Asynchronous Write Parameters[6]

Parameter	Description	Min.	Max.	Unit
t_{WRpwl}	SLWR Pulse Low	50		ns
t_{WRpwh}	SLWR Pulse High	70		ns
t_{SFD}	SLWR to FIFO DATA Set-up Time	2.7		ns
t_{FDH}	FIFO DATA to SLWR Hold Time	2.7		ns
t_{XFD}	SLWR to FLAGS Output Propagation Delay		70	ns

9.10 Slave FIFO Synchronous Packet End Strobe

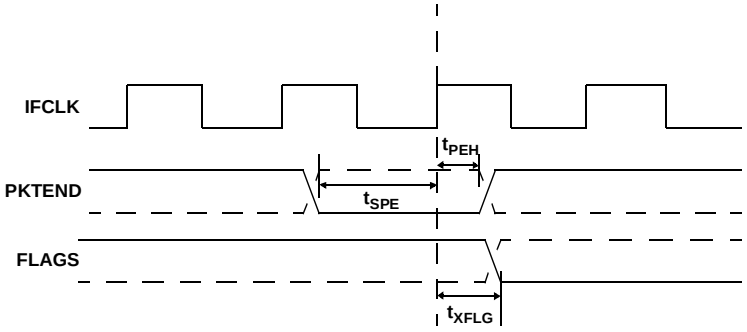


Figure 9-9. Slave FIFO Synchronous Packet End Strobe Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-9. Slave FIFO Synchronous Packet End Strobe Parameters[5]

Parameter	Description	Min.	Max.	Unit
t_{SPE}	PKTEND to Clock Set-up Time	10.4		ns
t_{PEH}	Clock to PKTEND Hold Time	0		ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay		5.3	ns

9.11 Slave FIFO Asynchronous Packet End Strobe

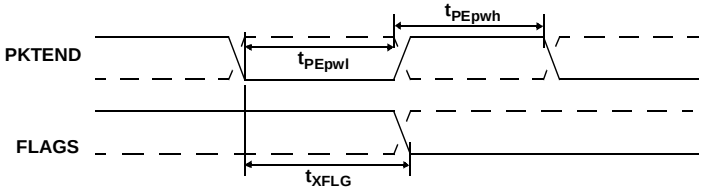


Figure 9-10. Slave FIFO Asynchronous Packet End Strobe Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-10. Slave FIFO Asynchronous Packet End Strobe Parameters[6]

Parameter	Description	Min.	Max.	Unit
t_{PEpwl}	PKTEND Pulse Width Low	50		ns
t_{PWpwh}	PKTEND Pulse Width High	50		ns
t_{XFLG}	PKTEND to FLAGS Output Propagation Delay		70	ns

9.12 Slave FIFO Output Enable

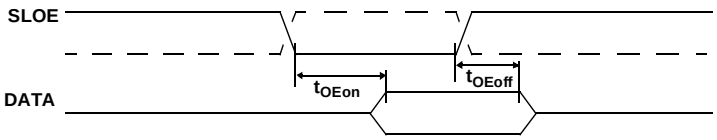


Figure 9-11. Slave FIFO Output Enable Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-11. Slave FIFO Output Enable Parameters

Parameter	Description	Min.	Max.	Unit
t_{OEon}	SLOE Assert to FIFO DATA Output		7.5	ns
t_{OEoff}	SLOE Deassert to FIFO DATA Hold		7.5	ns

9.13 Slave FIFO Address to Flags/Data

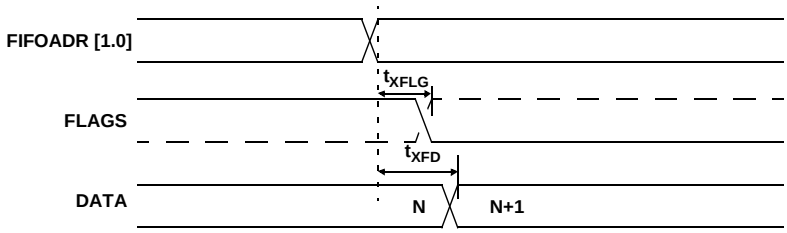


Figure 9-12. Slave FIFO Address to Flags/Data Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-12. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Min.	Max.	Unit
t_{XFLG}	FIFOADR[1:0] to FLAGS Output Propagation Delay		9.1	ns
t_{XFD}	FIFOADR[1:0] to FIFODATA Output Propagation Delay		13.9	ns

9.14 Slave FIFO Synchronous Address

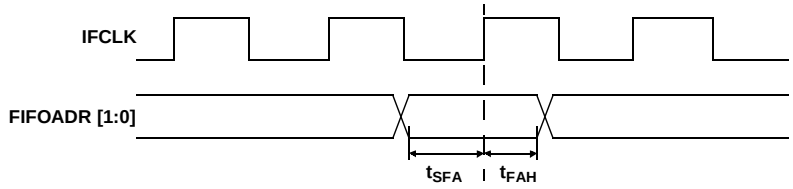


Figure 9-13. Slave FIFO Synchronous Address Timing Diagram

Table 9-13. Slave FIFO Synchronous Address Parameters[5]

Parameter	Description	Min.	Max.	Unit
t_{SFA}	FIFOADR[1:0] to Clock Set-up Time	19.2		ns
t_{FAH}	Clock to FIFOADR[1:0] Hold Time	0		ns

9.15 Slave FIFO Asynchronous Address

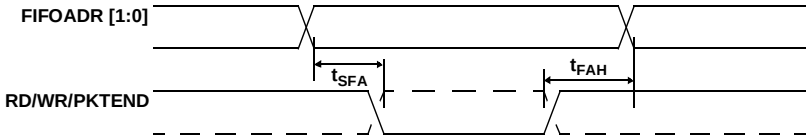


Figure 9-14. Slave FIFO Asynchronous Address Timing Diagram

* dashed lines denote signals with programmable polarity

Table 9-14. Slave FIFO Asynchronous Address Parameters[6]

Parameter	Description	Min.	Max.	Unit
t_{SFA}	FIFOADR[1:0] to RD/WR/PKTEND Set-up Time	0		ns
t_{FAH}	RD/WR/PKTEND to FIFOADR[1:0] Hold Time	0		ns

10.0 Ordering Information

Table 10-1. Ordering Information

Ordering Code	Package Type	RAM Size	# Prog I/Os	8051 Address /Data Busses
CY7C68013-128AC	128 TQFP	8K	40	16/8 bit
CY7C68013-100AC	100 TQFP	8K	40	-
CY7C68013-56PVC	56 SSOP	8K	24	-
CY3681	EZ-USB FX2 Xcelerator Development Kit			

Document #: 38–00929–B

11.0 Package Diagrams

The FX2 is available in three packages:

- 56-pin SSOP
- 100-pin TQFP
- 128-pin TQFP

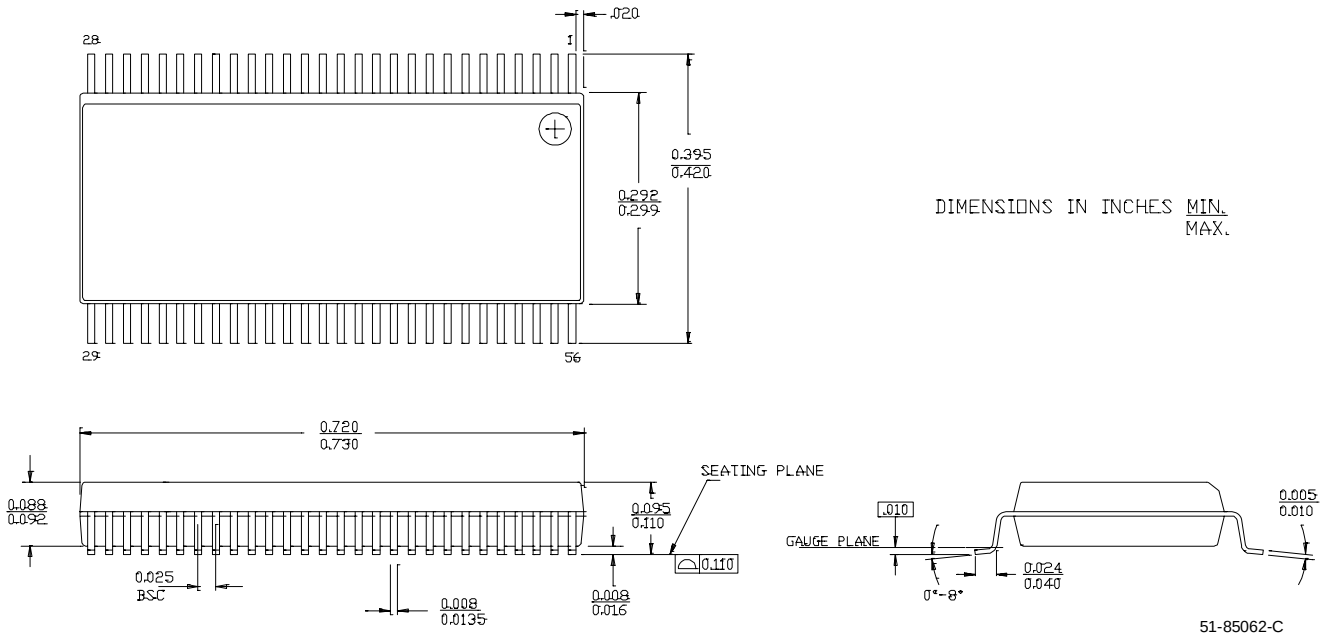


Figure 11-1. 56-Lead Shrunk Small Outline Package O56

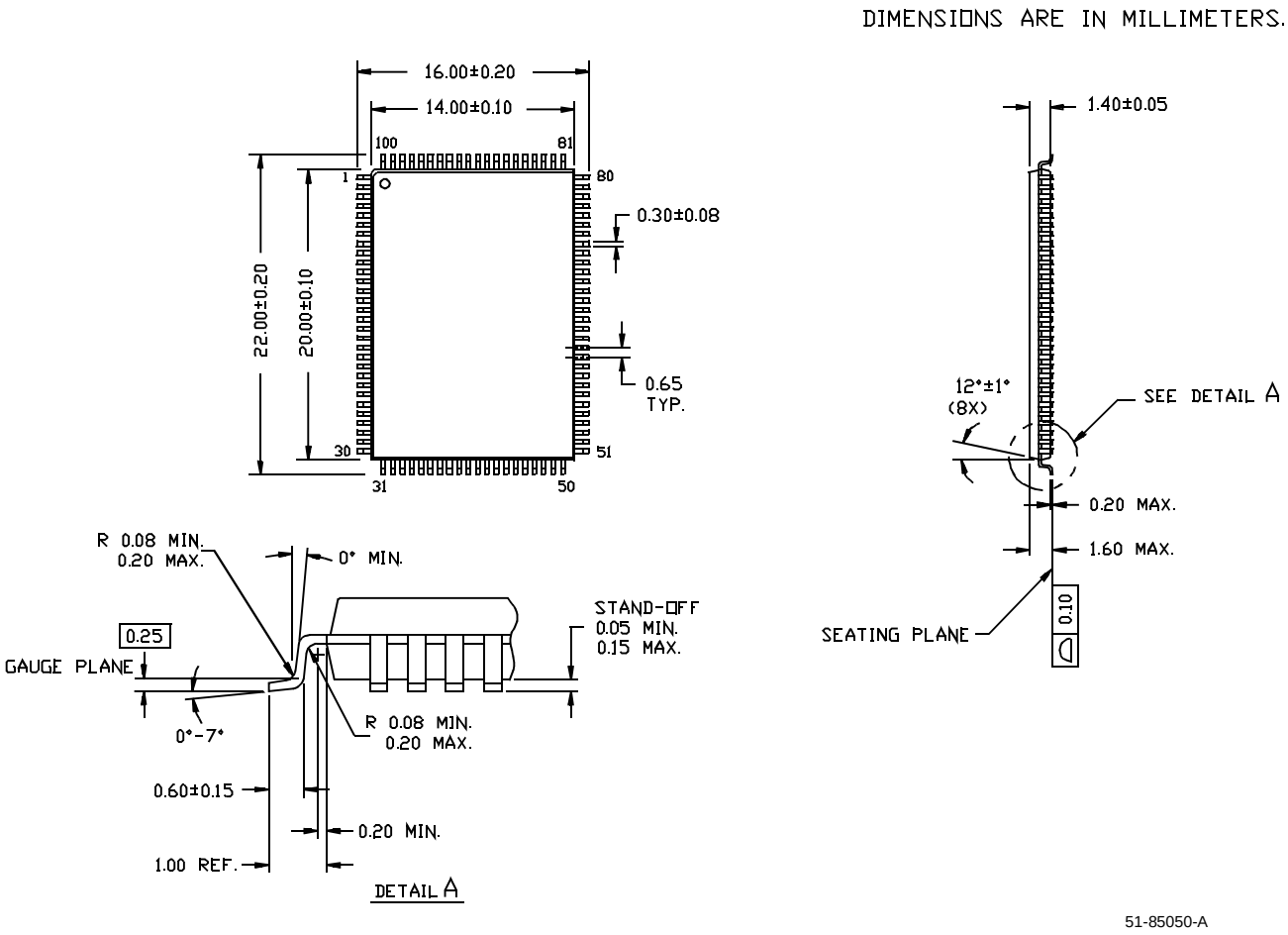


Figure 11-2. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

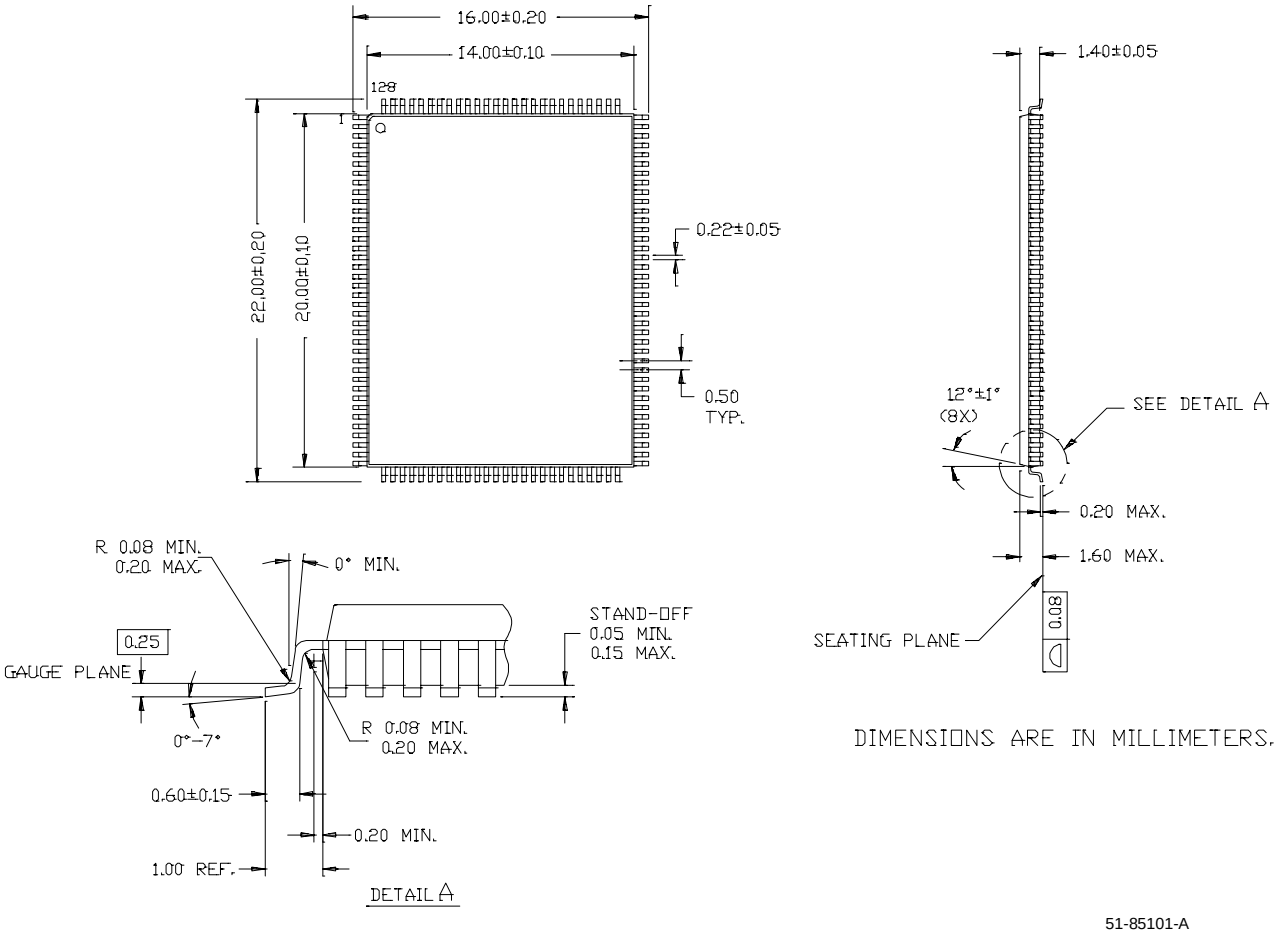


Figure 11-3. 128-Lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A128

12.0 Document Revision History

Table 12-1. Revision History

Description	Date / Revision
First Draft	March 8, 2000
updated 100-pin TQFP pin out	June 23, 2000
added mechanical drawings, timing diagrams, edits throughout	July 24, 2000
edits for pinout(s) naming/description, some DC / AC char.	July 25, 2000
edit pin naming corrections / typos	July 27, 2000
edits, from internal feedback, throughout added register summary updated timing diagrams updated 100-pin mechanical added some DC/AC spec's	July 28-Sept. 14, 2000
edits throughout	November 3, 2000