CY7C6981
Bluetooth™ Link Controller + Radio

Cypress Semiconductor Corporation • 3901 North First Street • San Jose • CA 95134 • 408-943-2600
Document #: 38-11002 Rev. ** Revised March 29, 2001

Disclaimer:

This document is subject to change, and may be found to contain errors of omission or changes in parameters. The reader, as an early developer of Bluetooth™ and under a nondisclosure agreement with Cypress, is encouraged to provide any information to Cypress that may be used to improve this document.

For feedback or technical support regarding Cypress Bluetooth products please E-mail Cypress Bluetooth applications engineers at btapps@cypress.com

TABLE OF CONTENTS

LIST OF FIGURES

1.0 Features

The Cypress CY7C6981 Integrated Bluetooth Link Controller and Radio provides a solution for Bluetooth wireless communications. The CY7C6981 contains a 2.4 GHz radio transceiver, a GFSK modem, and complete link controller in a small highly integrated package.

- **RF transceiver and baseband controller functions in a single package**
- **Fully compliant with the Bluetooth Specification 1.1**
- **Minimum of external components for ease of implementation and manufacturing**
- **+4 dBm transmit power for Bluetooth class 2 devices**
- **Support for class 1 device with external power amplifier**
- **–82 dBm receive sensitivity**
- **RSSI & AGC for enhanced noise immunity and higher node densities**
- **Transmit power control in 8 steps**
- **Supports all Bluetooth low power operating modes**
- **Supports all Bluetooth ACL and SCO connection types and packets**
- **Provides Bluetooth encryption, data whitening, FEC & HEC functionality**
- **723.2 Kbps sustainable throughput**
- **Integrated 8 KBytes buffer**
- **External Microprocessor interface**
- **PCM Audio Interface**
- **Capture timer**
- **10 mm x 10 mm x 1.2 mm 81 pin FBGA Package**
- **Cypress world-class development kit & software support**

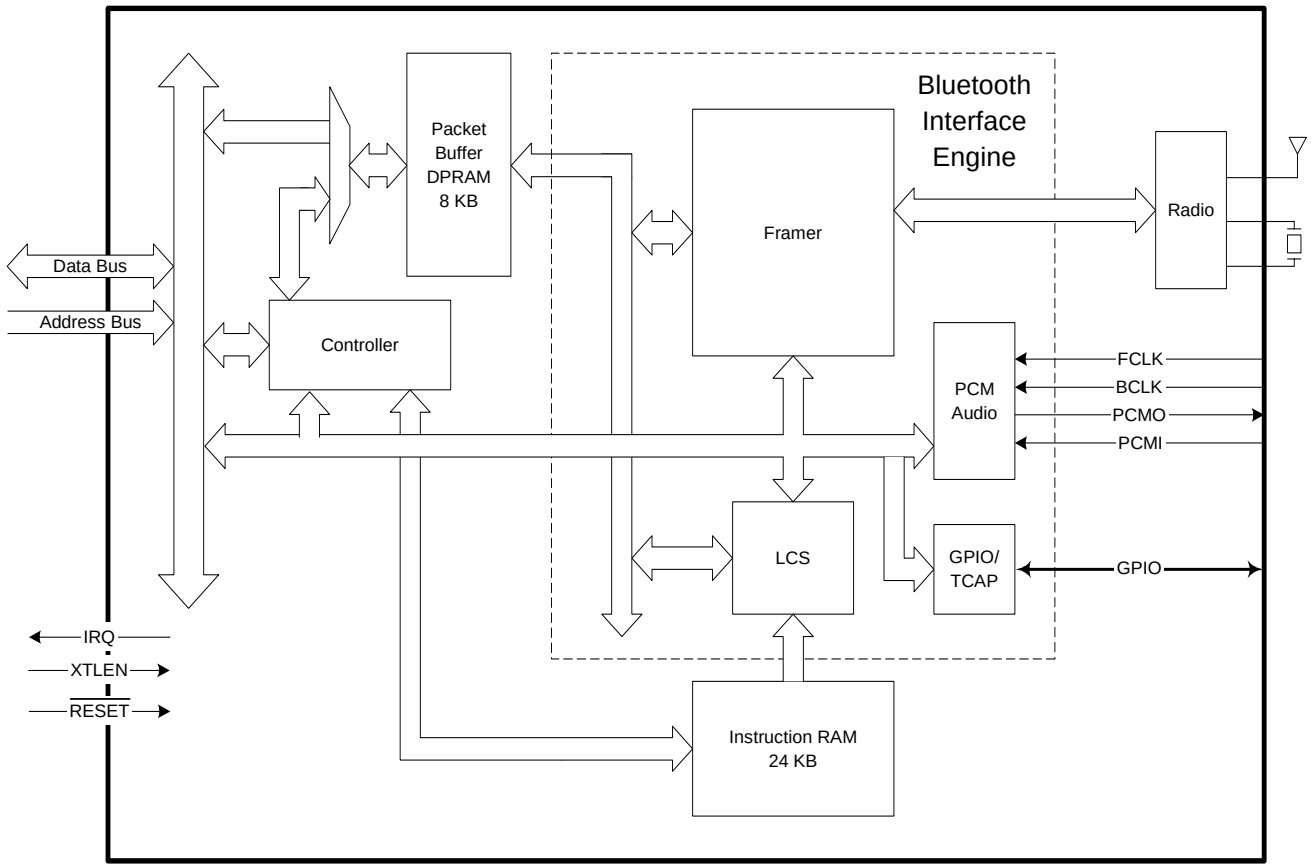


Figure 1-1. CY7C6981 Block Diagram

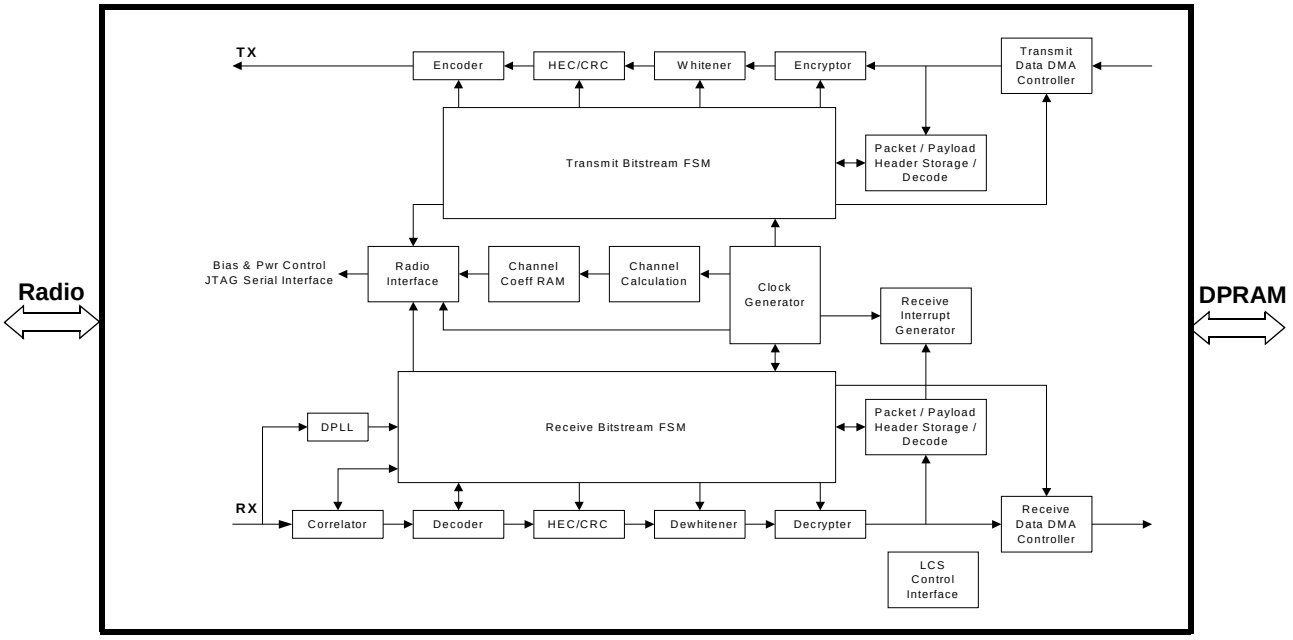


Figure 1-2. Framer Block Diagram

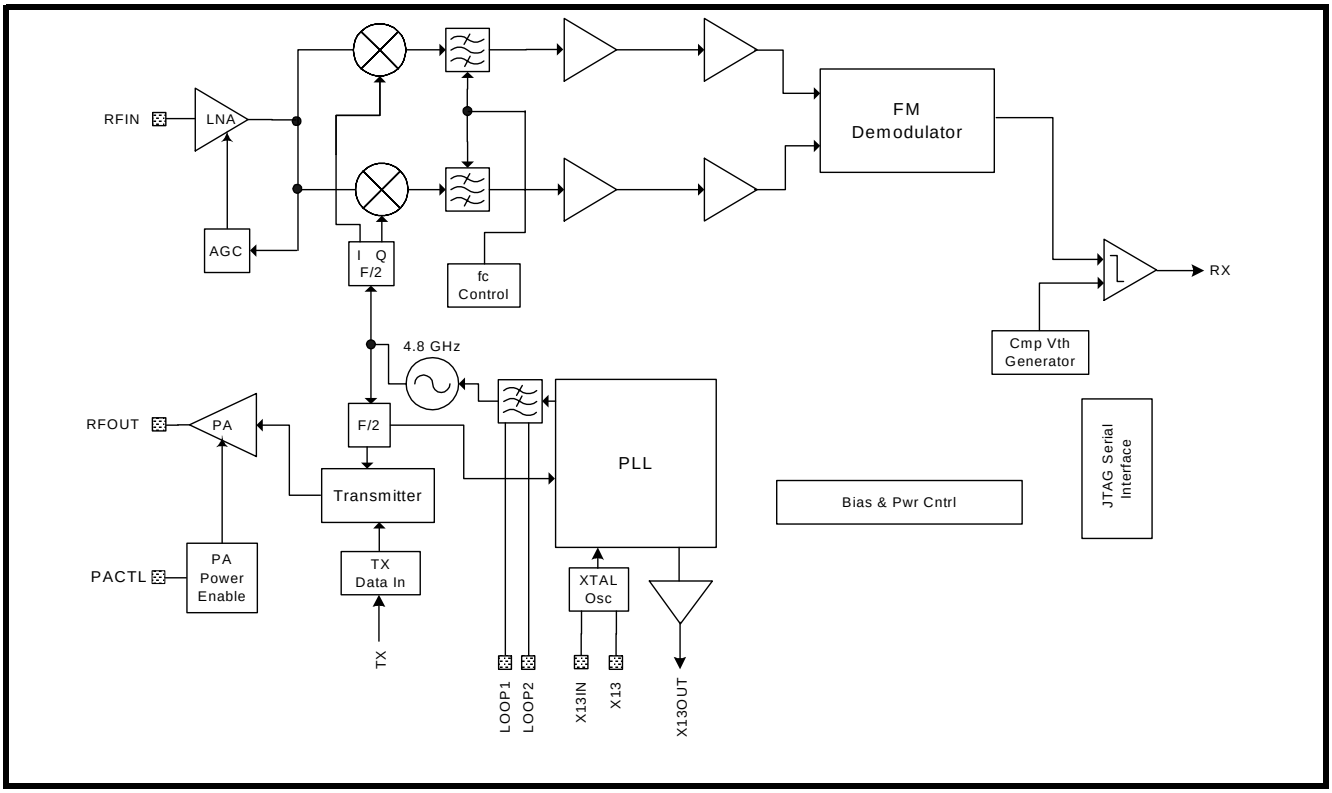


Figure 1-3. Radio Block Diagram

1.1 Example Applications

The high integrated CY7C6981 provides end-to-end functionality and is targeted for host-based Bluetooth applications.

- Interconnect desktop and laptop PC's without cables
- Cell phone handsets
- PDA's
- Cameras
- Scanners
- Printers
- MP3 Players
- Modems
- Access Points

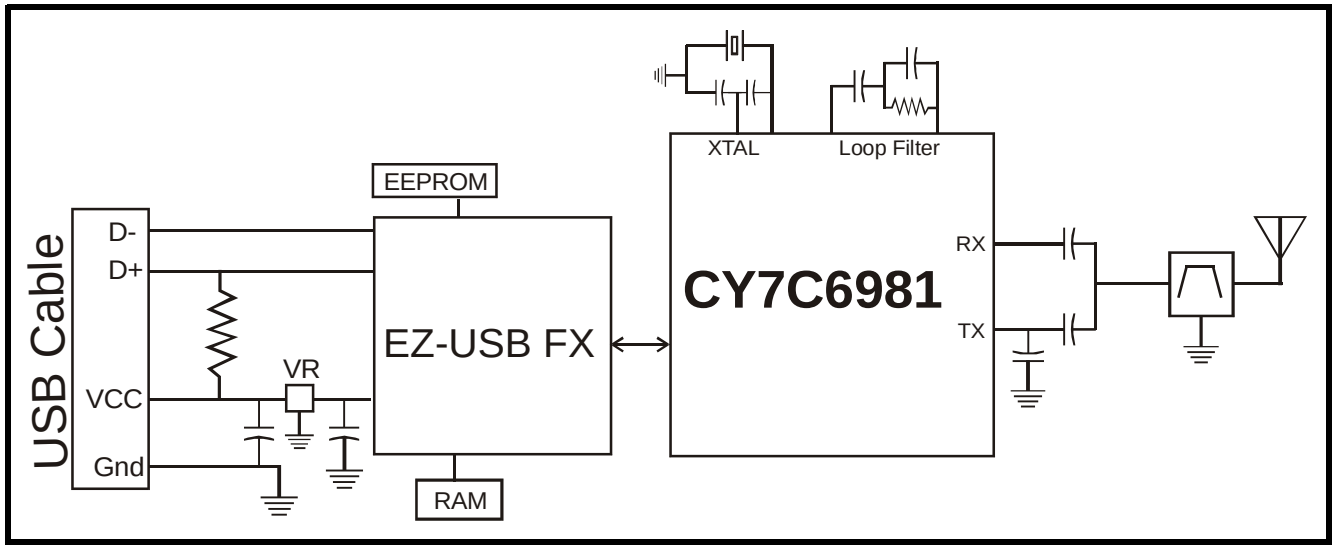


Figure 1-4. USB to Bluetooth™ application block diagram

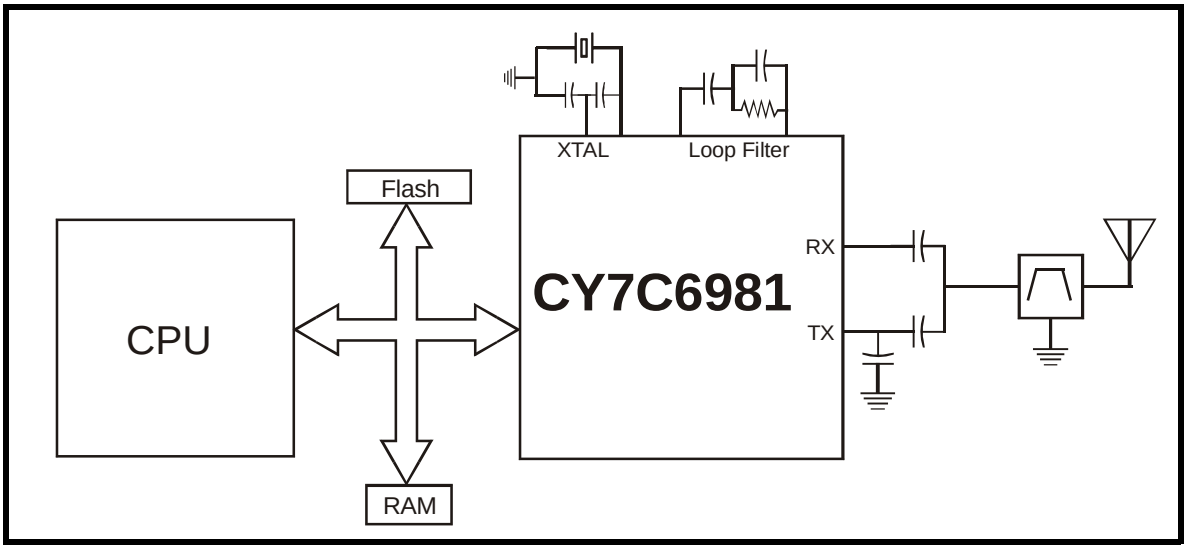


Figure 1-5. General Microprocessor application block diagram

1.2 CY7C6981 Pin Description

Ball	Name	Type	Default	Description
Control and Test Interface				
J7	$\overline{\text{RESET}}$	Input	N/A	**Active LOW Reset**. Resets the entire chip. This pin is normally tied to V_{CC} through a 10K resistor, and to GND through a 1-µF capacitor.
A9	CLKOUT	Output		**ClkOut.** It is a buffered 13-MHz clock that can be used for general purpose.
J9	$\overline{\text{TESTMODE}}$	Input	N/A	**Testmode.** This pin selects test mode for the chip. It has to be tied to V_{CC} for normal operation.
External Processor Interface				
A8	A0	Input	N/A	**Address bus**. This bus is connected to the external microprocessor address bus to address internal memory and register.
A7	A1	Input	N/A	
B7	A2	Input	N/A	
B8	A3	Input	N/A	
B9	A4	Input	N/A	
C9	A5	Input	N/A	
C8	A6	Input	N/A	
C7	A7	Input	N/A	
D7	A8	Input	N/A	
D8	A9	Input	N/A	
D9	A10	Input	N/A	
E9	A11	Input	N/A	
E7	A12	Input	N/A	
C6	D0	I/O/Z	Z	**Data bus.** This bidirectional bus is the external microprocessor Data bus connection to access Data memory and registers. The Data bus is high-impedance when inactive, output for bus reads, and input for bus writes.
B6	D1	I/O/Z	Z	
A6	D2	I/O/Z	Z	
A5	D3	I/O/Z	Z	
B5	D4	I/O/Z	Z	
C5	D5	I/O/Z	Z	
C4	D6	I/O/Z	Z	
C3	D7	I/O/Z	Z	
F7	$\overline{\text{CE0}}$	Input	N/A	**Chip Select0, 1, 2**. These signals are Chip Select. The global CY7C6981 Chip Enable is generated internally by NANDing $\overline{\text{CE0}}$,CE1,$\overline{\text{CE2}}$.
G7	CE1	Input	N/A	
G6	$\overline{\text{CE2}}$	Input	N/A	
J8	$\overline{\text{WE}}$	Input	N/A	**$\overline{\text{WE}}$** is the active-LOW write strobe used by the external microprocessor to write the CY7C6981 registers and memory.
H8	$\overline{\text{OE}}$	Input	N/A	**$\overline{\text{OE}}$** is the active-LOW read strobe used by the external microprocessor to read the CY7C6981 registers and memory.
H7	IRQ	Output/Z	Z	**IRQ** is the interrupt request for the external microcontroller
Radio Interface				
J5	RFOUT	Output	N/A	**Antenna Output**. Modulated RF signal to be transmitted.
H1	RFIN	Input	N/A	**Antenna Input**. Modulated RF signal received.
E1	LOOP1	Output	N/A	**Loop Filter Output**. Port for external loop filter components.

1.2 CY7C6981 Pin Description (continued)

Ball	Name	Type	Default	Description
F1	LOOP2	Input	N/A	**Loop Filter Input**. Port for external loop filter components.
H6	PACTL	Output	0	**External PA Enable is** used to enable the external power amplifier (PA). Default is zero, external PA disabled.
CLOCK				
H9	X13IN	Input	N/A	**Crystal Input**. Connect this pin to a 13 MHz clock or connect a crystal to GND and 47 pF capacitor to X13.
G9	X13			**Crystal Oscillator feedback**. Connect 14 pF capacitor to GND.
H8	XTLEN	Input	N/A	**Crystal Oscillator Enable**. Provides the capability to powers down the device.
General Purpose I/O				
E3	GPIO0 CAP_TIM_A	I/O/Z	I	Multiplexed pin whose function is selected by setting bit(s) in I/O Configuration Register. **GPIO0** is a bi-directional IO port pin. **Capture Timer A** input.
D3	GPIO1 CAP_TIM_B	I/O/Z	I	Multiplexed pin whose function is selected by setting bit(s) in I/O Configuration Register. **GPIO1** is a bi-directional IO port pin. **Capture Timer B** input.
B3	GPIO2	I/O/Z	I	**GPIO2** is a bi-directional IO port pin.
A3	GPIO3	I/O/Z	I	**GPIO3** is a bidirectional I/O port pin.
A2	GPIO4	I/O/Z	I	**GPIO4** is a bi-directional I/O port pin.
A1	GPIO5	I/O/Z	I	**GPIO5** is a bi-directional I/O port pin.
PCM Audio Interface				
C1	PCMO	Output	0	**PCM Data Output** is used to transmit data to a PCM Master device. PCMO is synchronous to BCLK.
C2	PCMI	Input	N/A	**PCM Data Input** is used to receive data from a PCM Master device. PCMI is synchronous to BCLK.
B1	FCLK	Input	N/A	**Frame Sync Clock** is used for Frame Synchronization. The Frame Sync rate is 8 KHz.
B2	BCLK	Input	N/A	**Serial Bit Clock** provides the clock synchronization for the Serial Data transfer. The Bit Clock rate is 512 Kbps

1.2 CY7C6981 Pin Description (continued)

Ball	Name	Type	Default	Description
Vcc and GND pins				
A4	V_{CC}	Power	N/A	**V_{CC}** Power supply for digital logic.
B4	V_{CC}	Power	N/A	
D1	V_{CC}	Power	N/A	
D2	V_{CC}	Power	N/A	
E8	V_{CC}	Power	N/A	
F8	V_{CC}	Power	N/A	
F9	V_{CC}	Power	N/A	
G1	RFVCCA	Power	N/A	**RFVCCA** Power supply for PA and LNA.
J6	RFVCCD	Power	N/A	**RFVCCD** Power supply for digital logic in RF block.
E2	RFVCCS	Power	N/A	**RFVCCS** Power supply for Synthesizer.
G5	RFVCCB	Power	N/A	**RFVCCB** Power supply for Baseband interface.
D4	GND	Ground	N/A	**Ground**
D5	GND	Ground	N/A	**Ground**
D6	GND	Ground	N/A	**Ground**
E4	GND	Ground	N/A	**Ground**
E5	GND	Ground	N/A	**Ground**
E6	GND	Ground	N/A	**Ground**
F4	GND	Ground	N/A	**Ground**
F5	GND	Ground	N/A	**Ground**
F6	GND	Ground	N/A	**Ground**
F2	RFGND	Ground	N/A	**Ground**
F3	RFGND	Ground	N/A	**Ground**
G2	RFGND	Ground	N/A	**Ground**
G3	RFGND	Ground	N/A	**Ground**
G4	RFGND	Ground	N/A	**Ground**
H2	RFGND	Ground	N/A	**Ground**
H3	RFGND	Ground	N/A	**Ground**
H4	RFGND	Ground	N/A	**Ground**
H5	RFGND	Ground	N/A	**Ground**
J1	RFGND	Ground	N/A	**Ground**
J2	RFGND	Ground	N/A	**Ground**
J3	RFGND	Ground	N/A	**Ground**
J4	RFGND	Ground	N/A	**Ground**

	1	2	3	4	5	6	7	8	9	
A	GPIO5	GPIO4	GPIO3	VCC	D3	D2	A9	A8	CLKOUT	A
B	FCLK	BCLK	GPIO2	VCC	D4	D1	A10	A7	A0	B
C	PCMO	PCMI	D7	D6	D5	D0	A11	A6	A1	C
D	VCC	VCC	GPIO1	GND	GND	GND	A12	A5	A2	D
E	LOOP1	RFVCCS	GPIO0	GND	GND	GND	A13	A4	A3	E
F	LOOP2	RFGND	RFGND	GND	GND	GND	A14	VCC	VCC	F
G	RFVCCA	RFGND	RFGND	RFGND	RFVCCB	$\overline{CE2}$	CE1	XTLEN	X13	G
H	RFIN	RFGND	RFGND	RFGND	RFGND	PACTL	$\overline{CE0}$	$\overline{OE}$	X13IN	H
J	RFGND	RFGND	RFGND	RFGND	RFOUT	RFVCCD	$\overline{RESET}$	$\overline{WE}$	$\overline{TEST-MODE}$	J
	1	2	3	4	5	6	7	8	9	

Figure 1-6. CY7C6981 Pins Top view

2.0 Functional Overview

- **2.4-GHz Frequency Hopping Spread Spectrum (FHSS) Transceiver –** The CY7C6981's transceiver meets all of the specifications in the Bluetooth™ radio specification, hopping at 1600 times per second.
- **GFSK Modulator/Demodulator –** Bluetooth compliant GFSK modem
- **Closed loop PLL –**VCO is integrated in the CY7C6981
- **AGC & RSSI circuitry –** Advanced AGC circuitry paired with RSSI allows the CY7C6981's radio to operate more efficiently in high noise and high node density environments.
- **Link Control Sequencer –** Decouples Host system by handling demanding low latency protocol requirements.
- **Framer** – Full featured Bluetooth framer which handles all packet format, encryption and hopping sequence.
- **PCM Audio Interface – Allows direct connection to and from audio sources.**
- **Bus Interface for External Microprocessor –** Interface support for most of the microprocessor in the market.

2.1 2.4 GHz Radio transceiver and GFSK modem

The receiver is a Low IF architecture, using RF and baseband AGC, and fully integrated IF filters to achieve high performance in the presence of interference. The FM demodulator and fast data slicer are fully integrated.

The frequency synthesizer provides the frequency hopping local oscillator for transmitter and receiver. It requires a minimum of external chip components: reference crystal and loop filter resistor and capacitors. The RF VCO is fully integrated, requiring no external tank circuits.

The transmitter uses a DSP based vector modulator to convert the transmitted data to an accurate Bluetooth GFSK modulated carrier. The maximum output power supports Class 2 (+4 dBm) operation. Class 1 operation is supported with an external power amplifier. There are a variety of DC power control features for transmitter, synthesizer, and receiver functions to optimize the average current drain.

2.2 Transmit power control and RSSI functions

The Receiver RSSI function reports relative power levels to the baseband chip to support the Bluetooth power control protocol. The transmitter power is controllable digitally over a 34 dB range. The PACTL pin provides the enable for an external Power Amplifier.

2.3 Bluetooth low power operating modes

The CY7C6981 provides support for all of the power modes within the Bluetooth specification.

2.4 Bluetooth Interface Engine

The CY7C6981 has an integrated hardware Bluetooth Interface Engine (BIE) and Sequencer that handles all Bluetooth link controller functionality. Time critical operations such as Data whitening, FEC/HEC, CRC, Encryption are executed in the BIE.

The BIE uses an 8-Kbyte buffer to allow minimum interruption of the host processor running LMP software. This reduces latency requirements, and eliminates the risk of dropping data when the host processor is not available to service the Bluetooth pipe.

The external host microcontroller communicates with the Link Controller inside the CY7C6981 through a set of registers and data buffers. The Link Manager code in the host microcontroller writes to control registers in order to manage the operation of the Link Controller. The Link Controller reports its activity to the Link Manager through status registers. The Link Controller generates interrupts to the host when time critical events need to be serviced.

The Link Manager sends data payloads to the Link Controller by copying the payload contents into an appropriate transmit packet buffer located in the Dual Port RAM. The Link Controller then forms the payload into appropriate Bluetooth packets. The Framer applies the appropriate CRC, encryption, data whitening, and FEC before the packets are transmitted over the air.

When Bluetooth packets are received over the air, the Framer performs decoding, dewhitening, decrypting, and CRC operations before supplying the packets to the Link Controller. The Link Controller then reassembles the appropriate payload buffer into Dual Port RAM, and notifies the Link Manager that a payload was received.

2.5 Memory and Registers Map

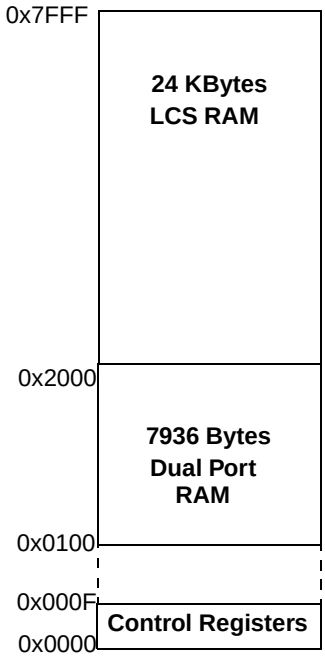


Figure 2-1. CY7C6981 Memory and Registers Map

The Control registers and the 7936 bytes of Dual Port Memory can be addressed by an external microprocessor in two ways:

- In Direct Mode using A[12:0]
- In Indirect Mode loading the address into Indirect Address 0 and 1 registers (0x02,0x03) and the data into the Indirect Data register (0x01).

The 24 Kbytes of LCS RAM can only be addressed in Indirect Mode.

The Indirect Mode could be very useful in systems with limited addressability space, in this case the address lines that are not used must be connected to GND.

2.6 Microprocessor Interface

The general purpose microprocessor interface includes an 8 bit data bus, 2 to 13 bits of address bus (see description above) and 5 control signals: $\overline{CE0}$, CE1, $\overline{CE2}$, $\overline{WE}$, $\overline{OE}$. The global CY7C6981 Chip Enable $\overline{CE}$ is generated internally by NANDing $\overline{CE0}$, CE1, $\overline{CE2}$ (fig. 2-2).

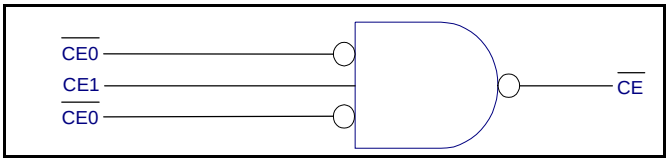


Figure 2-2. CY7C6981 Chip Enable diagram.

The data pins (D0 through D7) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by having Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. The data from Data pins (D0 through D7), is written into the location specified on the address pins (A0 through A12).

Reading from the device is accomplished by setting Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. The data from the memory location specified by the address pins will appear on D0 to D7.

Waveforms and timing of the read and write cycles supported in the CY7C6981 are shown in Fig. 9-1, 9-2, 9-3

2.7 PCM Audio Interface

The CY7C6981 has the capability to deliver digital audio over a PCM (Pulse Code Modulation) bus. This four wire serial interface includes frame sync, serial clock, data transmit, and data receive pins. The PCM Audio Interface operates as a slave; the CY7C6981 appears to the external microprocessor as PCM Audio Codec.

The PCM audio interface integrated in the CY7C6981 has the following characteristics:

Frame Rate: 8 KHz

Slot per frame: 4

Bit Clock rate: 512 Kbps

Bits per slot: 16

Bit order: MSB transferred first

Audio Coding: 13 bit linear zero stuffed

2.8 General Purpose I/O

The CY7C6981 provides 6 General Programmable I/O (GPIO) independently programmable. Each GPIO is accessed and configured through 3 GPIO registers: GPIO Data, GPIO Configuration, GPIO Direction.

Figure 2-3 shows the basic structure of a CY7C6981 GPIO. To configure the GPIO as an output the respective Direction bit is programmed with a 0 to turn on the output buffer. To configure the GPIO as an input the respective Direction bit is programmed with a 1 to turn off the output buffer.

A GPIO pin can be used for alternate function (ex. Capture Timer) through the respectively Configuration bit.

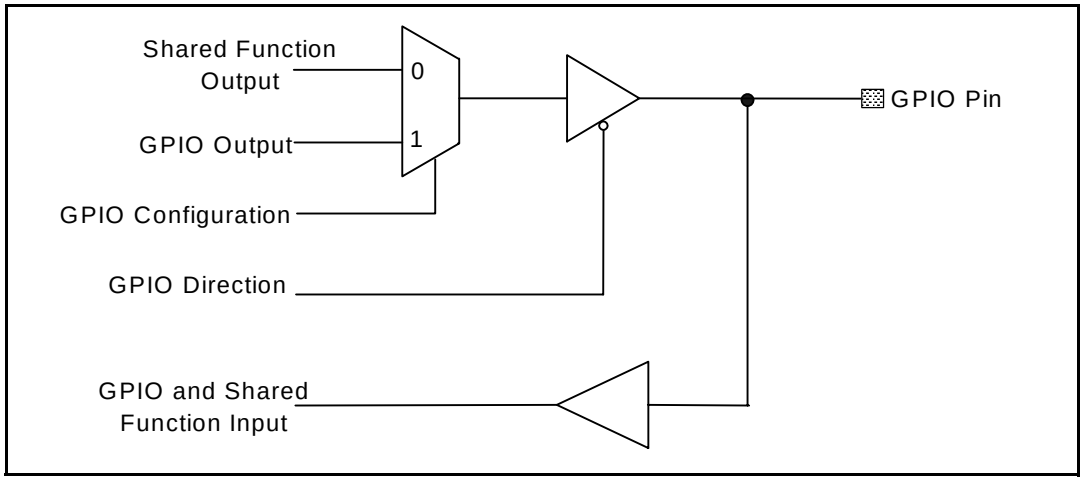


Figure 2-3. GPIO Block Diagram

3.0 Absolute Maximum Ratings

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ....–55°C to +125°C
Supply Voltage on VCC relative to VSS.....–0.5V to +4.6V
DC Input Voltage ..... –0.5V to VCC+0.5V
DC Voltage applied to outputs in High Z State..... –0.5V to VCC+0.5V
Static Discharge voltage (Digital)..... >2001V
Static Discharge voltage (RF) ..... >501V
Latch-up current..... >200 mA

4.0 Operating Conditions

T_A (Ambient Temperature Under Bias).....–40°C to + 85°C
Ground Voltage 0V
F_{OSC} (Oscillator or Crystal Frequency) ..... 13 MHz ± 20 ppm

5.0 DC Characteristics Over the Operating Range

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		2.7		3.6	V
I_{CC}	Operating Supply Current				70	mA
I_{SB}	Low Power Mode Current			10		µA
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5V	V
V_{IL}	Input Low Voltage		–0.5		0.8	V
I_I	Input Leakage Current	$0< V_{IN} < V_{CC}$	–1		+1	µA
V_{OH1}	Output Voltage High	I_{OH} = –100 µA	V_{CC}–0.2			V
V_{OH2}	Output Voltage High	I_{OH} = –1.6 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}= 1.6 mA			0.4	V
I_{OZ}	Output Leakage Current	$0<=V_O<=V_{CC}$ Output Disabled	–1		+1	µA
C_{PIN}	Pin Capacitance				8	pF

6.0 Radio Specification

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
	RF Frequency Range		2.402		2.480	GHz
Radio Receiver (T=25°C, V_{CC}= 3.3V)						
	Sensitivity	BER=10^{-3}		–82		dBm
	Maximum Received Signal			–20		dBm
	Interference Performance	BER<10^{-3}				
	Co-channel Interference rejection C/I	C = –60 dBm			11	dB
	Adjacent (1 MHz) channel selectivity C/I 1 MHz	C = –60 dBm			0	dB
	Adjacent (2 MHz) channel selectivity C/I 2 MHz	C = –60 dBm			–30	dB
	Adjacent (≥ 3 MHz) channel selectivity C/I ≥ 3 MHz	C = –67 dBm			–40	dB

	Image Frequency Interference, C/I Image	C = –67 dBm			- 9	dB
	Adjacent (1 MHz) interference to in-band image frequency, C/I image ± 1 MHz	C = –67 dBm			- 20	dB
	Out-of-Band Blocking Interference Signal Frequency	BER<10^{-3}				
	30 MHz – 2000 MHz	C = –67 dBm	– 10			dBm
	2000 MHz – 2399 MHz	C = –67 dBm	– 27			dBm
	2498 MHz – 3000 MHz	C = –67 dBm	– 27			dBm
	3000 MHz – 12.75 GHz	C = –67 dBm	– 10			dBm
	Intermodulation	C = –64 dBm Df = 5, 10 MHz	–39			dBm
	Spurious Emission					
	30 MHz – 1GHz				–57	dBm
	1 GHz – 12.75 GHz				–47	dBm
Radio Transmitter (T=25°C, V_{CC}= 3.3V)						
	Maximum RF Transmit power	Pwr setting = Max.	–6	0	+4	dBm
	RF power stability over operating temperature range			TBD		dB
	RF power control range			34		dB
	RF power range control step size	8 steps		6		dB
	Modulation accuracy				1	%
	Frequency Drift - One-slot packet		–25	0	25	KHz
	Frequency Drift - Three-slot packet		–40	0	40	KHz
	Frequency Drift - Five-slot packet		–40	0	40	KHz
	Maximum Frequency Drift Rate			0	400	Hz/ ms
	In-band Spurious					
	Adjacent Channel Power (± 500 KHz)				– 20	dBc
	Second Channel Power				– 20	dBm
	≥ Third Channel Power				– 40	dBm
	Out-of-band Spurious Operation Mode					
	30 MHz – 1 GHz				–36	dBm
	1 GHz – 12.75 GHz				–30	dBm
	1.8 GHz – 1.9 GHz				–47	dBm
	5.15 GHz – 5.3 GHz				–47	dBm
	Out-of-band Spurious Idle Mode					
	30 MHz – 1 GHz				–57	dBm
	1 GHz – 12.75 GHz				–47	dBm
	1.8 GHz – 1.9 GHz				–47	dBm
	5.15 GHz – 5.3 GHz				–47	dBm

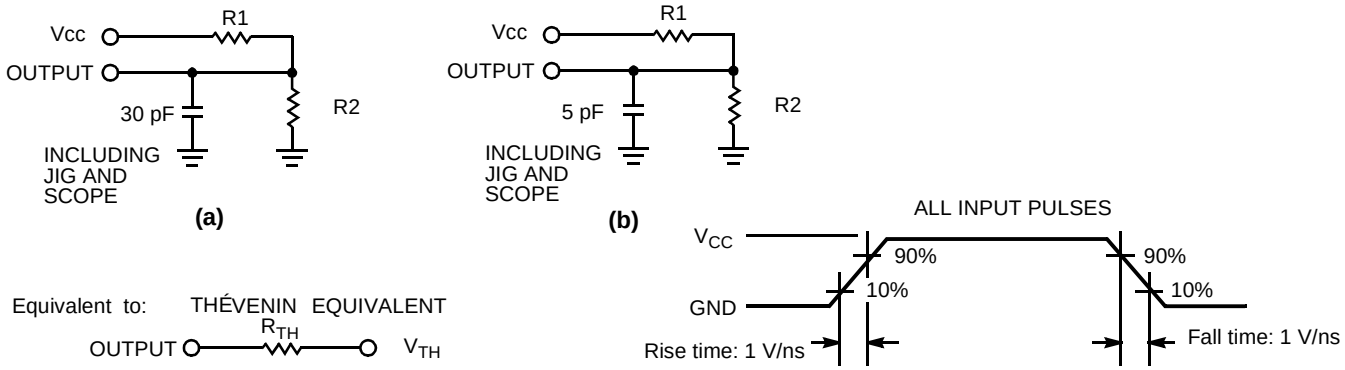
7.0 Switching Characteristics. Over the Operating Range [1]

Microprocessor Interface - READ CYCLE			Min.	Max.	Unit
t_{RC}	Read Cycle Time		70		ns
t_{ACE}	$\overline{CE}$[2] LOW to Data Valid			70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid			35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[3]		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [4]			25	ns
t_{LZCE}	$\overline{CE}$[2] LOW to Low Z[3]		10		ns
t_{HZCE}	$\overline{CE}$[2] HIGH to High Z[3, 4]			25	ns
Microprocessor Interface WRITE CYCLE[5, 6]					
t_{WC}	Write Cycle Time		70		ns
t_{AW}	Address Set-Up to Write End		60		ns
t_{HA}	Address Hold from Write End		0		ns
t_{SA}	Address Set-Up to Write Start		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		50		ns
t_{SD}	Data Set-Up to Write End		30		ns
t_{HD}	Data Hold from Write End		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3, 4]			25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[3]		10		ns

Notes:

1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance
2. The global CY7C6981 Chip Enable ($\overline{CE}$)is generated internally by NANDing $\overline{CE0}$,CE1,$\overline{CE2}$.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
4. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. The minimum write cycle time for write cycle ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

8.0 AC Test Loads and Waveforms



Parameter		Unit
R1	1340	Ω
R2	1172	Ω
R_{TH}	625	Ω
V_{TH}	1.4	V
V_{CC}	3.00	V

9.0 Switching Waveforms

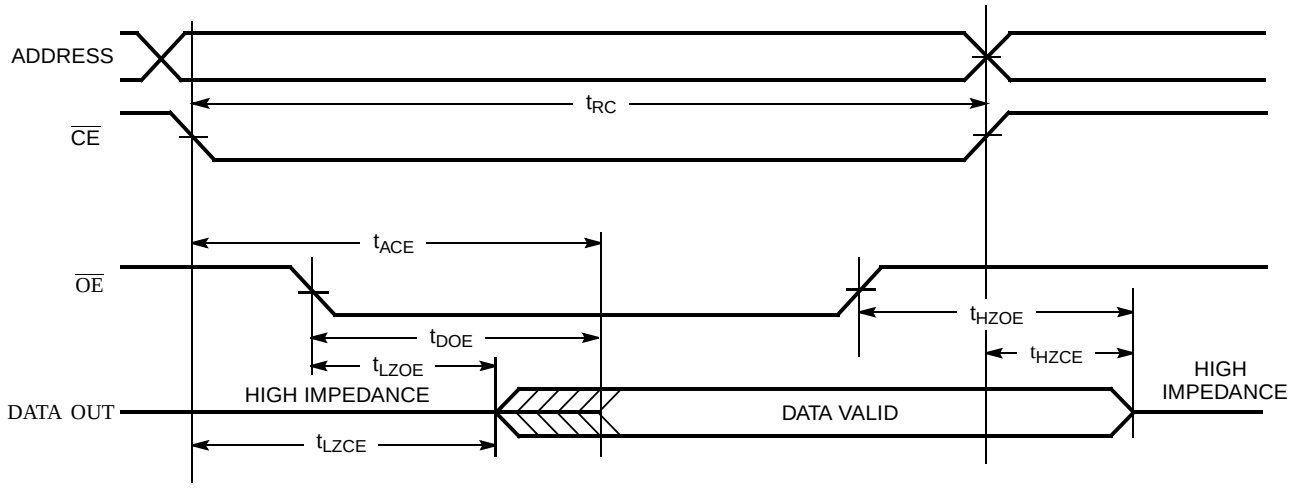


Figure 9-1. Read Cycle ($\overline{OE}$ Controlled)[7,8]

Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

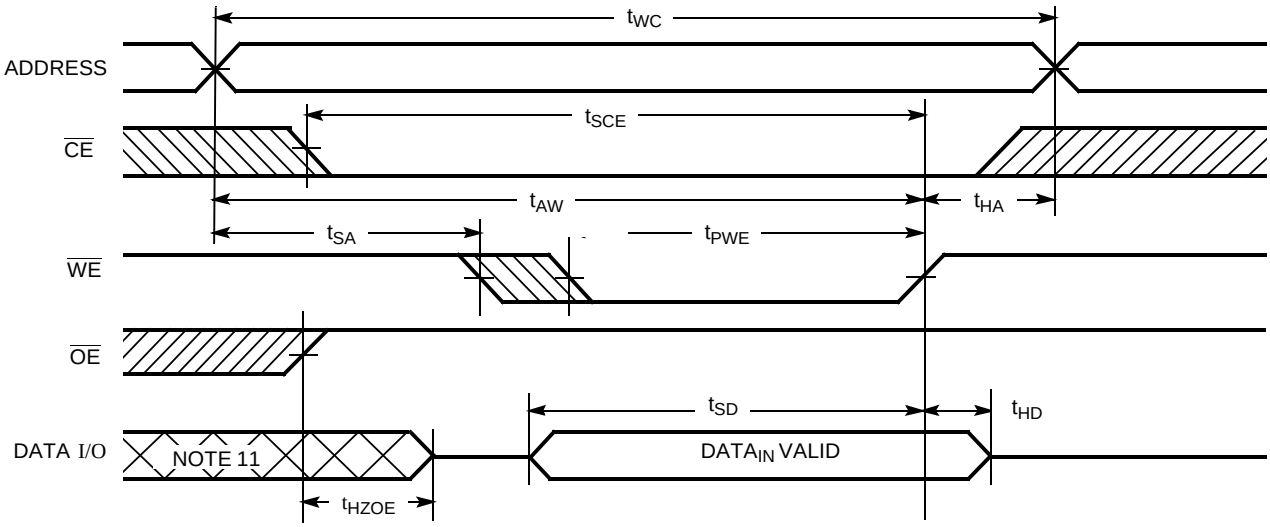


Figure 9-2. Write Cycle ($\overline{WE}$ Controlled)[5,9,10]

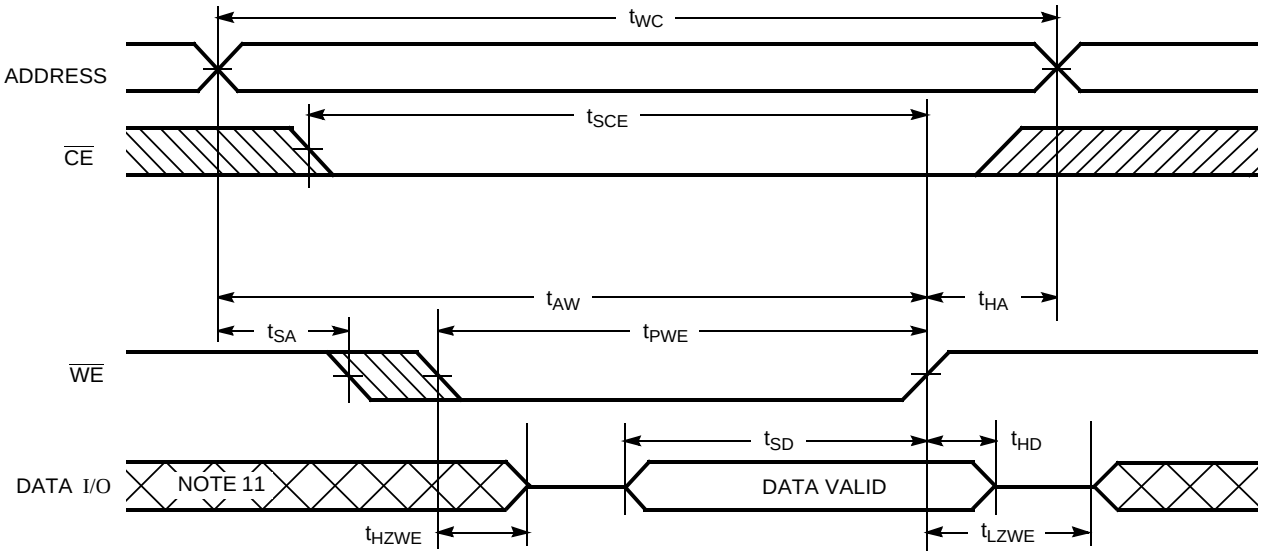


Figure 9-3. Write Cycle ($\overline{WE}$ Controlled, $\overline{OE}$ Low)[6,10]

Notes:
9. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
10. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
11. During this period the I/Os are in the output state and input signals should not be applied.

10.0 Ordering Information

Part Number	Package name	Package Type	Operating Range
CY7C6981-BAI	BA81A	81-Ball Thin Ball Grid Array (10 x 10 x 1.2 mm)	Industrial

11.0 Package Diagrams

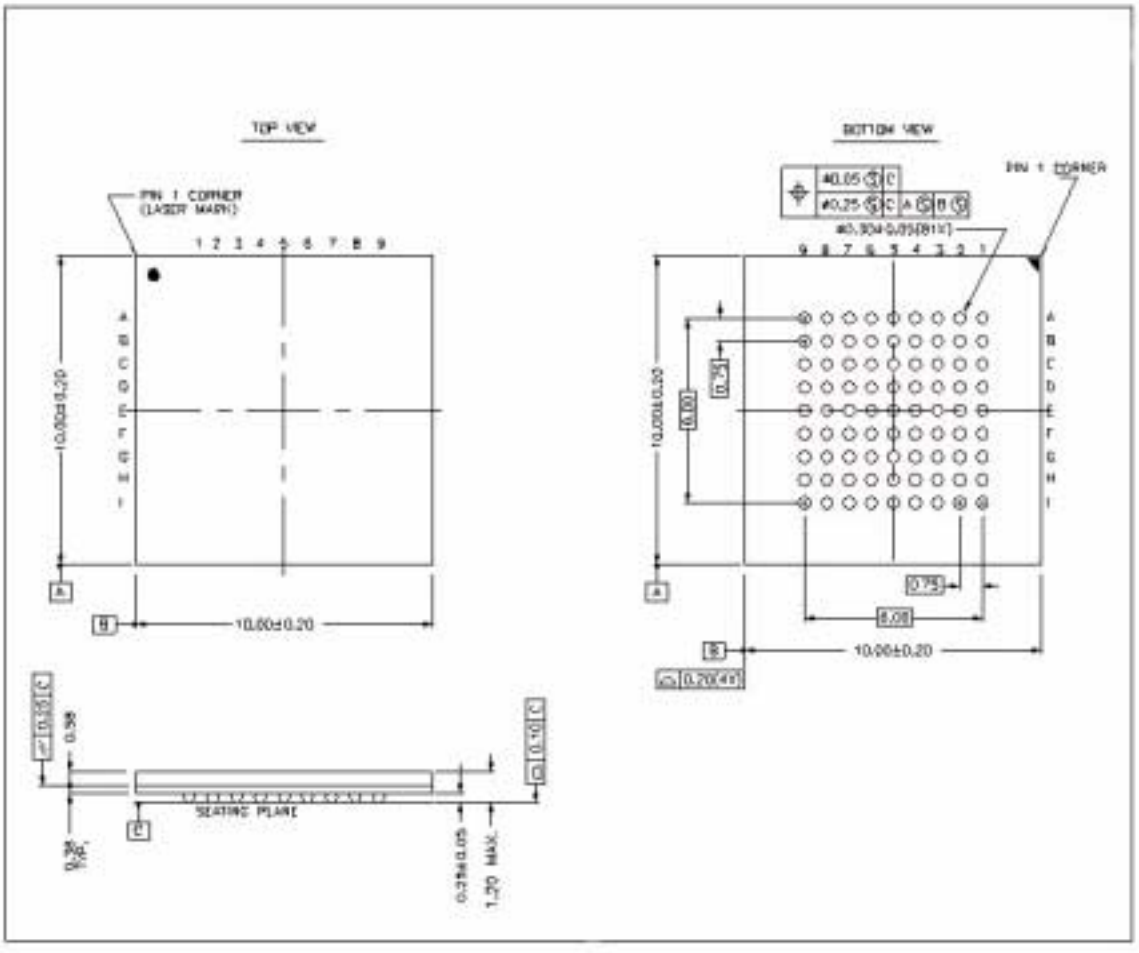


Figure 11-1. CY7C6981 Package Diagram

Bluetooth is a trademark owned by Telefonaktiebolaget L M Ericsson, Sweden and licensed to Cypress Semiconductor.

Document Title: CY7C6981 Bluetooth™ Link Controller and Radio Document Number: 38-11002				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106128	04/03/01	LXA	New Data Sheet