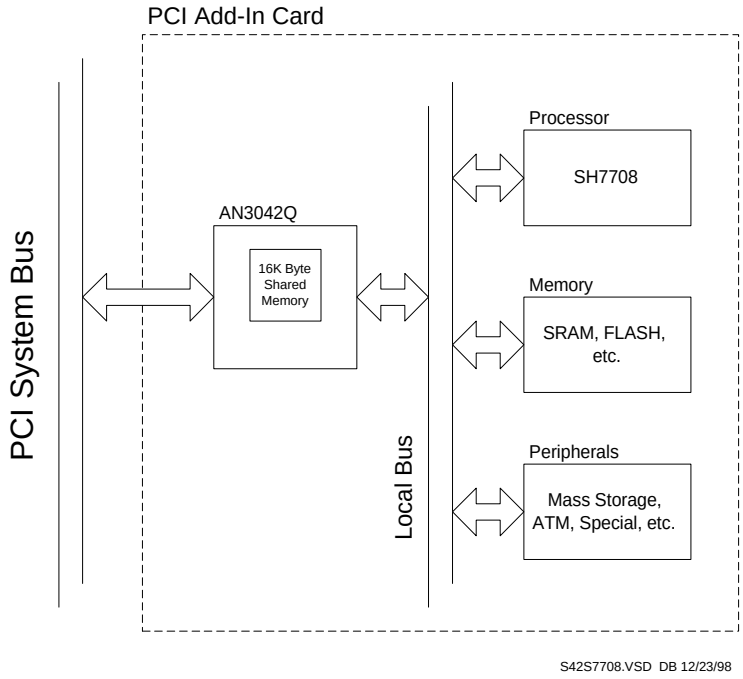
Overview

The AN3042Q interfaces directly to the Hitachi SH7708 SH3 processor. The interface described in this application note connects an AN3042Q to a 32-bit SH7708 running at 50 MHz with a 25 MHz bus speed.

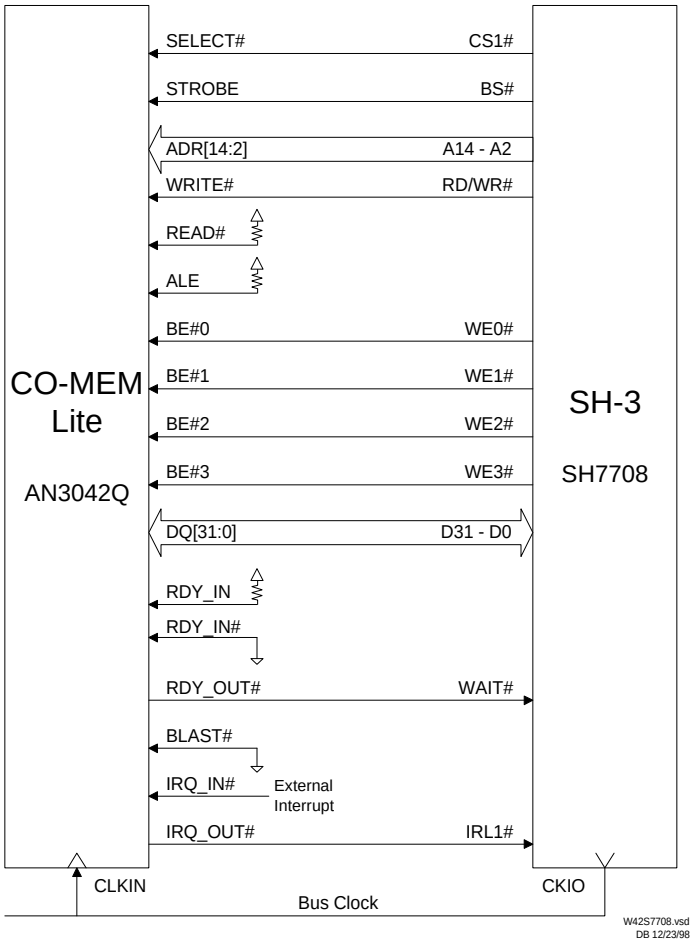
System Block Diagram

The AN3042Q connects the SH7708 to the PCI system bus.



Wiring Diagram

Wiring the AN3042Q to the SH7708 is simple. The interrupt connections in the diagram are not required for the bus interface; they are included for illustrative purposes. SH7708 memory area 1 is used here as seen by the use of CS1#. Any of the 7 memory areas of the SH7708 may be used. In SH7708 terms, the AN3042Q should be treated as a "normal memory." For purposes of this application note, the SH7708 is operating in little endian mode.



AN3042Q Configuration Programming

The AN3042Q Local Bus Configuration register must be programmed to support the SH7708 external bus architecture. The configuration register may be loaded either at power-up from a PROM via the AN3042Q's I2C interface or from the PCI bus system host. The value for the register is:

LBUSCFG = 0x0E11

Timing

This section includes timing diagrams for the processor bus interface between the SH7708 and the AN3042Q. The interface is based on a 25 MHz CKIO signal from the SH7708 component. By using PLL circuits, clock multipliers, and clock dividers which are part of the SH7708, several SH7708 internal clocking combinations are possible. For instance, the internal circuits of the SH7708 may be set to run at 50 MHz while the external bus clock runs at 25 MHz.

This application note illustrates use of the SH7708's capability to generate the clock to the AN3042Q local bus interface. The reference clock for all SH7708 external bus timing is CKIO. CKIO is directly connected to the AN3042Q CLKIN input signal in this application note. This note is applicable to the SH7708 clocking modes 0, 1, and 2. CKIO is part of the SH7708's Clock Pulse Generator, (CPG). There are several conditions that must be considered when setting up the CPG. Design details may be found in Section 9 of the SH7708 Series Hardware Manual.

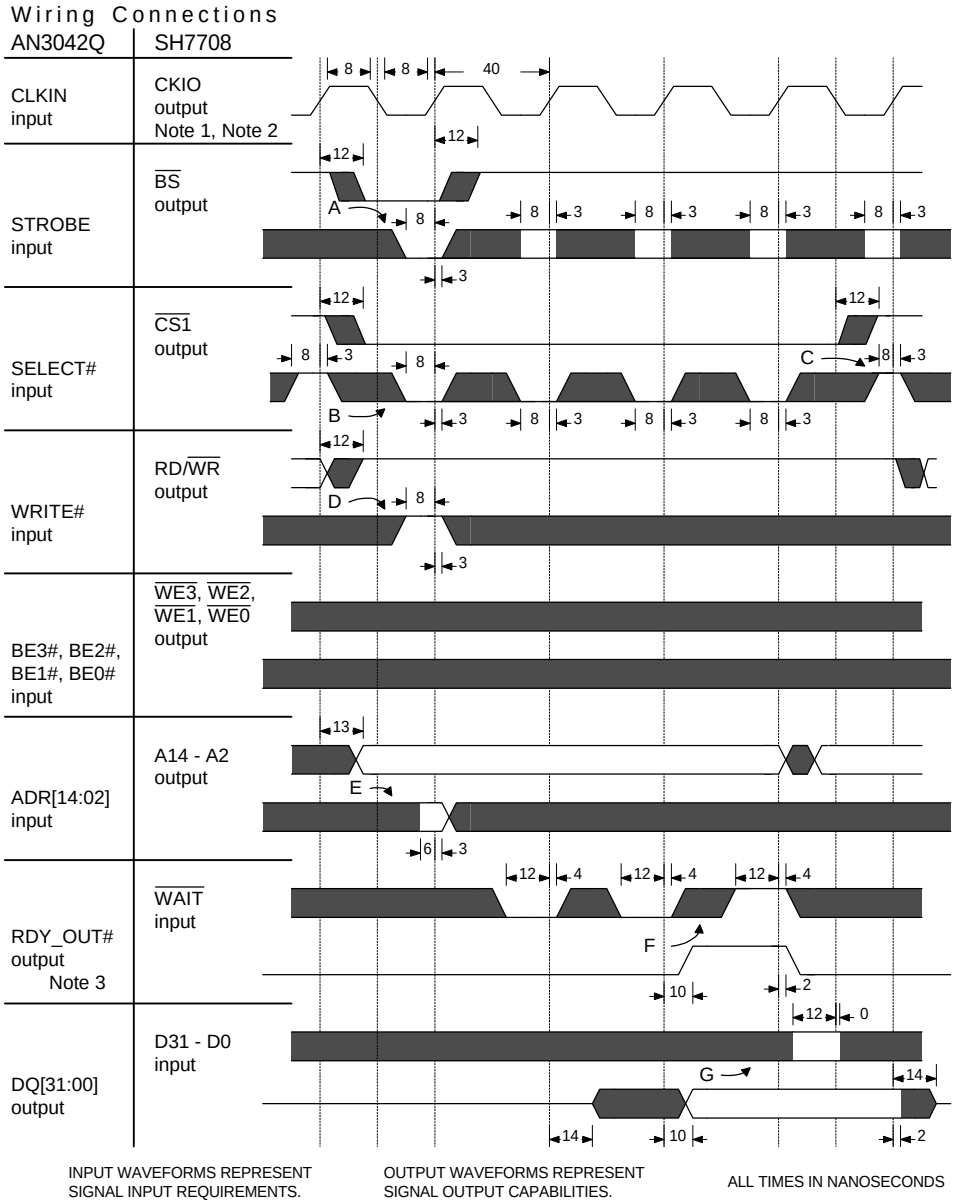
Characteristics of CKIO as generated by the SH7708 may not be desirable in some implementations. For instance, the clock is shutdown during SH7708 Standby mode and when it restarts it will violate AN3042Q clocking requirements. However, the SH7708 Sleep mode does not shutdown the CKIO clock. Also, the AN3042Q Operation Registers and I2C port are unavailable when the CLKIN signal is not toggling. One way to avoid this is not to allow the SH7708 to switch to the Standby mode or to provide an external bus clock from other circuitry. Another reason for external bus clock generation circuitry is that larger systems may require clock buffering and the use of a low skew clock buffer would be indicated. SH7708 clock mode 7 is used to define CKIO as an input to the SH7708. The internal PLL is still used and clock multiplication is available for SH7708 internal circuits.

The timing diagrams show waveforms organized in pairs. One member of the pair is the signal name of the AN3042Q and the other member is signal name of the SH7708. As shown in the Wiring Diagram, these signals are directly wired together. The intention of the timing diagrams is to show that the two components have compatible timing. The waveforms for the output signals illustrate the signals' output characteristics and the waveforms for the input signals illustrate the signals' input requirements. In this manner, both component specifications can be viewed together. Immediately after the read and write access timing diagrams, a summary of timing margin for each signal pair is provided.

Explanation and key to reading the timing diagrams --

- Timing data are taken from the SH7708 and AN3042Q specifications; see References.
- Timing numbers are in nanoseconds and worst case commercial environment.
- Clock pulse widths and clock cycle time are minimum values.
- Where relevant, maximum data valid output timing is shown to support setup calculations.
- Output waveform timing represents signal output characteristics and capabilities.
- Where relevant, minimum data input setup timing is shown to support setup calculations.
- Input waveform timing represents signal input requirements.

The following is the timing diagram for SH7708 read access to the AN3042Q.



NOTES --

1 CKIO is generated using SH7708 clock modes 0, 1, or 2 in this diagram. Other clocking options are available with the SH7708; e.g., CKIO generated externally and input to both the AN3042Q and the SH7708. Care is needed when using the SH7708 generated CKIO as the AN3042Q clock input. See text in the Timing section of this application note for more detail.

2 The AN3042Q CLKIN input requires a minimum 8 nsec high/low pulse width and the SH7708 CKIO output provides a minimum 8 nsec high/low pulse width when CKIO is operating at or below 30 MHz. CKIO rise and fall times are 6 nsec maximum. For larger systems, CKIO may be generated from a different source (e.g. a low skew clock buffer) to provided a better clock margins.

3 Wait states occur when the AN3042Q asserts RDY_OUT# to low. The minimum of one additional wait state is illustrated here.

LETTERS A through G are references for the timing margin summary list. See text in Timing section.

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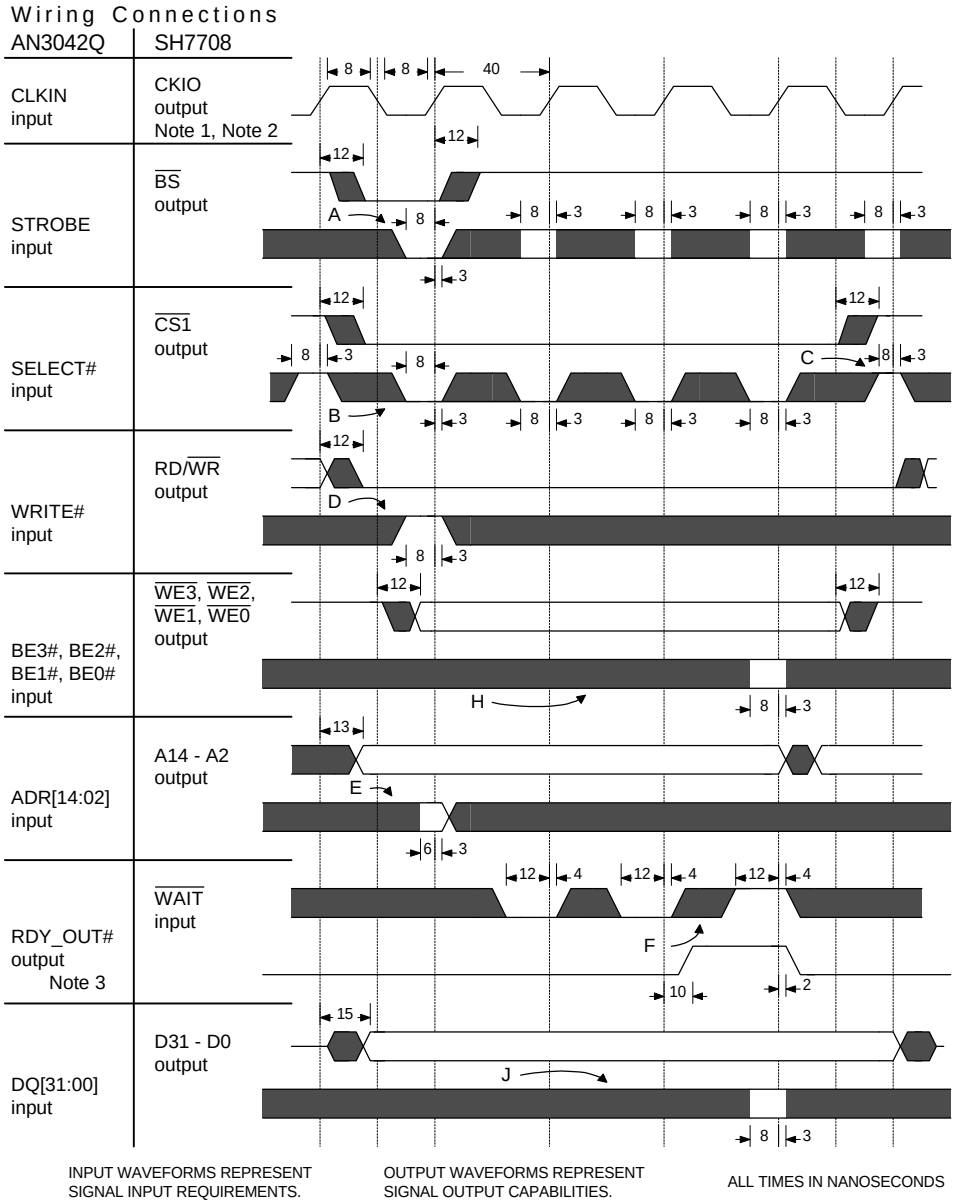
The following is the timing diagram for SH7708 write access to the AN3042Q.



NOTES --

1 CKIO is generated using SH7708 clock modes 0, 1, or 2 in this diagram. Other clocking options are available with the SH7708; e.g., CKIO generated externally and input to both the AN3042Q and the SH7708. Care is needed when using the SH7708 generated CKIO as the AN3042Q clock input. See text in the Timing section of this application note for more detail.

2 The AN3042Q CLKIN input requires a minimum 8 nsec high/low pulse width and the SH7708 CKIO output provides a minimum 8 nsec high/low pulse width when CKIO is operating at or below 30 MHz. CKIO rise and fall times are 6 nsec maximum. For larger systems, CKIO may be generated from a different source (e.g. a low skew clock buffer) to provided a better clock margins.

3 Wait states occur when the AN3042Q asserts RDY_OUT# to low. The minimum of one additional wait state is illustrated here.

LETTERS A through F, H and J are references for the timing margin summary list. See text in Timing section.

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From the two diagrams, timing margin for a SH7708 to AN3042 bus interconnect can be extracted. The timing shown is worst case commercial environment. Loading beyond the specification, signal line lengths, and other environmental constraints beyond commercial worst case can use this margin and maintain a compatible interface. Identifying letters are shown on the two timing diagrams.

Read and Write Access to the AN3042

A	AN3042 STROBE input setup	20	nsec
B	AN3042 SELECT# input setup at access start	20	nsec
C	AN3042 SELECT# input setup at access end	0	nsec
D	AN3042 WRITE# input setup	20	nsec
E	AN3042 ADR[14:02] input setup	21	nsec
F	SH7708 WAIT# input setup	8	nsec

Data Bus for Read Access to the AN3042

G	SH7708 D31-D0 input setup	38	nsec	(output stable across cycles)

Data Bus and Write Enables for Write Access to the AN3042

H	AN3042 BE#[3:0] input setup	120	nsec	(output stable across cycles)
J	AN3042 DQ[31:00] input setup	137	nsec	(output stable across cycles)

Performance

Throughput between the SH7708 and the shared memory of the AN3042Q is 20 MB/s. Access to the AN3042Q Operation Registers or FIFO may incur wait states during concurrent accesses by the PCI bus. One wait state equates to one external bus clock cycle.

AN3042Q mastered DMA bursting from the AN3042Q shared memory to system host memory has been measured to be approximately 120MB/s on an unloaded PCI bus. Anchor Chips Incorporated has application notes concerning DMA operation and PCI bursting that can provide more insight into AN3042Q performance for particular environments.

References

Specifications used by this application note are listed below.

CO-MEM Lite, AN3042Q Integrated Circuit Technical Reference Manual, Version 1.1, October 1998, Anchor Chips Incorporated.

SH7708 Series Hardware Manual, Revision 5.0, April 1998, PMH13TH003D4, Hitachi Semiconductor.

Additional component literature may be downloaded from web sites at Anchor Chips Incorporated and Hitachi Semiconductor. The two main sites are listed below.

Anchor Chips PCI Developer's Home	http://www.anchorchips.com/pcidev/
Hitachi Semiconductor	http://semiconductor.hitachi.com/

The PCI 2.1 specification may be purchased from the PCI Special Interest Group (SIG) or other sources. The web site for the PCI SIG is:

PCI SIG Home Page	http://www.pcisig.com/

Some related Anchor Chips Incorporated application notes are listed below. These documents may be downloaded from the Anchor Chips PCI Developer's Home.

How to doDMA
PCI Bus Mastering for System Performance