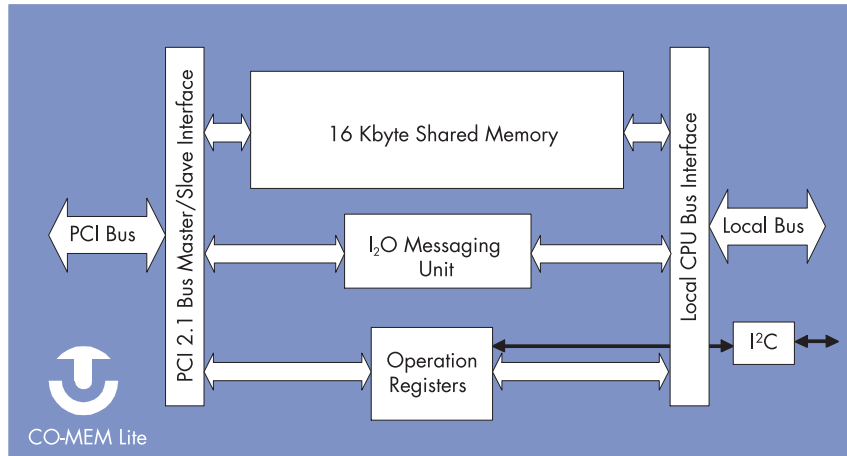


## AN3042QC



The CO-MEM Lite chip provides a simple way to interface a microprocessor to the PCI bus. The chip's internal 16-Kbyte RAM is used as a shared memory buffer between the local microprocessor and the PCI bus. An I<sub>2</sub>O messaging unit facilitates communications between the host and local software.

The CO-MEM Lite chip's dual-port memory appears in both the local microprocessor and PCI address spaces, and can simultaneously be accessed from both sides. In addition, the chip can become a PCI bus master to move any data block up to 16 Kbytes using the full-burst capabilities of the PCI bus.

The CO-MEM Lite chip provides a direct access mechanism from the local bus to the PCI bus. With it, the local processor can direct the chip to run a PCI bus master cycle of any kind to any address. This means that the CO-MEM Lite chip can be used as a host bridge and can run PCI configuration cycles. It also provides a convenient mechanism for the local processor to retrieve and post I<sub>2</sub>O message buffers to other I<sub>2</sub>O agents.

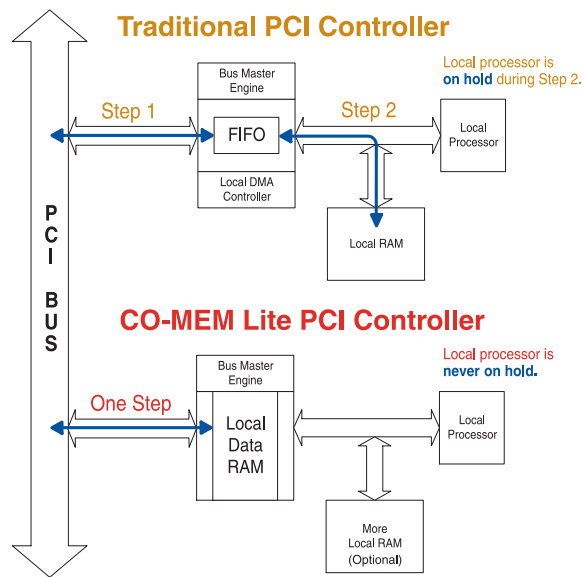
Using the CO-MEM Lite chip on a board is simple and efficient. The combination of a fully-compliant PCI interface, on-chip memory, and a configurable microprocessor interface means that few external components are necessary for complete peripheral implementation. The CO-MEM Lite chip's PCI interface supports both master and slave modes, along with 3V or 5V signaling. A 3.3V power supply and streamlined TQFP package complete the picture making the CO-MEM Lite chip the ideal PCI peripheral controller chip for today's designs.

## Features

- PCI 2.1 bus master/slave interface
- Configurable interface to allow direct connect to many microprocessors
- Data bus widths of 8, 16, or 32 bits
- Interrupt generation to both host and local systems
- Embedded host-bridge capability
- 16 Kbytes of shared memory for long burst cycles on the PCI bus
- Supports PCI 3V and 5V signaling requirements
- Looks like RAM to the local processor
- I<sub>2</sub>O message unit
- Local interface clock speeds up to 50 MHz
- 3.3V power supply
- 160 TQFP package

# Speed and Flexibility Make PCI Interface Simple

The CO-MEM Lite Chip allows the designer to interface an application to the PCI bus in a straightforward, inexpensive way. High efficiency, low cost, and flexibility make the CO-MEM Lite chip the price-performance leader in PCI solutions.



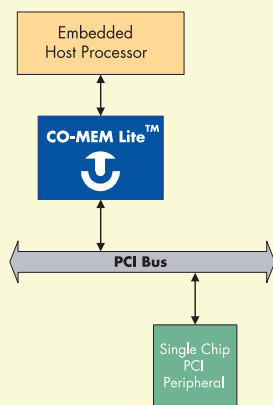
## Faster Communication

The traditional PCI controller uses a FIFO for storage when moving data across the PCI bus as a bus master. This means that transferring between the PCI bus and the local processor's memory is a two-step process—the FIFO has to be loaded and unloaded. During this process, the local processor is on hold while data is moved to or from local memory. To maintain maximum PCI bus efficiency, the process must be carefully coordinated to avoid FIFO-full and FIFO-empty conditions.

The CO-MEM Lite PCI controller uses its internal shared memory as the storage element for PCI bus master transfers. This allows PCI bus master transfers to be done in just one step. Up to 16 Kbytes can be moved to or from the PCI bus without local processor intervention. The local processor has immediate access to the data since the shared memory is already part of the local processor's memory map. Maximum PCI bus efficiency is guaranteed as there are no FIFO-full or empty conditions to deal with. CO-MEM Lite makes for faster, more efficient bus master transfers.

## Embedded Host Bridge

Many of today's single-chip peripherals are available only with a PCI interface. To hook these cost-effective solutions up to an embedded processor requires a PCI bus. The plug-and-play nature of PCI means that the bus must be run by a PCI host bridge. The CO-MEM Lite chip's direct access mode allows the processor to run PCI configuration cycles. CO-MEM Lite functions as the PCI host bridge in the embedded processor application. The local processor can use direct access mode to configure all of the PCI peripherals in the embedded system. The shared memory of the CO-MEM Lite chip can be used as target memory for those PCI peripherals with bus master capabilities. The CO-MEM Lite chip makes embedded PCI a cost-effective option for many new system designs.



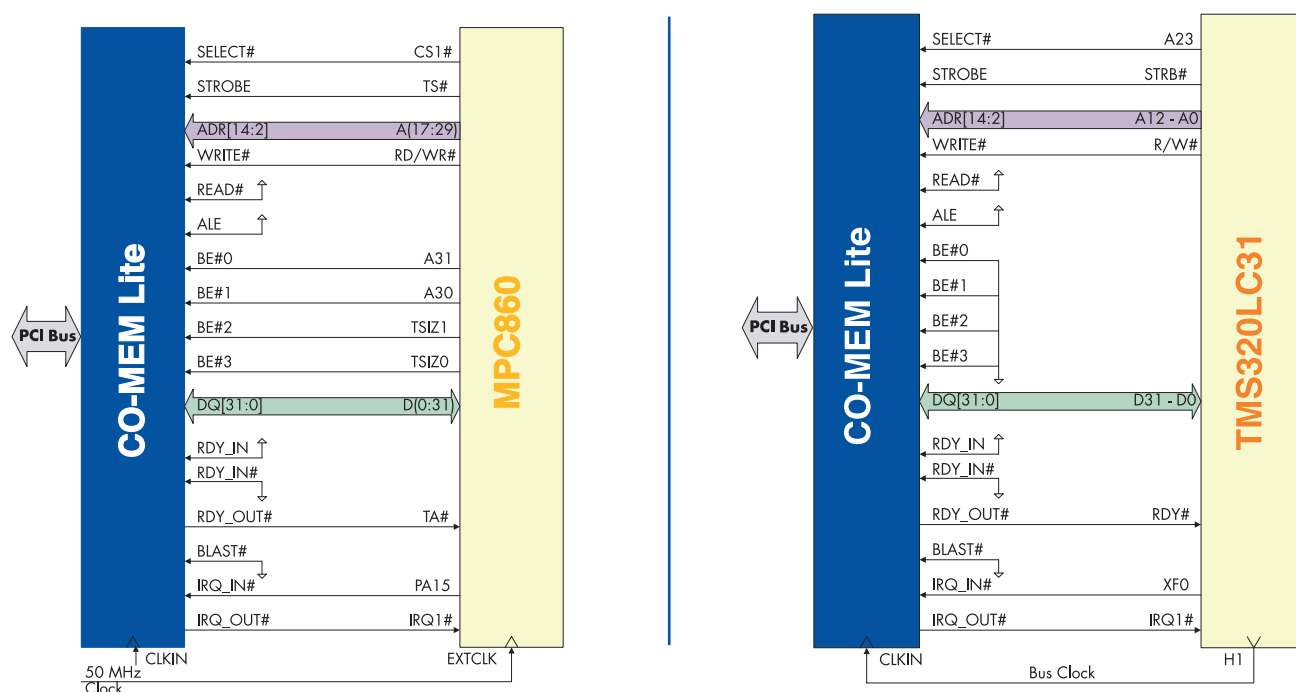
## Highly Configurable

The CO-MEM Lite local bus interface is highly configurable, making it easy to interface to any 8-, 16-, or 32-bit microprocessor. In fact, in most cases no “glue” logic is necessary at all. The CO-MEM Lite local bus interface has options that allow it to support different polarities of most control signals, as well as various definitions of the read, write, address strobe, burst last, and ready signals.

Support for both Motorola and Intel-style zero wait-state bursting is built into the CO-MEM Lite local bus interface. The configuration word that controls these parameters is loaded from an external I<sup>2</sup>C, non-volatile memory. The AN3042 Technical Reference Manual provides the detailed information necessary to configure the CO-MEM Lite local bus interface properly. The table that is included here shows a partial list of configuration word values.

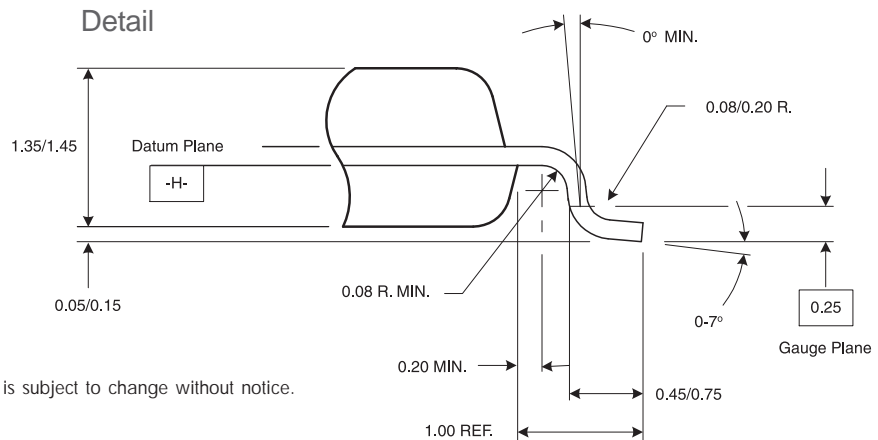
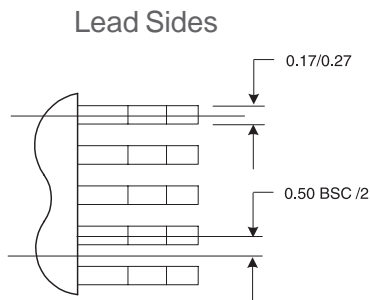
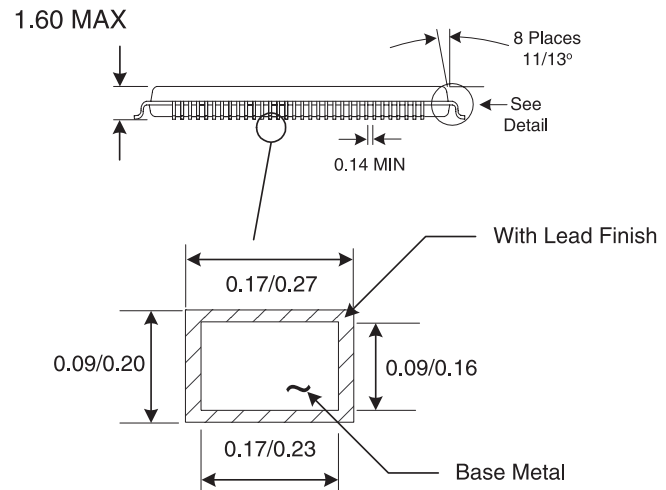
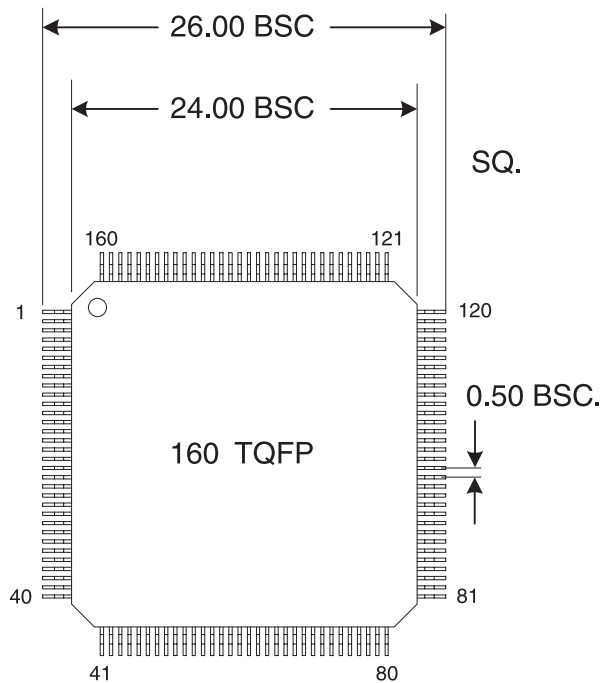
Microprocessors with multiplexed and separate address and data lines are supported by the CO-MEM Lite local bus interface, as are external clock frequencies of up to 50 MHz.

Processor	Configuration Word
Motorola 68040	0x0B50
Motorola Power QUICC MPC860	0x0B50
Motorola QUICC 68360	0x8B18
Intel i960	0x0A00
Intel i486	0x6A00
Intel 80186	0x2D21
Texas Instruments TMS320LC31	0x0A90



CO-MEM Lite can be configured to connect to any microprocessor. Here are two examples. Note that **no glue logic** is necessary.

# Package



All linear dimensions are in millimeters. This drawing is subject to change without notice.

For more information about the CO-MEM Lite PCI controller, visit [www.anchorchips.com](http://www.anchorchips.com).



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