CO-MEM Lite

AN3042 Integrated Circuit

Technical Reference Manual

Version 1.2

Preliminary – Information Subject to Change

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The AN3042 Technical Reference Manual, version 1.2

Document :

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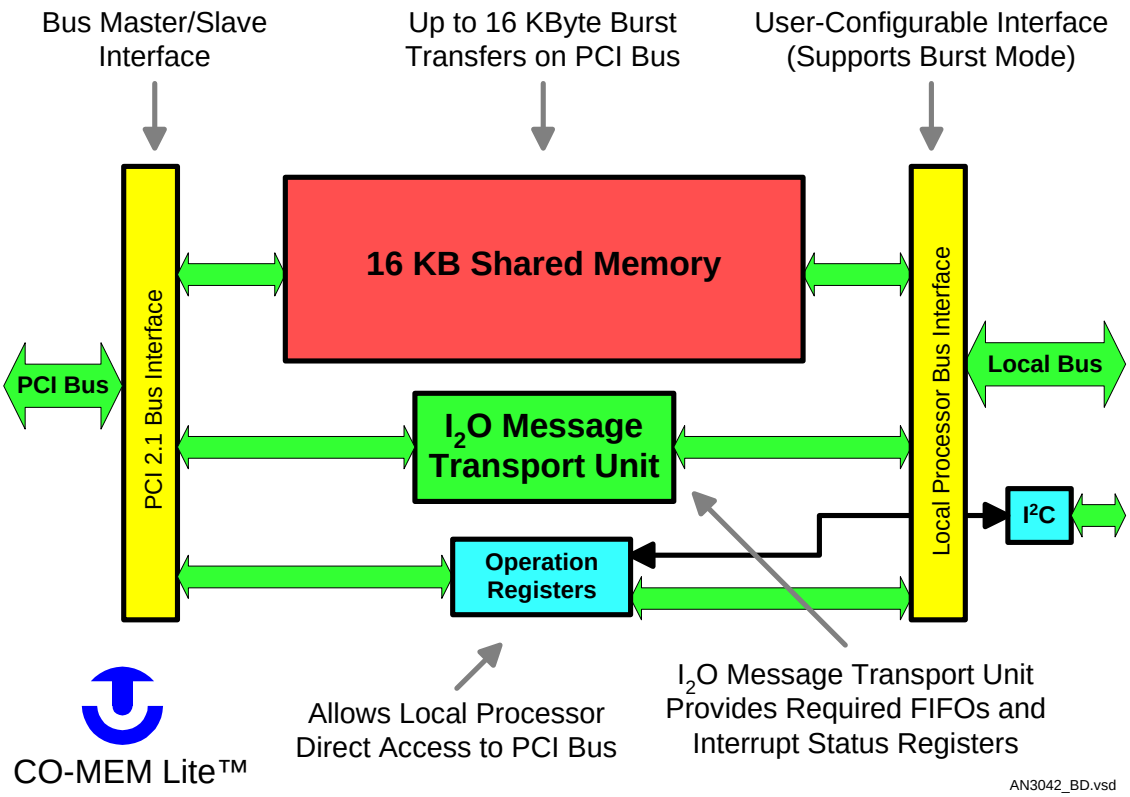
OVERVIEW



Introduction

The AN3042 is one of the PCI interface controllers in the Anchor Chips CO-MEM family. The AN3042 provides a PCI master/target interface with direct connects to many popular microprocessors. It provides 16K bytes of internal SRAM that is used as shared memory between the local microprocessor and the PCI bus. An I_2O message unit, complete with message queues and interrupt capability, is also provided. The AN3042 allows the designer to interface an application to the PCI bus in a straightforward, inexpensive way.

Features:

- 16K Bytes of shared memory
- Master and Target PCI V2.1 compliant interface
- Embedded host bridge capability
- Direct interface to many microprocessors
- I_2O message transport unit
- Local bus clock rates up to 50 MHz
- 3.3 Volt Power Supply including compatibility with 5 Volt PCI Bus signaling
- 160 pin thin plastic quad flat package

Functional Description

The AN3042 is composed of a number of shared resources that allow effective data movement between the local bus and the PCI bus.

A primary resource within the AN3042 is its 16K bytes of dual port memory. This memory is interfaced to both the PCI bus and to a local microprocessor bus. This shared memory can be accessed as a target from both buses at the same time for inter-process communication. From either the local or PCI bus the AN3042 can be directed to become a PCI bus master to move data into or out of the internal shared memory as a direct memory access (DMA). The AN3042 can DMA across the PCI bus any size data block, up to 16K bytes. It uses the full bursting capabilities of the PCI bus for maximum efficiency and can transfer data over the full 32-bit PCI address space. The AN3042 implements optional requirements of the PCI specification by selecting the optimum PCI command for each transaction in order to maximize overall efficiency of the system platform.

The AN3042 provides a direct access mechanism from the local bus to the PCI bus. With it, the local processor can direct the AN3042 to run a PCI bus master cycle of any kind to any address. This means that the AN3042 can run PCI configuration cycles allowing it to be used as a host bridge.

Four First-In First-Out (FIFO) storage elements provide another resource to the user. These are for general purpose usage and are accessible from either the PCI bus or the Local bus. When the I_2O messaging unit functionality of the AN3042 is to be used, the four FIFO become part of the I_2O messaging unit of the AN3042. The I_2O messaging unit consists of the four FIFO and the I_2O system interrupt registers. The shared memory of the AN3042 is used to store I_2O message frame buffers while most of shared memory is still available for general purpose use. Efficient I_2O messaging is realized by using the direct access mechanism for the local processor to retrieve and post I_2O message pointers to other I_2O agents. And, data transfer of the message buffers is made very efficient using the AN3042 PCI bus mastering controller to burst the message frames to other I_2O agents.

Mailbox registers are specially synchronized so that they can be accessed from both the PCI side and the local side simultaneously without data corruption. By writing to the mailbox registers, a method is available for the local processor to cause an interrupt to the host and vice versa. This is enabled by the interrupt mask located in the AN3042 Operations Registers. These mailboxes are useful for implementing a software-controlled access protocol to the shared memory, (for instance, semaphores).

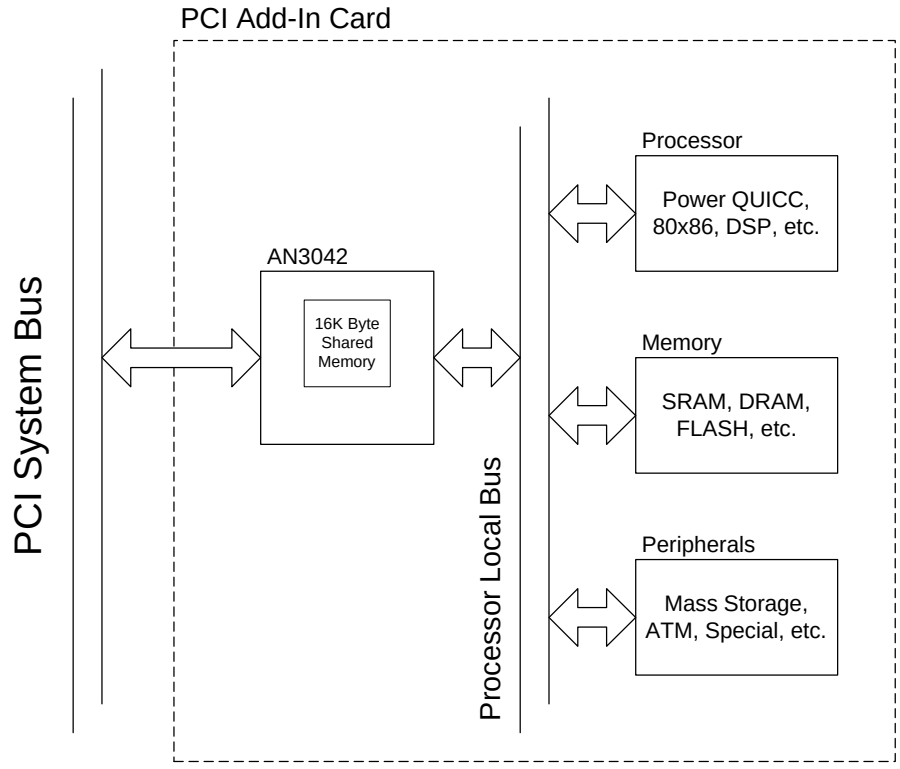
The AN3042 includes an interrupt controller. There are separate interrupt mask and command/status registers for the PCI bus and the Local bus. The interrupt sources are DMA completion, mailbox, FIFO not empty (also for I_2O), FIFO overflow, PCI master abort, PCI target abort, and there is an external interrupt input pin.

An I^2C serial interface is provided to allow the use of a serial EEPROM for non-volatile storage of AN3042 initialization parameters including PCI configuration information and local bus settings. The AN3042 will

optionally access the EEPROM after reset and download the initialization information before responding to PCI or local bus transactions. The I^2C serial interface can be used after power-up to provide access to other I^2C serial peripherals. This gives a simple way to connect the wide variety of available I^2C serial components to the local or host processor.

The AN3042 local bus is a flexible, configurable interface that is designed to readily connect to many industry standard microprocessors.

The following block diagram illustrates a generic application for the AN3042.



Pin Description

The Pin Type for AN3042 is defined as follows:

in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
t/s	Tri-State is a bi-directional, tri-state input/output pin.
s/t/s	Sustained Tri-State is an active low tri-state signal driven by only one bus agent at a time. When ownership is passed to another agent, the signal is driven high for one clock, and then tri-stated for an additional clock before being driven by the new owner.
o/d	Open Drain signals allow multiple devices to share the pin as a wired-OR.

PCI Bus Signals

Signal Name	Type	Description
CLK	in	***CLOCK.*** This is the PCI Bus clock and is the timing reference for all PCI bus transactions. The AN3042 can operate with up to a 33 MHz PCI bus interface.
RST#	in	***RESET.*** This signal is the PCI bus reset. It is one of the few PCI signals which may be asserted or de-asserted asynchronously to the PCI bus clock (**CLK**).
AD[31:0]	t/s	***Address and Data.*** These signals represent the PCI bus address and data signals multiplexed on the same PCI pins. Information on these pins is identified as an address during the clock cycle in which the signal **FRAME#** is first asserted. This is termed the "address phase" of a bus transaction. Information on these pins represents valid read or write data when both **IRDY#** and **TRDY#** are asserted, based on the current cycle type as defined on the **C/BE** lines during the address phase. This condition is termed the "data phase" of a bus transaction.
C/BE#[3:0]	t/s	***Command and Byte Enables.*** These pins are used with the **AD[31:0]** pins. During the address phase of a bus operation, they identify the bus command to be performed. During the data phase of a bus operation they identify which bytes are involved.
PAR	t/s	***Parity.*** This PCI bus pin represents the even parity across the **A/D[31:00]** and **C/BE[3:0]** pins (36 pins) and is generated with a one clock delay.
FRAME#	s/t/s	***Cycle Frame.*** This PCI bus pin is asserted by the current bus master to signify the beginning of a bus transaction. Data transfers may continue in burst mode while **FRAME#** remains asserted. When **FRAME#** is de-asserted it indicates that the transaction is in the final data phase.
IRDY#	s/t/s	***Initiator Ready.*** This signal is driven by the current bus master (initiator) and asserted to indicate its ability to complete the current data phase. Data is transferred when both **IRDY#** and **TRDY#** are asserted, otherwise wait cycles will occur.
TRDY#	s/t/s	***Target Ready.*** This signal is driven by the selected bus target and asserted when that target is ready to complete the current data phase. Data is transferred when both **IRDY#** and **TRDY#** are asserted, otherwise wait cycles will occur.
STOP#	s/t/s	***Stop.*** The **STOP#** signal is driven by the selected bus target and is asserted when it wishes to cease the current data transaction.
IDSEL	in	***Initialization Device Select.*** This signal is used to gain access to the PCI configuration register space of a given PCI Bus agent.
DEVSEL#	s/t/s	***Device Select.*** The DEVSEL# signal is driven and asserted by the currently selected PCI bus target based on the current address and that target's assigned address range. Bus masters examine this signal to determine whether the desired device is present.
REQ#	t/s	***Request.*** This signal indicates to the bus arbiter that this device wishes to use the bus. It is a point-to-point signal that is driven whenever **RST#** is not asserted.

Signal Name	Type	Description
GNT#	t/s	***Grant.*** This point-to-point signal indicates that the bus has been granted to the requester. It is driven whenever **RST#** is not asserted and is ignored during the assertion of **RST#**.
PERR#	s/t/s	***Parity Error.*** This signal indicates that a parity error has occurred. It is driven by the target or master that is the receiver of data at the clock after the PAR signal becomes valid.
SERR#	o/d	***System Error.*** This open drain signal is driven by any device that detects odd parity during an address phase.
INTA#	o/d	***Interrupt A.*** This signal is asserted when interrupt servicing of the AN3042 device is required. The INTA# pin is a shared PCI bus signal and utilizes an open-drain element to allow a wired-OR.

Local System Signals

Signal Name	Type	Description
PCLKOUT2 **PCLKOUT1** **PCLKOUT0**	out	***Clock Outputs.*** These pins provide three buffered copies of the PCI bus clock. When the AN3042 is to be operated fully synchronous to the PCI bus clock, it is necessary to connect one of the clock outputs to the **CLKIN** pin (described below).
CLKIN	in	***Clock In.*** This pin provides the timing reference for local bus signals. The **CLKIN** pin can be driven by an external clock (asynchronous to the PCI Bus clock). In order to operate synchronous to the PCI bus clock, one of the buffered copies of the clock, **PCLKOUT[2:0],** may be used as input to **CLKIN**.
RSTOUT#	out	***Reset Out.*** This pin provides a buffered version of the PCI bus signal, **RST#.**
RSTOUTD# **RSTOUTD**	out	***Reset Out Delayed.*** This pin is similar to the **RSTOUT#** pin described above, however **RSTOUTD#** remains asserted until released by the host interface via software control. This allows the AN3042 to hold the local processor in reset until the host processor is ready to release it.
IRQ_OUT#	out	***Interrupt Request Out.*** This signal is used to trigger an interrupt on the local microprocessor. A variety of host triggered events can be used to cause the assertion of this interrupt request output. This signal may be masked using the Local Interrupt Control/Status Register.
IRQ_IN#	in	***Interrupt Request In.*** This signal, when asserted, will result in the AN3042 driving the PCI bus **INTA#** signal and therefore cause an interrupt of the host system. This signal may be masked using the Host Interrupt Control/Status Register.
TEST_MODE	in	***Test Mode.*** When high, this pin puts the AN3042 into a factory test mode. When high and READ# is low, all outputs are tri-stated. When READ# is high, the part is put into a factory test mode and the WRITE# signal is used as control.

Local Bus Interface Signals

Signal Name	Type	Description
ADR[14:2]	in	***Address.*** These signals identify the local memory location. When the local processor outputs multiplexed address and data, those lines need to be tied to both the **DQ[14:2]** and **ADR[14:2]**.
BE#[3:0]	in	***Byte Enables.*** The Byte Enable inputs identify the specific bytes involved in an access. When the AN3042 operates in a 16 bit or 8 bit wide local mode, **BE3#** becomes **ADR1.** In 8 bit wide mode, **BE2#** becomes **ADR0**. The pins are also used as size and encoded byte enables when interfacing to Motorola processors; see the Local Bus section for definition.
DQ[31:0]	t/s	***Data.*** AN3042 data input and output are provided on these bi-directional pins.
SELECT#	in	***Chip Select.*** This signal must be asserted for the full duration of any access.
ALE	in	***Address Latch Enable.*** The local address provided on **ADR[14:2]** is latched on the trailing edge (from active to inactive) of this signal. The polarity of ALE is programmable.
STROBE	in	***Address Strobe.*** The assertion of this signal begins a memory access and indicates that a valid address has been latched through **ALE** or is provided at the pins (if **ALE** is not used and is tied active). The address is provided on the **ADR[14:2]** pins (during non-multiplexed mode), or on the **DQ[14:2]** (during multiplexed mode).
WRITE# **READ#**	in	***Write and Read signals.*** These signals control the transfer of data to and from the local data bus. The polarity and function of these signals is programmable so that they can be interfaced to processors that support WR#/RD or RD#/WR, as well as separate RD/RD# and WR/WR# signals. When the TEST_MODE signal is asserted, these two signals are used for test functions.
BLAST#	in	***Burst Last.*** The signal indicates the end of a burst transfer. This signal has two modes. It can be active during the burst and go inactive when the burst is over, or it can go active during the last data phase of the burst.
RDY_IN# **RDY_IN**	in	***Ready In.*** The assertion of these signals indicates that the local processor is prepared to complete the current data transaction.
RDY_OUT#	out	***Ready Out.*** When this signal is asserted it indicates that the AN3042 is ready to complete the current access. The polarity of this signal is programmable.

Local Configuration Signals

Signal Name	Type	Description
SCL	oc	***Serial Clock.*** This pin is the clock output to be used with an external I^2C serial memory device. A pull-up resistor is required.

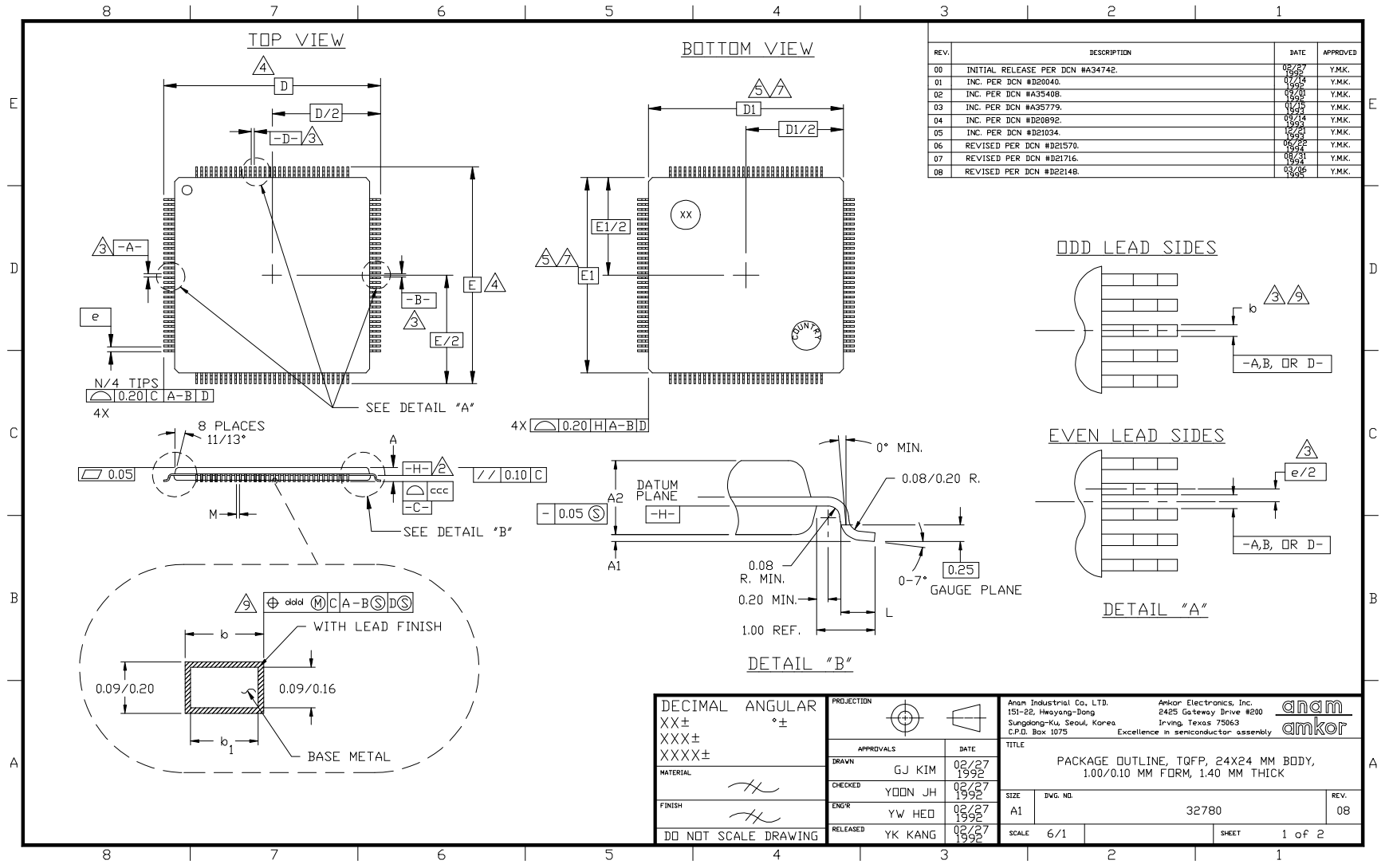
Signal Name	Type	Description
SDA	oc	***Serial Data.*** This pin is the bi-directional data pin to be used with an external I^2C serial memory device. A pull-up resistor is required.

Power Pins

Signal Name	Type	Description
VSSP1 - VSSP8, VSS1 - VSS12	gnd	***Ground.*** These pins are ground pins (0 volts).
VDDP1 VDDP8, VDD1 VDD8	power	***Power.*** These pins provide power, nominally 3.3 volts.

Package Drawing

The AN3042Q is available in a 160-pin plastic thin quad flat pack.



REV.	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE PER DCN #A34742.	02/27 1992	Y.M.K.
01	INC. PER DCN #D20040.	07/14 1992	Y.M.K.
02	INC. PER DCN #A35408.	03/01 1993	Y.M.K.
03	INC. PER DCN #A35779.	04/15 1993	Y.M.K.
04	INC. PER DCN #D20892.	09/14 1993	Y.M.K.
05	INC. PER DCN #D21034.	12/20 1993	Y.M.K.
06	REVISED PER DCN #D21570.	06/22 1994	Y.M.K.
07	REVISED PER DCN #D21716.	08/31 1994	Y.M.K.
08	REVISED PER DCN #D22148.	03/06 1995	Y.M.K.

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BV.

SYMBOL	JEDEC VARIATION BV — ALL DIMENSIONS IN MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			1.60	
A_1	0.05	0.10	0.15	
A_2	1.35	1.40	1.45	
D		26.00 BSC.		4
D_1		24.00 BSC.		7,8
E		26.00 BSC.		4
E_1		24.00 BSC.		7,8
L	0.45	0.60	0.75	
M	0.14			
N		*160, 176		
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

* NOTE: THE 160 LEAD IS A COMPLIANT DEPOPULATION OF THE 176 LEEAD MO-136 VARIATION BV.

TITLE: PACKAGE OUTLINE, TQFP, 24X24 MM BODY, 1.00/0.10 MM FORM, 1.40 MM THICK
SIZE A1 | DWG. NO. 32780 | REV. 08
SCALE 6/1 | SHEET 2 of 2

Pin List

Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.
VDD1	1	VSSP3	41	VDDP7	81	VDD6	121
ADR[8]	2	C/BE#[3]	42	C/BE#[0]	82	DQ[21]	122
ADR[7]	3	IDSEL	43	AD[7]	83	DQ[22]	123
ADR[6]	4	AD[23]	44	AD[6]	84	DQ[23]	124
ADR[5]	5	AD[22]	45	AD[5]	85	DQ[24]	125
ADR[4]	6	NC1	46	AD[4]	86	DQ[25]	126
ADR[3]	7	AD[21]	47	VSSP8	87	DQ[26]	127
ADR[2]	8	AD[20]	48	VDDP8	88	DQ[27]	128
VSS1	9	AD[19]	49	AD[3]	89	DQ[28]	129
ALE	10	VSSP4	50	AD[2]	90	VSS8	130
IRQ_IN#	11	VDDP4	51	AD[1]	91	VDD7	131
IRQ_OUT#	12	AD[18]	52	AD[0]	92	DQ[29]	132
VSS2	13	AD[17]	53	VSS4	93	DQ[30]	133
VDD2	14	AD[16]	54	VDD3	94	DQ[31]	134
RSTOUTD	15	C/BE#[2]	55	DQ[0]	95	VSS9	135
RSTOUTD#	16	NC2	56	DQ[1]	96	BLAST#	136
RSTOUT#	17	FRAME#	57	DQ[2]	97	READ#	137
VSS3	18	IRDY#	58	DQ[3]	98	WRITE#	138
SELECT#	19	TRDY#	59	DQ[4]	99	RDY_IN	139
SDA	20	VSSP5	60	DQ[5]	100	RDY_IN#	140
SCL	21	VDDP5	61	DQ[6]	101	RDY_OUT#	141
TEST_MODE	22	DEVSEL#	62	VSS5	102	PCLKOUT0	142
INTA#	23	STOP#	63	VDD4	103	PCLKOUT1	143
RST#	24	PERR#	64	DQ[7]	104	PCLKOUT2	144
CLK	25	NC3	65	DQ[8]	105	VSS10	145
VSSP1	26	SERR#	66	DQ[9]	106	CLKIN	146
VDDP1	27	PAR	67	DQ[10]	107	VSS11	147
GNT#	28	C/BE#[1]	68	DQ[11]	108	VDD8	148
REQ#	29	AD[15]	69	DQ[12]	109	BE#[3]	149
AD[31]	30	VSSP6	70	DQ[13]	110	BE#[2]	150
AD[30]	31	VDDP6	71	VSS6	111	BE#[1]	151
AD[29]	32	AD[14]	72	VDD5	112	BE#[0]	152
VSSP2	33	AD[13]	73	DQ[14]	113	STROBE	153
VDDP2	34	AD[12]	74	DQ[15]	114	ADR[14]	154
AD[28]	35	AD[11]	75	DQ[16]	115	ADR[13]	155
AD[27]	36	AD[10]	76	DQ[17]	116	ADR[12]	156
AD[26]	37	AD[9]	77	DQ[18]	117	ADR[11]	157
AD[25]	38	AD[8]	78	DQ[19]	118	ADR[10]	158
AD[24]	39	NC4	79	DQ[20]	119	ADR[9]	159
VDDP3	40	VSSP7	80	VSS7	120	VSS12	160

Memory Map

AN3042 resources are accessed from the PCI bus as an offset from Base Address Register 0 (BAR 0), unless otherwise indicated. Resources are also accessed from the Local bus when the SELECT# pin is active. PCI I/O access to this memory map is also available via I/O pointers located at Base Address Register 1 (BAR 1). The memory map covers a continuous 32KB address space.

Memory Contents	Address [14:0], Byte Offset	Size
I_2O Specific Registers	0x0000 - 0x03FF	1KB
Operations Registers	0x0400 - 0x07FF	1KB
reserved	0x0800 - 0x1FFF	6KB
Direct Access to PCI Bus (for Local bus Only)	0x2000 - 0x3FFF	8KB
Shared Memory	0x4000 - 0x7FFF	16KB

PCI Bus

The PCI bus of the AN3042 operates per the PCI Specification revision 2.1. This section describes the specific PCI functions supported by the AN3042. Reference URL: http://www.pcisig.com/

PCI Configuration Space

PCI Configuration Space				
31	**16**	**15**	**0**	**Address, Byte Offset**
Device ID, *RO*		Vendor ID, *RO*		0x00
Status, *CS*		Command, *CS*		0x04
Class Code, *RO*			Revision ID, *RO*	0x08
BIST (not used) 0x00	Header Type 0x00	Latency Timer, *RW*	Cache Line Size, *RW*	0x0C
Base Address Register #0 -- 32KBytes Memory Space, *RW*				0x10
Base Address Register #1 -- 8 Bytes I/O Space, *RW*				0x14
Base Address Register #2 (not used) 0x0000				0x18
Base Address Register #3 (not used) 0x0000				0x1C
Base Address Register #4 (not used) 0x0000				0x20
Base Address Register #5 (not used) 0x0000				0x24
Cardbus CIS Pointer, *RO*				0x28
Subsystem Device ID, *RO*		Subsystem Vendor ID, *RO*		0x2C
Expansion ROM Base Address (not used) 0x0000				0x30
Reserved 0x0000				0x34
Reserved 0x0000				0x38
MAX_LAT, *RO*	MIN_GNT, *RO*	Interrupt Pin, *RO*	Interrupt Line, *RW*	0x3C

Legend for PCI Configuration Space Table	
0x00 or 0x0000	Hardwired to zero
RO	Read-only: may be initialized by EEPROM across I^2C serial interface
CS	Control and status register
RW	Read/write

Vendor ID

Address - 0x01 - 0x00

Default Value: 0x12BE

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This 2-byte register contains the Vendor ID assigned by the PCI SIG. The default value is the Anchor Chips Incorporated Vendor ID. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own vendor ID.

Device ID

Address - 0x03 - 0x02

Default Value: 0x3042

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This 2-byte register contains the device ID assigned by the manufacturer. The default value is the AN3042 chip device ID. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own device ID.

Command

Address - 0x05 - 0x04

Default Value: 0x0000

Read/Write

This 2-byte register contains bits for device control. These bits are normally set by the system BIOS. The following bits are supported:

Bit 0 -- enable response to I/O space accesses;

Bit 1 -- enable response to Memory space accesses;

Bit 2 -- enable PCI bus master operation, (may be initialized over the I^2C serial interface);

Bit 3 -- enable special cycle monitoring, (but AN3042 performs no special function as a target);

Bit 4 -- enable bus master use of the Memory Write and Invalidate command;

Bit 6 -- enable the PERR# signal for host notification of data parity errors;

Bit 8 -- enable the SERR# signal for host notification of system errors; and

Bit 9 -- enable fast back-to-back transactions to different agents, (but AN3042 does not generate).

Status

Address - 0x07 - 0x06

Default Value: 0x0280

Read-only and Write-1-to-Clear except as indicated

This 2-byte register contains bits for device status. The following bits are supported:

Bit 7 -- read-only bit set to indicate, as a target, the chip can accept fast back-to-back transactions;

Bit 8 -- set when PERR# is asserted;

Bits 10 and 9 -- read-only bits set to 0x1 indicating medium response timing for DEVSEL#;

Bit 12 -- set when, as a master, the chip's transaction has been terminated with Target-Abort;

Bit 13 -- set when, as a master, the chip terminates a transaction with Master-Abort;

Bit 14 -- set when SERR# is asserted; and

Bit 15 -- set whenever a parity error is detected.

Revision ID

Address - 0x08

Default Value: 0x01

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This 1-byte register contains the Revision ID assigned by the manufacturer. The default value is set by Anchor Chips at manufacturing time. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own Revision ID.

Class Code

Address - 0x0B - 0x09

Default Value: 0x0E0001

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This 3-byte register contains the class code assigned by the manufacturer. The default value indicates an I_2O base class (0x0E), a sub-class of 0x00, and the programming interface that supports system interrupt capability (0x01). Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own class code.

Cache Line Size

Address - 0x0C

Default Value: 0x00

Read/Write

This register contains the cache line size in DWORDs. The only valid size is 0x08; any other value written will result in a 0x00 being written to the register. The value in this register is used to control when the master can perform Memory Write and Invalidate cycles. Additionally, the type of memory read command is determined by this value; (i.e., Memory Read, Memory Read Line, or Memory Read Multiple).

Latency Timer

Address - 0x0D

Default Value: 0x00

Read/Write

This register controls how quickly the master must get off the bus if GNT# is removed. The AN3042 implements bits [7:3] of this register, providing a granularity of eight clocks.

Base Address Register 0 (Memory Type Access)

Address - 0x13 - 0x10

Default Value: 0x00000000

Read all 32-bits, Write bits [31 - 15]

This register provides the base address of the AN3042 memory map. Bits [31 - 15] are read/write, indicating to the system BIOS that the shared memory space is 32K bytes. If a PCI memory transaction has address bits [31 - 15] matching the contents of this register and memory accesses are enabled (by Command register bit 1), then the AN3042 chip will acknowledge and accept the transfer.

Base Address Register 1 (I/O Type Access)

Address - 0x17 - 0x14

Default Value: 0x00000001

Read all 32-bits, Write bits [31 - 3]

This register provides the base address of the AN3042 I/O pointer space. Bits [31 - 3] are read/write, indicating to the system BIOS that the I/O pointer space is 8 bytes. If a PCI I/O transaction has address bits [31 - 3] matching the contents of this and I/O accesses are enabled (by Command register bit 0), then the AN3042 will acknowledge and accept the transfer.

Cardbus CIS Pointer

Address - 0x2B - 0x28

Default Value: 0x00000000

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This register contains the Cardbus Card Information Structure (CIS). Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own CIS pointer value.

Subsystem Vendor ID

Address - 0x2D - 0x2C

Default Value: 0x0000

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This 2-byte register contains the subsystem vendor ID chosen by the manufacturer. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own subsystem vendor ID.

Subsystem Device ID

Address - 0x2F - 0x2E

Default Value: 0x0000

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This 2-byte register contains the subsystem device ID chosen by the manufacturer. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own subsystem device ID.

Interrupt Line

Address - 0x3C

Default Value: 0x00

Read/Write

This single-byte register contains the interrupt line routing.

Interrupt Pin

Address - 0x3D

Default Value: 0x00

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This single-byte register contains the interrupt pin information. The default value indicates that the AN3042 chip is not connected to the interrupts on the PCI bus. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to specify which interrupt pin is on the bus. Only bits [2 -0] are implemented. All four Interrupt numbers are supported, (INTA# through INTD#).

MIN_GNT

Address - 0x3E

Default Value: 0x00

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This single-byte register contains the minimum grant time in 1/4 microsecond increments needed for efficient operation. The default value indicates the add-in card has no major requirements for the setting of the latency timer. The latency timer governs how long a burst transaction may use the PCI bus. Whatever the value, the AN3042 itself does not use the MIN_GNT data. It is used as a means to communicate system requirements to the host. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own minimum grant time reflective of their add-in card requirements.

MAX_LAT

Address - 0x3F

Default Value: 0x00

Read-only: Can be initialized from the external memory accessed via the I^2C serial interface

This single-byte register contains the minimum latency time in 1/4 microsecond increments needed for efficient operation. The default value indicates the add-in card has no major requirements for how soon it needs access to the PCI bus once it has requested an access. Whatever the value, the AN3042 itself does not use MAX_LAT data. It is used as a means to communicate system requirements to the host. Using the I^2C serial interface for initialization provides a method to allow a manufacturer to load their own minimum latency time reflective of their add-in card requirements.

PCI Bus Commands

All Memory and I/O commands are supported as target and master.

- I/O Read C/BE#[3:0] = 0x2
- I/O Write C/BE#[3:0] = 0x3
- Memory Read C/BE#[3:0] = 0x6
- Memory Write C/BE#[3:0] = 0x7
- Memory Read Multiple C/BE#[3:0] = 0xC
- Memory Read Line C/BE#[3:0] = 0xE
- Memory Write and Invalidate C/BE#[3:0] = 0xF

All Configuration commands are supported as target and master. Additionally, the AN3042 can perform these accesses on its own PCI Configuration space. Control originates from the Local bus using the AN3042 Direct Access feature. This is a necessary feature for the AN3042 to perform as a Host Bridge device. For details, see the Direct Access and Host Bridge descriptions in the AN3042 Operations section.

- Configuration Read C/BE#[3:0] = 0xA
- Configuration Write C/BE#[3:0] = 0xB

Interrupt Acknowledge and Special Cycle are supported on master cycles. As a target, no action is performed by the AN3042.

- Interrupt Acknowledge C/BE#[3:0] = 0x0
- Special Cycle C/BE#[3:0] = 0x1

The following command is not supported, a target access will result in no response by the AN3042 as per the PCI specification.

- Dual-Address Cycle C/BE#[3:0] = 0xD

The following commands are PCI Reserved and are not responded to as per PCI specification.

- Reserved C/BE#[3:0] = 0x4
- Reserved C/BE#[3:0] = 0x5
- Reserved C/BE#[3:0] = 0x8
- Reserved C/BE#[3:0] = 0x9

PCI I/O Pointers

I/O Address Pointer

Address - 0x1 - 0x0

Default Value: unknown, not initialized

Write-only

The value written to this location is the offset into the AN3042 Memory Map. Bit 15 is don't care.

I/O Data Pointer

Address - 0x7 - 0x4

Default Value: unknown, not initialized

Read/Write

Upon a write to the pointer, the data shall be written to the location in the AN3042 Memory Map specified by the contents of the I/O address pointer. If an I/O read access to the pointer, then the data at the location in the AN3042 Memory Map which is specified by the contents of the I/O address pointer shall be returned.

Local Bus

General Description

The AN3042 provides a configurable local processor bus interface which can provide direct connection to several processor types. The interface is synchronous to the CLKIN signal. The CLKIN signal can be tied to the local processor's clock, a derivative, or an independent clock source. To run the local interface at PCI clock speeds, any one of the PCLKOUT[2:0] pins should be connected to CLKIN.

The basic local processor bus transaction consists of an address phase, followed by one or more data phases. The interface signals are generally divided into those signals that qualify the address phase (ALE, STROBE, SELECT#, READ#, WRITE#, and ADR[14:2],), and those that qualify data phases, (RDY_IN#, RDY_IN, BLAST#, BE#[3:0], and DQ[31:0]). The AN3042 drives RDY_OUT# to signal the need for wait states on the local processor bus as well as an indication of valid data on DQ[31:0] during read access of the AN3042. Note that several of the AN3042 local bus signals have configurable polarity. These are: ALE, BLAST#, RDY_OUT#, and STROBE. Also, the READ# and WRITE# signals have special combined signal modes.

The basic local-bus cycle starts with the address phase. The address phase is defined as both STROBE and SELECT# active at the rising edge of CLKIN. Also sampled at this time are the READ# and WRITE# signals to determine if the access is a read or write. If the access is a read, then the AN3042 will begin driving the DQ bus at the next CLKIN rising edge.

There are two ways to get an address into the AN3042. With ALE tied active, the address is latched during the address phase. That is, when STROBE and SELECT# are active, the address on the ADR[14:2] pins is latched on the rising edge of CLKIN. The second way is to use the trailing edge of ALE to latch the address. The AN3042 still needs a valid address phase (STROBE and SELECT# active at the rising edge of CLKIN) before it will begin processing the address. A valid and stable address must occur before the trailing edge of ALE and before the rising edge of CLKIN where STROBE and SELECT# are active.

After the address phase come wait states and data phases. The STROBE signal can be active or inactive during wait and data phases. A data phase occurs when the RDY_IN# and RDY_IN inputs and the RDY_OUT# output are all active at the rising edge of CLKIN. If any ready signal is inactive, then the next clock cycle is a wait state. The BE#[3:0] pins are sampled during the data phase of write cycles to determine which data bytes are to be written. The data on the DQ pins is also latched at this time.

The BLAST# signal is sampled during the data phase to determine if the last data phase is occurring. In one mode, an inactive level during the data phase indicates that there are more data phases in the transaction and that the address that was captured in the address phase should be updated. When BLAST# is active during the data phase, it indicates that this is the last data phase of the transaction. In the other mode, BLAST# is active during every data phase and goes inactive with RDYIN# and RDYIN at the end of the last data phase. In both cases, if the access is a read, then the AN3042 will stop driving the DQ bus synchronously with the rising edge of CLKIN for that data phase.

Interface Definitions

8-Bit Interface

The 8-bit interface option is selected using BW[1:0] = '00'. Only data lines DQ[7:0] are used. The unused portion of the data bus, DQ[31:8] must be tied high or low; the bits cannot be left floating. The least two significant bits of the local address bus should be connected to the byte enable pins BE#[3:2].

BW[1:0]	BEMODE	A1, A0 (BE#[3], BE#[2])	DQ [7:0] Accessed Data
00	X	00	Data[7:0]
00	X	01	Data[15:8]
00	X	10	Data[23:16]
00	X	11	Data[31:24]

Connect

- BE#[3] = A1
- BE#[2] = A0
- BE#[1] = Logic high
- BE#[0] = Tie to RDY_IN#

16-Bit Interface

The 16-bit interface option is selected using BW[1:0] = '01'. Only data lines DQ[15:0] are used. The unused portion of the data bus, DQ[31:16] must be tied high or low; the bits cannot be left floating. The least significant bit of the 16-bit addressed bus should be connected to the byte enable pins BE#[3].

BW[1:0]	BEMODE	A1 (BE#[3])	DQ [15:0] Accessed Data
01	X	00	Data[15:0]
01	X	01	Data[31:16]

Connect

- BE#[3] = A1
- BE#[2] = Not used, should be tied high
- BE#[1] = BE1, UDS, BHE (Byte Enable 1, Upper Data Strobe, Byte High Enable)
- BE#[0] = BE0, LDS, DEN (Byte Enable 0, Lower Data Strobe, Data Enable)

Notes: BE#[1:0] are used as byte enables. If the processor always does 16-bit accesses, then these can be tied active low. These byte enables can also be used for Upper Data Strobe (UDS) and Lower Data Strobe (LDS) for processors which produce these signals.

The least significant bit of the local address bus is tied to BE#[3], and it *must be valid during the address phase.* This input must be incremented (toggled) at the end of each data phase. Bursts to the 16-bit interface do not need to start on a DWORD boundary. The internal DWORD address will automatically increment after a data phase where BE#[3] is high.

32-Bit Interface

The 32-bit interface option is selected using BW[1:0] = '10' or BW[1:0] = '11'. Data lines DQ[31:0] are used. With BW[1:0] = '10', the byte enables are used directly as byte write enables. With BW[1:0] = '11', however, the meaning of the byte enables is determined from the following tables (based on BEMODE).

Connect for encoded byte enables

- BE#[3] = SIZ1 (Operand Transfer Size, bit 1)
- BE#[2] = SIZ0 (Operand Transfer Size, bit 0)
- BE#[1] = A1
- BE#[0] = A0

BW[1:0]	BEMODE	Interpretation
10	X	Use byte enables for all 4 byte lanes
11	0	Use the following table

External BE#[3:0]	Interpretation -- 'byte' terminology here uses byte 3 as least significant byte	Internal BE#[3:0] for writes
0000	all-byte write starting at byte 0 (DQ[31:0])	0000
0001	all-byte write starting at byte 1 (DQ[23:0]) (truncated to three bytes)	1000
0010	all-byte write starting at byte 2 (DQ[15:0]) (truncated to two bytes)	1100
0011	all-byte write starting at byte 3 (DQ[7:0]) (truncated to one byte)	1110
0100	single-byte write starting at byte 0 (DQ[31:24])	0111
0101	single-byte write starting at byte 1 (DQ[23:16])	1011
0110	single-byte write starting at byte 2 (DQ[15:8])	1101
0111	single-byte write starting at byte 3 (DQ[7:0])	1110
1000	two-byte write starting at byte 0 (DQ[31:16])	0011
1001	two-byte write starting at byte 1 (DQ[23:8])	1001
1010	two-byte write starting at byte 2 (DQ[15:0])	1100
1011	two-byte write starting at byte 3 (DQ[7:0]) (truncated to one byte)	1110
1100	three-byte write starting at byte 0 (DQ[31:8])	0001
1101	three-byte write starting at byte 1 (DQ[23:0])	1000
1110	three-byte write starting at byte 2 (DQ[15:0]) (truncated to two bytes)	1100
1111	three-byte write starting at byte 3 (DQ[7:0]) (truncated to one byte)	1110

BW = '11', BEMODE = '0', is used to interface to 32-bit processors that provide a byte address, instead of fully decoded byte enables. For example, this mode can be used to interface the Motorola 68020- or 68030-type bus to the AN3042. The SIZ1 and SIZ0 signals of the 68020 are connected to the BE#[3] and BE#[2] pins, respectively, and the A1 and A0 signals are connected to the BE#[1] and BE#[0] pins on the AN3042.

BW[1:0]	BEMODE	Interpretation
11	1	Use the following table

External BE#[3:0]	Interpretation	Internal BE#[3:0] for writes
00xx	32-bit write DQ[31:0]	0000
0100	8-bit write DQ[31:24]	0111
0101	8-bit write DQ[23:16]	1011
0110	8-bit write DQ[15:8]	1101
0111	8-bit write DQ[7:0]	1110
100x	16-bit write DQ[31:16]	0011
101x	16-bit write DQ[15:0]	1100
11xx**	burst of four 32-bit writes, BLAST# not used	0000

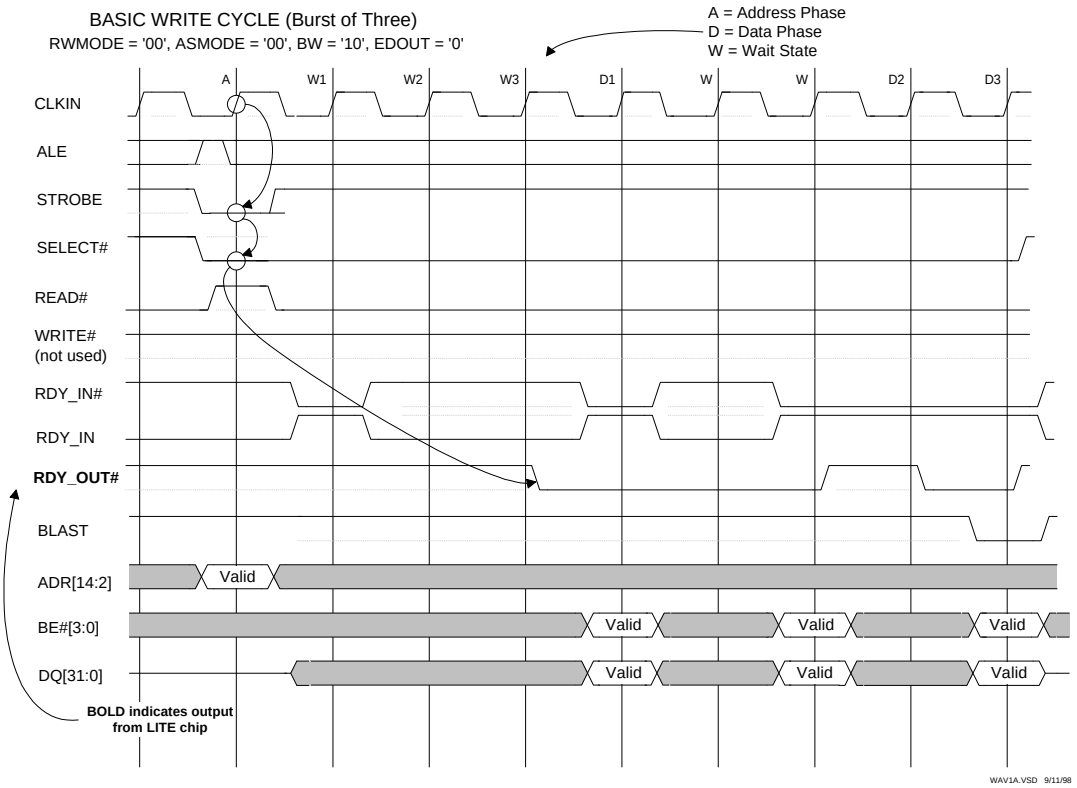
** Note: This encoding, {BW[1:0], BEMODE, BE[3:2]} = {11111}, results in a burst of four DWORD. BLAST# is not used and should remain inactive (high).

BW = '11', BEMODE = '1' is used to interface to 32-bit processors that provide a byte address, instead of fully decoded byte enables. The SIZ1 and SIZ0 signals of the Motorola 68040-style interface are connected to the BE#[3] and BE#[2] pins, respectively, and the A1 and A0 signals are connected to the BE#[1] and BE#[0] pins on the AN3042. A cache-line fill is triggered using the SIZ1 and SIZ0 pins on the 68040-type bus. When these bits are set to '11', the AN3042 will interpret this as a burst-of-four, ignoring the burst last signal BLAST#.

Timing Diagrams

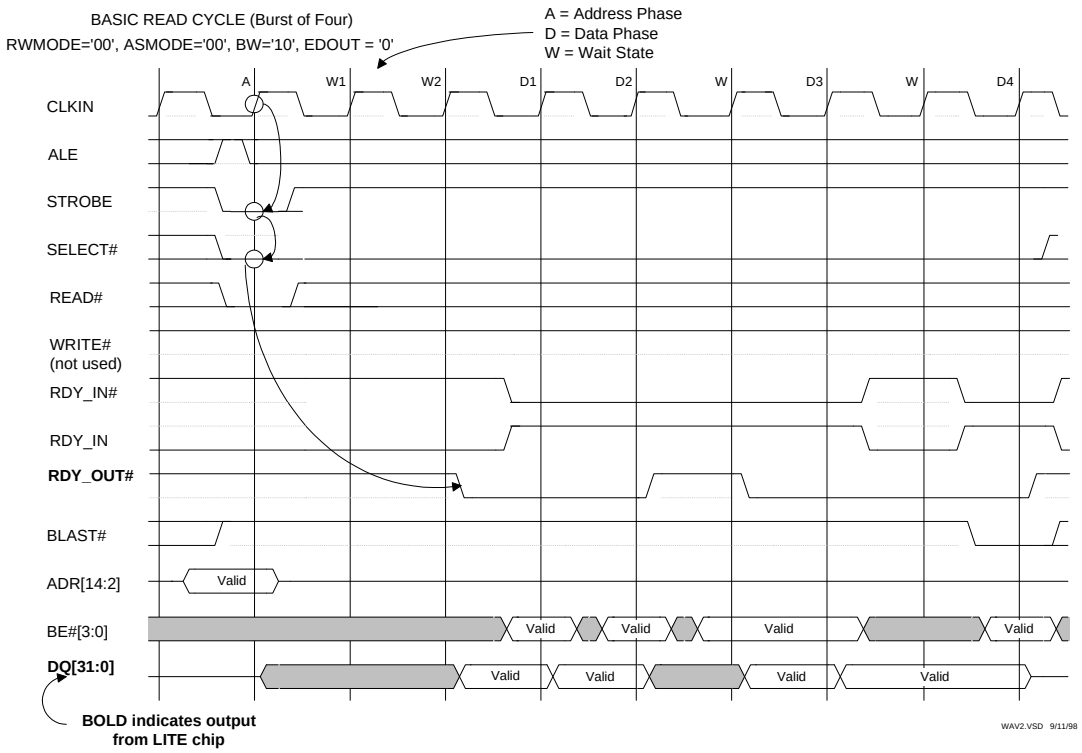
Write Cycle

A basic write cycle is illustrated below. It includes a burst of three data phases on a 32-bit wide bus.



Read Cycle

The basic read cycle differs from the write cycle only in the level of the READ# and WRITE# signals, and the timing and driving of the data bus DQ. A basic read burst of four data phases on a 32-bit wide bus is illustrated.

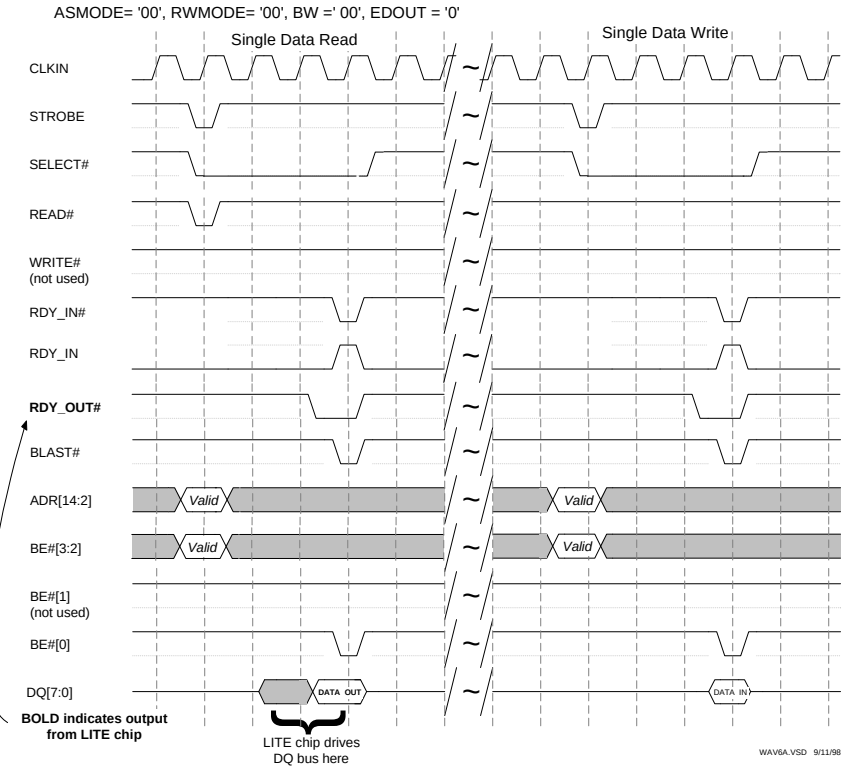


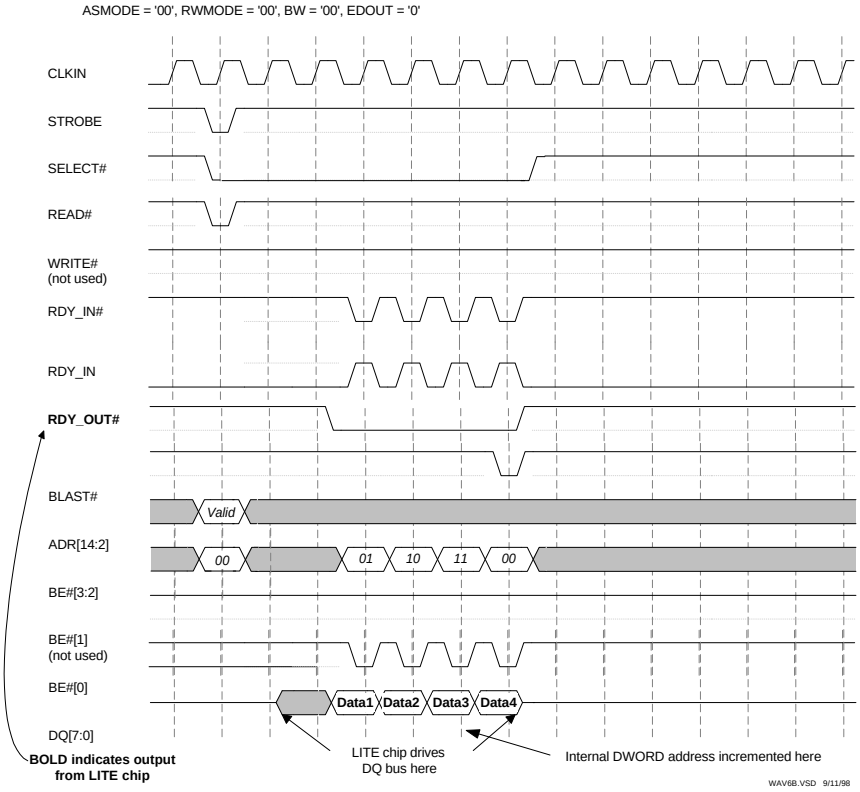
Basic 8-bit Interface

The following two waveforms illustrate the operation of the 8-bit interface mode. Note that only data lines DQ[7:0] are used. DQ[31:8] are unused and must be tied high or low; they cannot be left floating. The least significant bits of the local address, A[1] and A[0], must be connected to the byte enable pins BE#[3] and BE#[2], respectively. These must be valid during the address phase.

In burst operation, BE#[3:2] are inputs used at A1 and A0 of the local address bus. Bursts to the 8-bit interface do not need to start on a DWORD boundary. The internal DWORD address will automatically increment after a data phase where BE#[3:2] equals '11', (A[1:0] = '11').

The first waveform illustrates single cycle operation and the second illustrates data burst operation.


ASMODE= '00', RWMODE= '00', BW =' 00', EDOUT = '0'
Single Data Read
Single Data Write
CLKIN
STROBE
SELECT#
READ#
WRITE#
(not used)
RDY_IN#
RDY_IN
RDY_OUT#
BLAST#
ADR[14:2]
BE#[3:2]
BE#[1]
(not used)
BE#[0]
DQ[7:0]
Valid
DATA OUT
DATA IN
BOLD indicates output from LITE chip
LITE chip drives DQ bus here
WAV6A.VSD 9/11/98


ASMODE = '00', RWMODE = '00', BW = '00', EDOUT = '0'
CLKIN
STROBE
SELECT#
READ#
WRITE#
(not used)
RDY_IN#
RDY_IN
RDY_OUT#
BLAST#
ADR[14:2]
BE#[3:2]
BE#[1]
(not used)
BE#[0]
DQ[7:0]
Valid
00
01
10
11
00
Data1
Data2
Data3
Data4
BOLD indicates output from LITE chip
LITE chip drives DQ bus here
Internal DWORD address incremented here
WAV6B.VSD 9/11/98

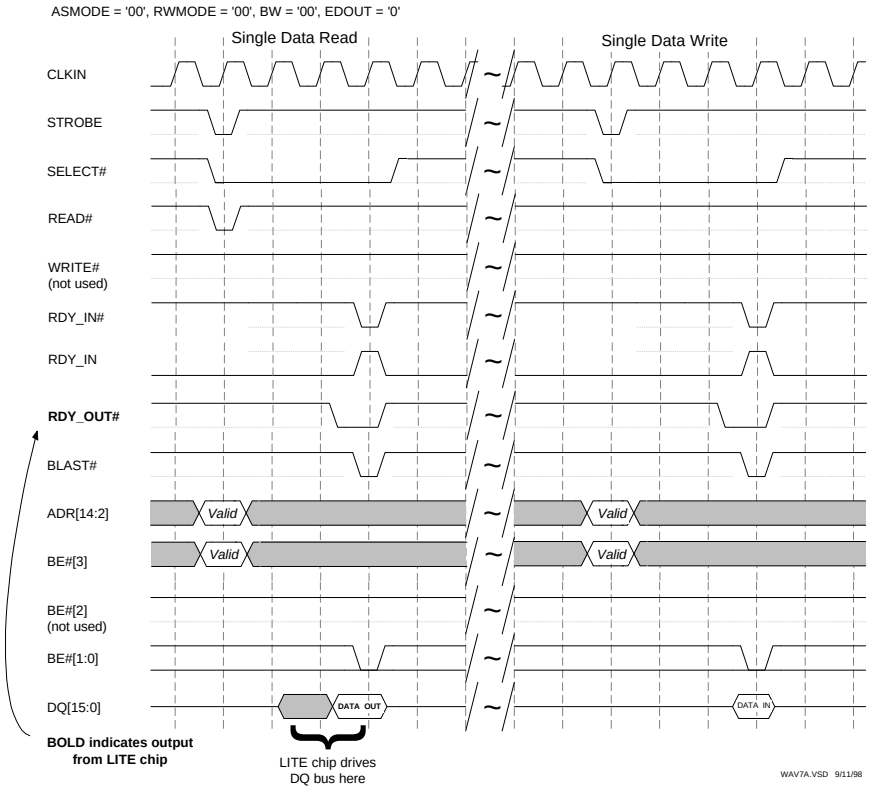
Basic 16-bit Interface

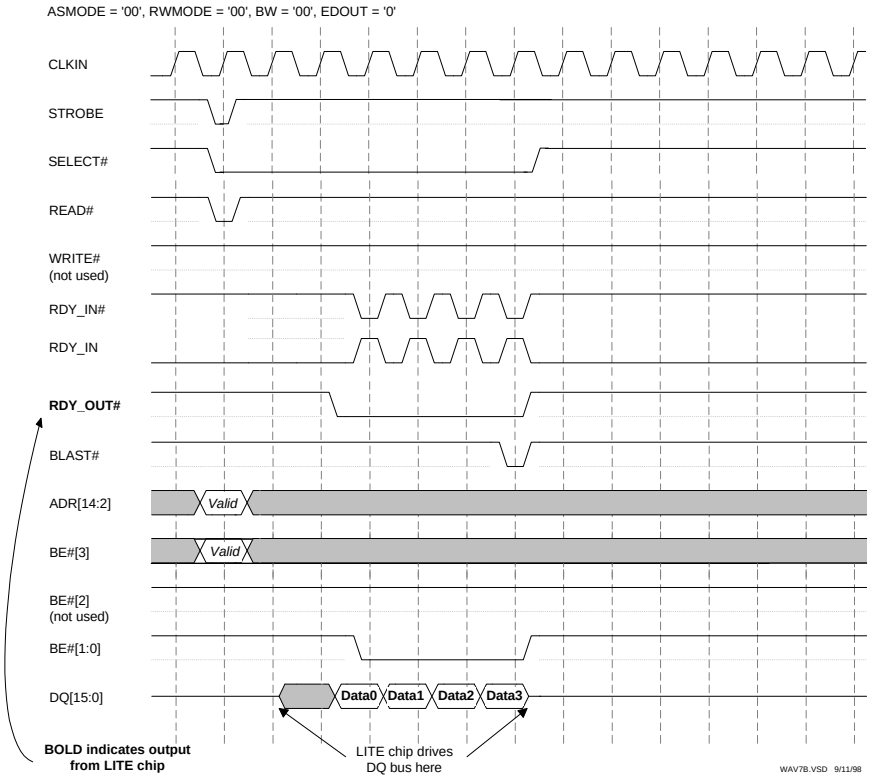
The following two waveforms illustrate the operation of the 16-bit interface mode. Note that only data lines DQ[15:0] are used. DQ[31:16] are unused and must be tied high or low; they cannot be left floating. The least significant bit of the local address of the 16-bit bus, A[1], must be connected to the byte enable pin BE#[3]. It must be valid during the address phase.

Note that BE#[1:0] are used as byte enables. If the processor always does 16-bit accesses, then these can be tied active low. These byte enables can also be used for Upper Data Strobe (UDS) and Lower Data Strobe (LDS) for processors which produce these signals.

In burst operation, BE#[3] must be incremented (toggled) at the end of each data phase. Bursts to the 16-bit interface do not need to start on a DWORD boundary. The internal DWORD address will automatically increment after a data phase where BE#[3] equals '1', (A[1] = '1').

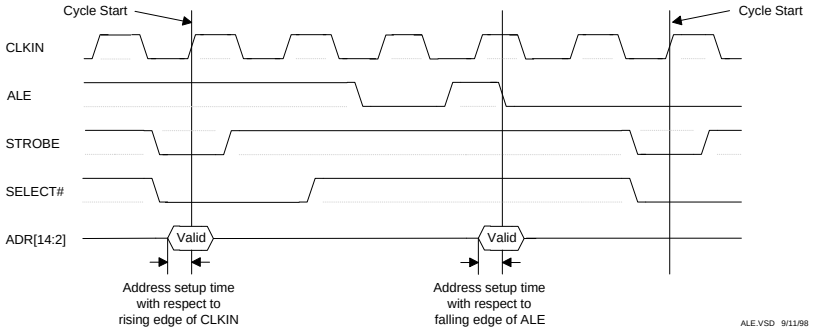
The first waveform illustrates single cycle operation and the second illustrates data burst operation.





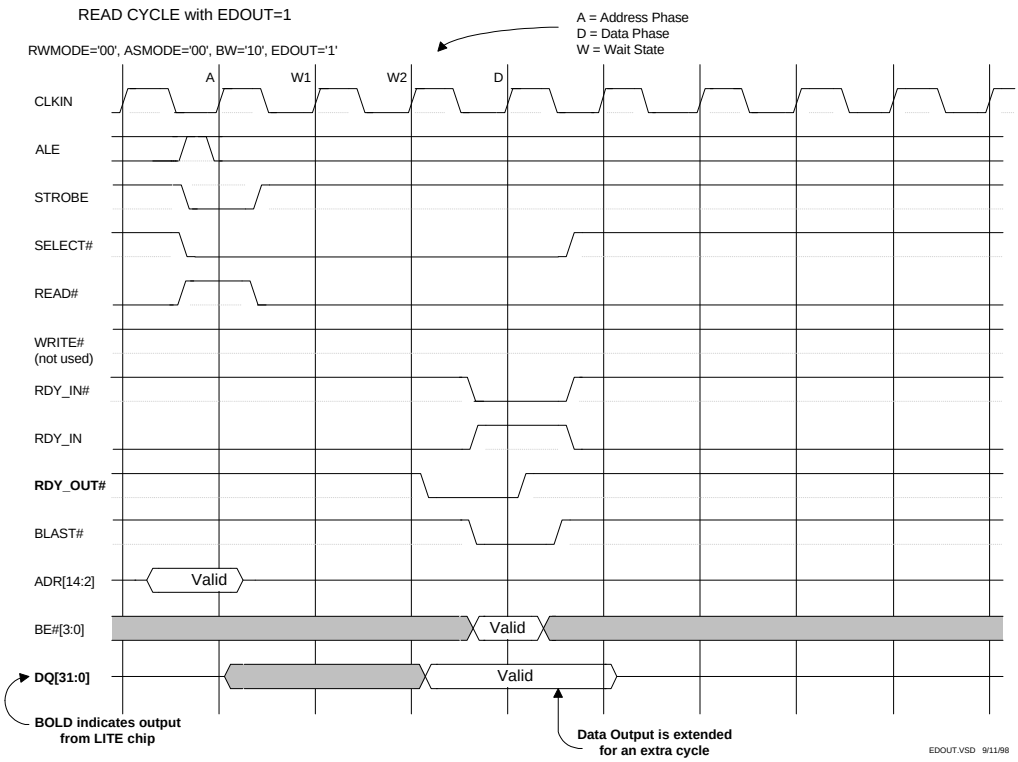
ALE -- Address Latch Enable

The ALE signal may be used in two modes. With ALE tied active, the address is latched during the address phase. That is, when the STROBE and SELECT# signals are active, the address on the ADR[14:2] pins is latched on the rising edge of CLKIN. The second way is to use the trailing edge of ALE to latch the address. The AN3042 still needs a valid address phase (STROBE and SELECT# active at the rising edge of CLKIN) before it will begin processing the address. A valid and stable address must occur before the trailing edge of ALE and before the rising edge of CLKIN where STROBE and SELECT# are active. The active polarity of ALE is defined in the Operations Registers: ALE_POL of the Local Bus Configuration Register.



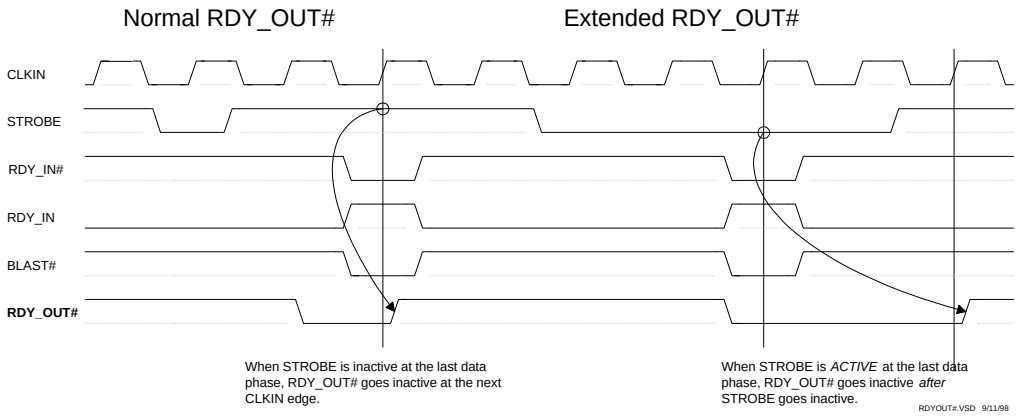
EDOUT -- Extended Data Out

The extended data out control defines when the AN3042 drives the DQ bus during a local bus read. The control is defined in the Operations Registers: EDOUT of the Local Bus Configuration Register. When EDOUT = '0', the AN3042 will drive the DQ bus during a read starting one clock after the address phase and stop driving at the clock edge where both of the ready inputs and BLAST# are active. When EDOUT = '1', the AN3042 will drive the DQ bus during a read starting one CLKIN clock after the address phase and stop driving one clock after the clock edge where the two ready inputs and BLAST# are active. The data is driven for one clock period after the signal that the transaction is over. This allows for applications that require additional hold time.



RDY_OUT# -- Ready Out

STROBE can be active or inactive during data phases. However, if STROBE is active during the data phase when BLAST# is active AND the extended ready out control (XTND_RDY_OUT) is set, the AN3042 keeps RDY_OUT# active until STROBE goes inactive. In the case of a read, the AN3042 will continue to drive the data on DQ until STROBE is de-asserted.



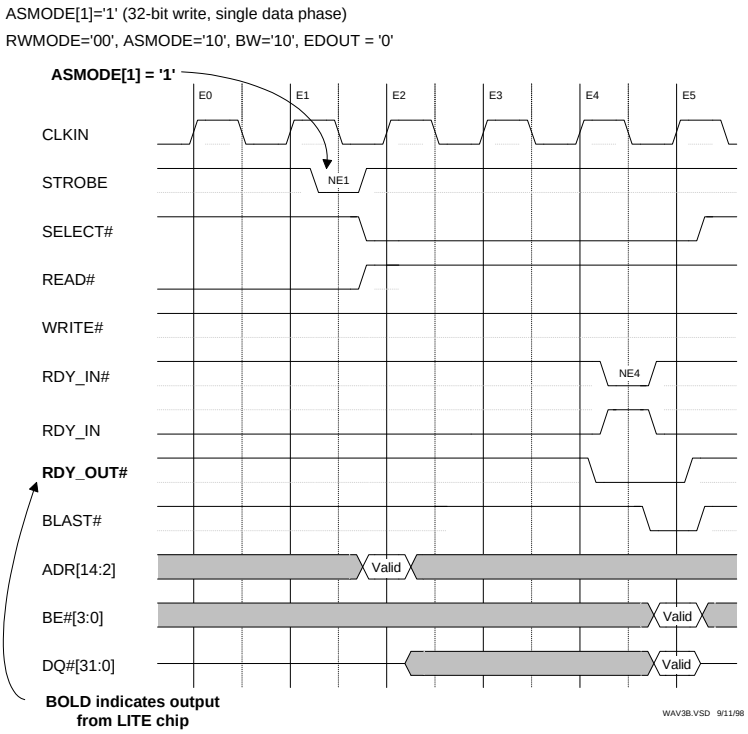
ASMODE -- Address Strobe Mode

The address strobe mode control defines the polarity and the timing used to sample the AN3042 address strobe input signal, STROBE, and the timing used to sample the ready in input signals, RDY_IN and RDY_IN#. The two bit control field is defined in the Operations Registers: ASMODE of the Local Bus Configuration Register.

ASMODE[0] defines the polarity of the STROBE input signal; '0' = active low and '1' = active high.

ASMODE[1] controls the sampling edge of the STROBE, RDY_IN, and RDY_IN# signals. Logic low indicates that the signals are sampled using the rising edge of CLKIN. A logic high indicates that the signals are sampled with the falling edge of CLKIN. Sampling on the falling edge should only be used when the required minimum setup time with respect to the clock rising edge cannot be met on the signals.

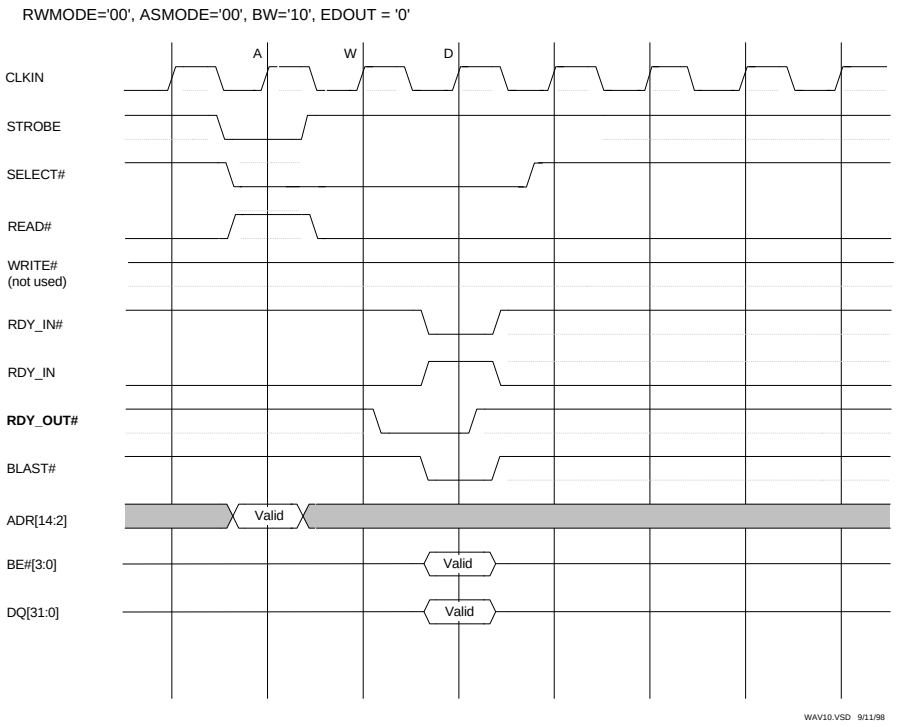
The following waveform illustrates the operation of the ASMODE[1] pin. ADR and READ# are sampled at E2, and a valid write occurs at E4. Note that STROBE is captured at the negative edge labeled NE1 and that the ADR and READ# signals are sampled at the positive clock edge labeled E2. Also note that the ready signals are sampled at the negative edge labeled NE4 and not at the positive edge labeled E5. STROBE is active low since ASMODE[0] = '0'.



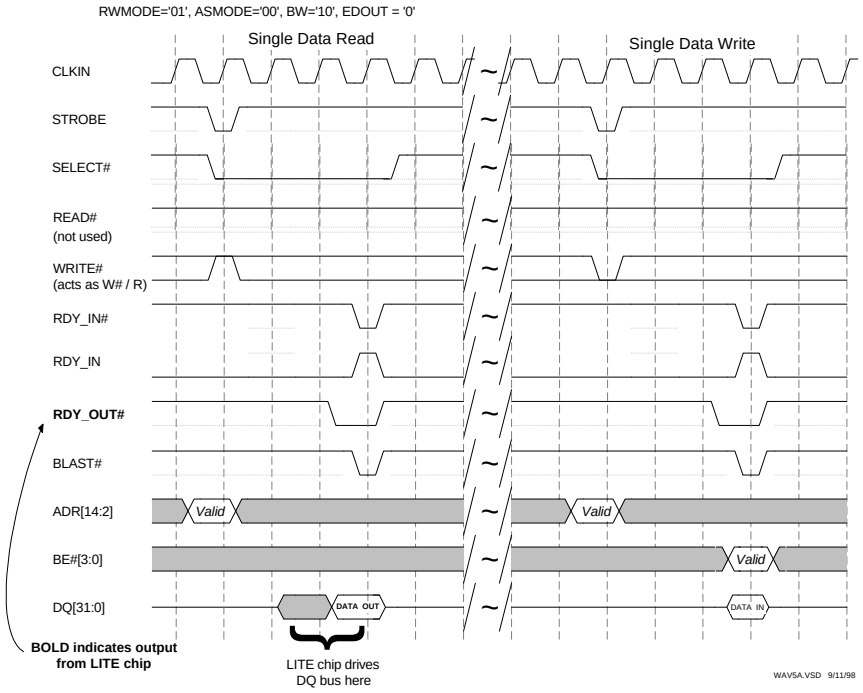
RWMODE -- Read Write Mode

The read write mode control defines how the address strobe (STROBE), read (READ#), and write (WRITE#) input signals are interpreted by the AN3042 internal logic. The two bit control field is defined in the Operations Registers: RWMODE of the Local Bus Configuration Register. Each of the four cases for RWMODE are illustrated in the following four diagrams.

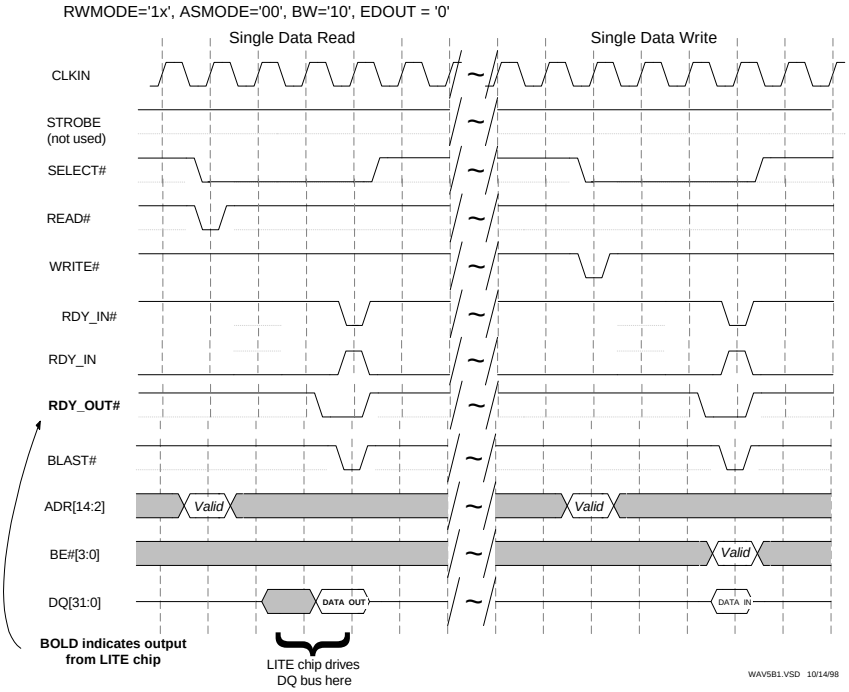
Use RWMODE = '00' to interface to a processor that has a read-write signal defined as W_R# (write is logic 1, read is logic 0). In this mode, the WRITE# is not used and should be tied high. A write cycle is illustrated below.



Use RWMODE = '01' to interface to a processor that has a read-write signal defined at R_W# (write is logic 0, read is logic 1). In this mode, the WRITE# acts as R_W# and it is sampled when SELECT# and STROBE are both active. The READ# pin is not used and should be tied high. This is illustrated below.



Use RWMODE = '10' or RWMODE = '11' to interface to a processor that has separate active low read and write signals. The two modes are identical. Sampling of the READ# and WRITE# signals is used as the internal address strobe in place of the STROBE signal.. This is illustrated below.



I²C Serial Port and Auto-Configuration

The AN3042 I²C serial port may master the I²C bus, but it is not a target on the bus. Read and write access to the port is available to both the PCI and Local buses via the I²C programming Operations Registers. The AN3042 supports single byte device internal addressing. The port can be used for Auto-Configuration of the AN3042 as well as for basic read and write access to I²C devices connected to the port.

Auto-Configuration is the function that uses the port to load AN3042 configuration information. A typical device containing the data is a serial Electrically Erasable Programmable Read Only Memory, (EEPROM). The EEPROM includes data for some PCI configuration registers and some Operations Registers. The EEPROM containing the AN3042 configuration data must be located at I²C device address 0x0 and must contain the proper AN3042 Signature. For details, see the memory map below and the accompanying field descriptions.

I²C Serial Port Device 0x0 Memory Map for Auto-Configuration				
Byte 3	**Byte 2**	**Byte 1**	**Byte 0**	**Internal Address, Byte Offset**
don't care	don't care	don't care	don't care	0x00 ... 0x3F
AN3042 Signature 0x48	**AN3042 Signature** 0x37	**AN3042 Signature** 0x48	**AN3042 Signature** 0x37	0x40
Device ID high byte	**Device ID** low byte	**Vendor ID** high byte	**Vendor ID** low byte	0x44
Class Code, base class high byte	**Class Code,** sub-class middle byte	**Class Code,** programming intf. low byte	**Revision ID**	0x48
Subsystem Device ID high byte	**Subsystem Device ID** low byte	**Subsystem Vendor ID** high byte	**Subsystem Vendor ID** low byte	0x4C
MAX_LAT	**MIN_GNT**	**Interrupt Pin, Master Enable (*)**	don't care	0x50
Cardbus CIS Pointer high byte	**Cardbus CIS Pointer** low byte	**Cardbus CIS Pointer** high byte	**Cardbus CIS Pointer** low byte	0x54
reserved	reserved	reserved	reserved	0x58
reserved	reserved	reserved	reserved	0x5C
reserved	reserved	reserved	reserved	0x60
reserved	reserved	reserved	reserved	0x64
reserved	reserved	reserved	reserved	0x68
reserved	reserved	**Local Bus Configuration** high byte	**Local Bus Configuration** low byte	0x6C
reserved	reserved	reserved	reserved	0x70
Host Control bits [31:24]	**Host Control** bits [23:16]	**Host Control** bits [15:8]	**Host Control** bits [7:0]	0x74
don't care	don't care	don't care	don't care	0xFF … 0x78

(*) = Master Enable is the most significant bit of this byte; see text for more description of this flag.

AN3042 Signature

Address - 0x43 - 0x40

Device Configuration Signature -- A valid EEPROM AN3042 configuration image is indicated at this address by the value of 0x48374837. It is read from the EEPROM at I^2C device address 0x0 immediately after the AN3042 comes out of reset. The AN3042 comes out of reset as indicated by the de-assertion of the AN3042 RST# input. Upon recognition of a valid signature, the contents of the EEPROM will be transferred to the appropriate AN3042 registers. The appropriate registers are indicated by the other labeled fields of the I^2C Serial Port Device 0x0 Memory Map for Auto-Configuration and are described in this section. If the value at this location is not 0x48374837, then the transfer will not occur and the default (reset) values for the AN3042 registers will remain in effect after the AN3042 comes out of reset.

Vendor ID

Address - 0x45 - 0x44

PCI Configuration Vendor ID -- the meaning of this field is described in the PCI Bus section.

Device ID

Address - 0x47 - 0x46

PCI Configuration Device ID -- the meaning of this field is described in the PCI Bus section.

Revision ID

Address - 0x48

PCI Configuration Revision ID -- the meaning of this field is described in the PCI Bus section.

Class Code

Address - 0x4B - 0x49

PCI Configuration Class Code (Base Class, Sub-Class, Programming Interface) -- the meaning of this field is described in the PCI Bus section.

Subsystem Vendor ID

Address - 0x4D - 0x4C

PCI Configuration Subsystem Vendor ID -- the meaning of this field is described in the PCI Bus section.

Subsystem Device ID

Address - 0x4F - 0x4E

PCI Configuration Subsystem Device ID -- the meaning of this field is described in the PCI Bus section.

Interrupt Pin

Address - 0x51, bits 2, 1, 0

PCI Configuration Interrupt Pin -- the meaning of this field is described in the PCI Bus section.

Master Enable

Address - 0x51, bit 7

PCI Configuration Command Bit 2 -- enable PCI bus master operation. For a host bridge, this typically must be set to allow the host to configure itself and configure and access other devices on the PCI bus. Even though an external master can manipulate the PCI Command register, it is typical that the host is the first device to configure devices on the PCI bus. Since the default value for PCI Command bit 2 is that PCI bus mastering is disabled, the Master Enable bit in the EEPROM image should be set to enable PCI mastering.

MIN_GNT

Address - 0x52

PCI Configuration MIN_GNT -- the meaning of this field is described in the PCI Bus section.

MAX_LAT

Address - 0x53

PCI Configuration MAX_LAT -- the meaning of this field is described in the PCI Bus section.

Cardbus CIS Pointer

Address - 0x57 - 0x54

PCI Configuration Cardbus CIS Pointer -- the meaning of this field is described in the PCI Bus section.

Local Bus Configuration

Address - 0x6C - 0x6D

Operations Registers Local Bus Configuration -- the detailed meaning of this field is described in the Operations Registers section. For the AN3042 Local bus to exhibit the correct protocol, the Local Bus Configuration Operations Register needs to be loaded before the AN3042 is accessed via the Local bus interface. The Local bus interface circuitry will be held in reset until transfer of the EEPROM configuration data is complete. At such completion, and dependent upon the state of the Host Control Operations Register, the Local bus will be available for access using the programmed Local bus interface protocol.

Host Control

Address - 0x77 - 0x74

Operations Registers Host Control -- Only bits 1 and 0 have meaning; the other bits are reserved. When programming bits 1 and 0, other bits of the DWORD should be written with '0'.

One of two reset controls from the AN3042 may be used to reset the local processor system. The AN3042 RSTOUT# output signal is a buffered copy of the PCI bus RST# signal and is not conditioned by the bits of the Host Control register. This signal will de-assert before the Auto-Configuration process completes, so some applications will not use this signal in order to prevent premature local processor attempts to access the AN3042.

The other form of reset control provides a direct link to the Auto-Configuration process. Using this method, the local processor will remain in reset until completion of the Auto-Configuration process. In this case, the AN3042 RSTOUTD# output signal, (or its active high version, RSTOUTD), is used to reset the local processor. This signal is a copy of bit 0 of the Host Control register, (the Local Processor Reset). With Auto-Configuration, the local processor will be either held in reset or released from reset depending upon the value in the EEPROM. Furthermore, as an Operations Register, the Host Control register may be accessed from the PCI bus once Auto-Configuration is complete. Therefore, if it is desired that the local processor be held in reset until updated by a command over the PCI bus, bit 0 of this field should be set.

Bit 1 of the Host Control register should be cleared in most cases. Setting it to '1' will reset the Operations Registers to their default state and thereby reinitialize the Local Bus Configuration register. This bit is typically used only for debug or maintenance operations. Another seldom used operation is setting the Host Control register from the local processor. Even though the Operations Register is available from the Local bus, setting either bit 0 or bit 1 to '1' will lock-out the local processor from accessing the AN3042 by way of the Local bus interface.

Operations Registers

These registers are the means by which AN3042 functions are accessed. Access is available via either interface, the PCI bus or the Local bus. The Operations Registers include the PCI Bus Mastering registers (DMA), the I_2O messaging unit registers, the interrupt registers, the mail boxes, and the direct access register. Also included in the Operations Registers are the initialization and configuration registers used to customize the AN3042 operation to the user's needs. The critical Host Control Register and Local Bus Configuration Register may be programmed during the system initialization process. Programming via the I^2C serial is available for this purpose.

The Operations Registers reside in the Local bus clock domain, therefore, a clock must be applied to CLKIN for proper operation of the AN3042. Either an external clock may be provided or one of the AN3042 PCLKOUT[2:0] signal outputs may be used. PCLKOUT is a copy of the PCI Clock input, CLK. The PCLKOUT signals are intended to be an option for the user to connect to other circuits, as well.

Also available to support other circuits, the user may connect any or all of the three reset outputs from the AN3042. RSTOUT# is a registered copy of the PCI Reset input, RST#. It is synchronous to CLKIN. The other two reset output signals, RSTOUTD# and RSTOUTD, are the copy of a bit in an Operations Register, the 'R' bit of the Host Control Register. RSTOUTD# and RSTOUTD are complements of each other and are synchronous to CLKIN. Upon power-up reset of the AN3042 (via the PCI Reset RST#), this bit will be set active. It may be cleared during the start-up process using the I^2C serial interface or it may be cleared or set via commands received over the PCI bus. So these signals may be used to hold a local processor in reset until AN3042 configuration is complete or when a host is ready to release the local processor to begin its operations.

Operations Registers Addresses

This is a summary table of the AN3042 Operations Registers. Register locations are the offset from the Base Address Register 0 and are DWORD aligned. The value shown is the address of the least significant byte of the register offset. Default, power-up values are also shown. Both numbers are documented in hexadecimal notation. Bit positions in gray are unused and read back as '0' unless otherwise indicated in the default value.

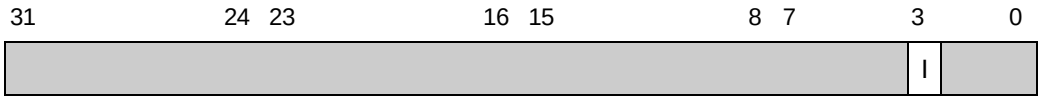
Operations Register				Offset / Mnemonic
31 24	23 16	15 8	7 0	Default Value
I_2O Host Interrupt Status Register				0x0030 I2OHISR
			I	0x00000000
I_2O Host Interrupt Mask Register				0x0034 I2OHIMR
			M	0xFFFFFFFF
I_2O Local Interrupt Status Register				0x0038 I2OLISR
			I	0x00000000
I_2O Local Interrupt Mask Register				0x003C I2OLIMR
			M	0xFFFFFFFF
I_2O FIFO Access	all default as empty FIFO, read as 0xFFFFFFFF			
Inbound Free FIFO (read only) and Inbound Post FIFO (write only)				0x0040 IBFPFIFO
Outbound Post FIFO (read only) and Outbound Free FIFO (write only)				0x0044 OBPFFIFO
Inbound Post FIFO (read only) and Inbound Free FIFO (write only)				0x0048 IBPFFIFO
Outbound Free FIFO (read only) and Outbound Post FIFO (write only)				0x004C OBFPFIFO
Direct Access				0x0460 DAHBASE
PCI Physical Base Address (4G byte, 8K byte blocks)		BE for Reads	PCI	0xXXXXXXXX
I^2C Serial Command Register (write only)				0x04A0 NVCMD
device address	memory address	write data	T R	n/a
I^2C Serial Read Data Register				0x04A4 NVREAD
data3	data 2	data1	data0	0xXXXXXXXX
I^2C Serial Status Register				0x04A8 NVSTAT
		ACK	D	0x000000XX
DMA Local Base Address Register				0x04B0 DMALBASE
		Local Base Address (16K byte)		0x0000XXXX
DMA Host Base Address Register				0x04B4 DMAHBASE
PCI Base Address (4G byte)				0xXXXXXXXX
DMA Burst Size Register				0x04B8 DMASIZE
		DMA Burst Size (16K byte)		0x0000XXXX
DMA Control Register				0x04BC DMACTL
		L P	PF W	0x0000000X
Host Control				0x04E0 HCTL
			S R	0x00000001
Host Interrupt Control/Status				0x04E4 HINT
IMASK			IT	0x00000000
Host to Local Data Mailbox				0x04E8 HLDATA
I		Byte 1	Byte 0	0x0000XXXX
Local Processor Interrupt Control/Status				0x04F4 LINT
IMASK			IT	0x00000000
Local to Host Data Mailbox				0x04F8 LHDATA
I		Byte 1	Byte 0	0x0000XXXX
Local Bus Configuration				0x04FC LBUSCFG
		Local Bus Configuration		0x00000B50

Operations Registers Descriptions

Detailed descriptions of the Operations Registers follow. Register locations are the offset from the Base Address Register 0 and are DWORD aligned. The value shown is the address of the least significant byte of the register offset. The offsets are documented in hexadecimal notation. Unused bits are grayed-out. Unused bits are read as '0' unless otherwise indicated.

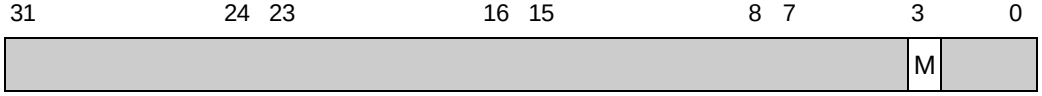
I_2O Registers

I_2O Host Interrupt Status Register - I2OHISR **0x0030**



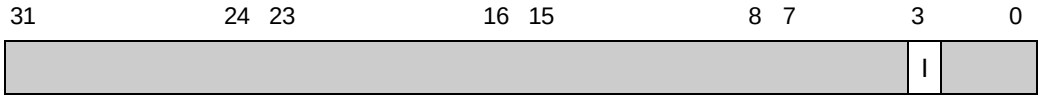
Bit	Description
3	Interrupt from the Outbound Post FIFO - the FIFO is not empty. Read only. '0' default.

I_2O Host Interrupt Mask Register - I2OHIMR **0x0034**



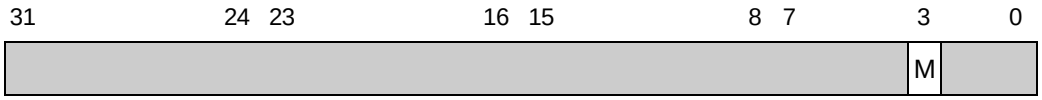
Bit	Description
3	Host Interrupt Mask Bit 1: interrupt is masked (default) 0: interrupt is not masked NOTE: unused bits in this register are read as 1's

I_2O Local Interrupt Status Register - I2OLISR **0x0038**



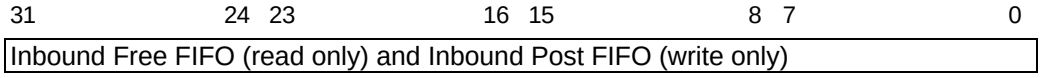
Bit	Description
3	Interrupt from the Inbound Post FIFO - the FIFO is not empty. Read only. '0' default.

I_2O Local Interrupt Mask Register - I2OLIMR **0x003C**



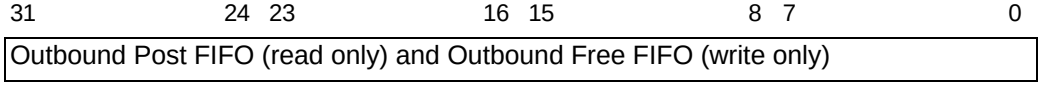
Bit	Description
3	Local Interrupt Mask Bit 1: interrupt is masked (default) 0: interrupt is not masked NOTE: unused bits in this register are read as 1's

I_2O Inbound Free / Post FIFO - IBFPFIFO **0x0040**



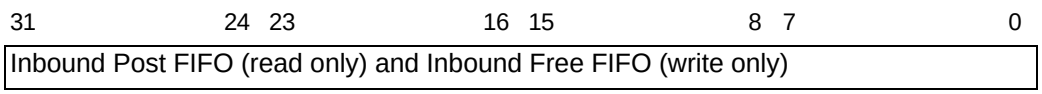
Bit	Description
31:0	A shared port -- Reading from this port returns data from the Inbound Free FIFO. The read of an empty FIFO returns 0xFFFF FFFF. Writing to this port places data into the Inbound Post FIFO. The FIFO is initially empty.

I_2O Outbound Post / Free FIFO - OBPFFIFO **0x0044**



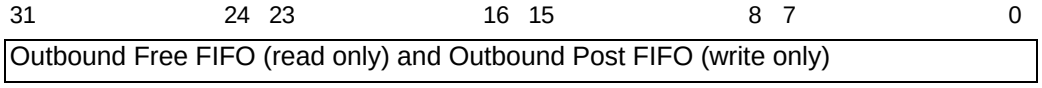
Bit	Description
31:0	A shared port -- Reading from this port returns data from the Outbound Post FIFO. The read of an empty FIFO returns 0xFFFF FFFF. Writing to this port places data into the Outbound Free FIFO. The FIFO is initially empty.

I_2O Inbound Post / Free FIFO - IBPFFIFO **0x0048**



Bit	Description
31:0	A shared port -- Reading from this port returns data from the Inbound Post FIFO. The read of an empty FIFO returns 0xFFFF FFFF. Writing to this port places data into the Inbound Free FIFO. The FIFO is initially empty.

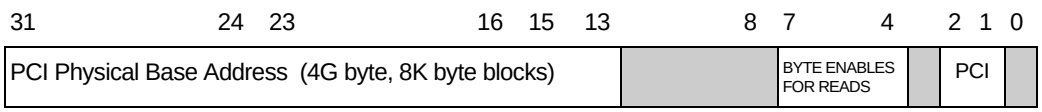
I_2O Outbound Free / Post FIFO ΘBFPFIFO **0x004C**



Bit	Description
31:0	A shared port -- Reading from this port returns data from the Outbound Free FIFO. The read of an empty FIFO returns 0xFFFF FFFF. Writing to this port places data into the Outbound Post FIFO. The FIFO is initially empty.

Direct Access Register

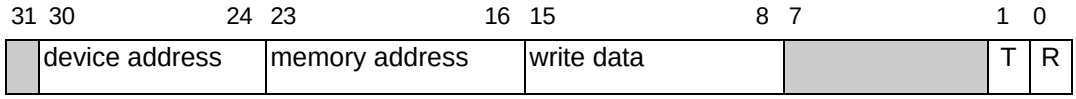
Direct Access Host Physical Base Address Register - DAHBASE **0x0460**



Bit	Description
31:13	PCI Physical Base Address for 8K byte access
7:4	Data Byte Enables for PCI Master Reads, C/BE#[3:0].
2:1	PCI cycle type for PCI Master Access 00 = interrupt acknowledge (read) (PCI command 0x0) or special cycle (write) (PCI command 0x1) 01 = I/O cycle (read or write) (PCI command 0x2 or 0x3) 10 = memory cycle (read or write) (PCI command 0x6 or 0x7) 11 = configuration cycle (read or write) (PCI command 0xA or 0xB)

I²C Serial Port Registers

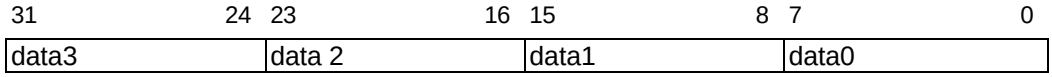
I²C Serial Command Register -- NVCMD (a write only register) 0x04A0



Bit	Description
30:24	**Device Address.** Device address of the I²C serial device. Default is 1010000.
23:16	**Memory Address.** Address within the I²C serial device.
15:8	**Write Data.** Write data. This data is ignored if the command is a read.
1	**Read Type.** This bit is ignored if the command is a write. The data read from a I²C serial device is accessible from the NVREAD register. 1 = 4 byte read 0 = single byte read
0	**Read / Write** 1 = read command 0 = write command Note: The write of this byte triggers the start of the EEPROM access. In an 8 or 16 bit system, this location must be written after the address and data have been written.

I²C Serial Read Data Register -- NVREAD 0x04A4

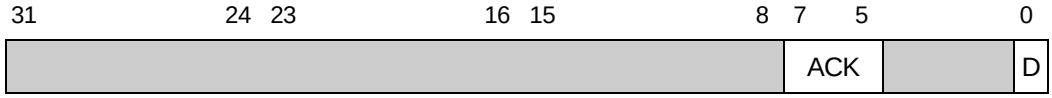
This register contains one or four bytes of data read from the I²C serial EEPROM.



Bit	Description
31:24	**Data3** Stores sequential read, byte 3. Undefined for single byte read.
23:16	**Data2** Stores sequential read, byte 2. Undefined for single byte read.
15:8	**Data1** Stores sequential read, byte 1. Undefined for single byte read.
7:0	**Data0** Stores single read and sequential read, byte 0.

I²C Serial Status Register - NVSTAT **0x04A8**

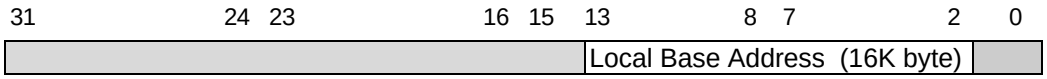
This register contains status information about the I²C serial data transfer.



Bit	Description
7:5	**Acknowledge** bit 7 = device address ack bit. 0 = ack, 1 = no ack. bit 6 = address ack bit. 0 = ack, 1 = no ack. bit 5 = second address ack bit. 0 = ack, 1 = no ack. In a successful read or write, these bits will be 000.
0	**Done Indicator** 1 = done 0 = in progress

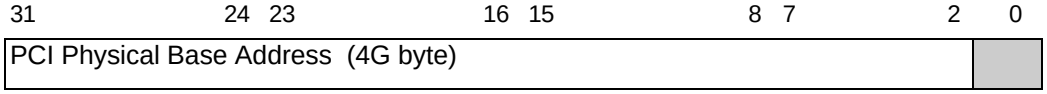
PCI Bus Mastering (DMA) Registers

DMA Local Base Address Register - DMALBASE **0x04B0**



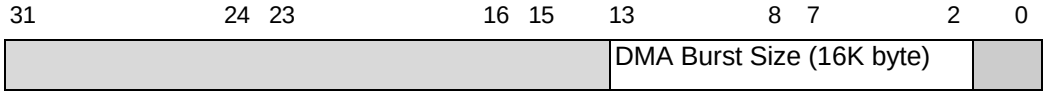
Bit	Description
13:2	Local Base Address - This is the first address of the DMA in the local memory. This register has DWORD resolution.

DMA Host Physical Base Address Register - DMAHBASE **0x04B4**



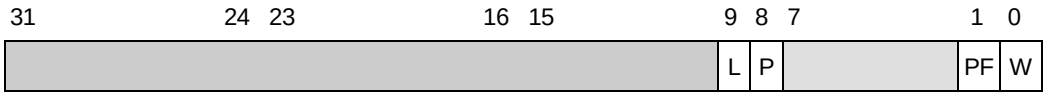
Bit	Description
31:2	PCI Physical Base Address - This is the first address of the DMA in the host's memory space. This register has DWORD resolution.

DMA Size Register - DMASIZE **0x04B8**



Bit	Description
13:2	Burst Size for any mastered DMA, read or write. This register has DWORD resolution.

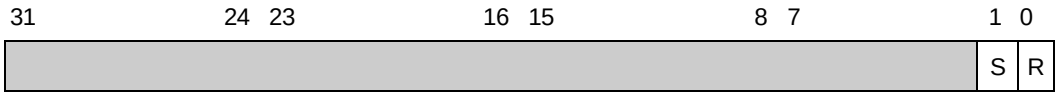
DMA Control Register - DMACTL **0x04BC**



Bit	Description
9	Local Ownership: A write to this bit by the local processor will toggle this bit if and only if the P bit is not set. This bit (along with the P bit) is intended to facilitate software arbitration of the DMA registers. '0' default.
8	PCI Ownership: A write to this bit by the PCI host processor will toggle this bit if and only if the L bit is not set. This bit (along with the L bit) is intended to facilitate software arbitration of the DMA registers. '0' default.
1	Pre-Fetch Inhibit for PCI memory reads: When this bit is set to one, the AN3042 PCI bus master engine will only use the PCI Read command (0x6). When this bit is zero (default), the AN3042 PCI bus master engine will use PCI commands Read (0x6), Read Line (0xC), and Read Multiple (0xE) as appropriate to optimize utilization of the PCI system bus(es).
0	Write: Determines the direction of the DMA and starts transfer. 1: DMA operation is a write to the host memory from the AN3042 shared memory. 0: DMA operation is a read from host memory into the AN3042 shared memory. A write to the low byte of this register triggers the DMA to occur. '0' default.

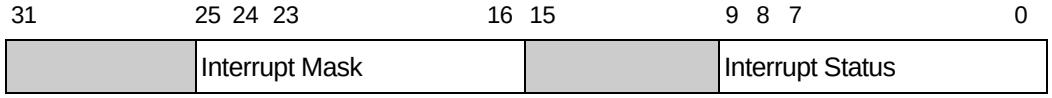
Host Control and Status Registers

Host Control Register - HCTL **0x04E0**



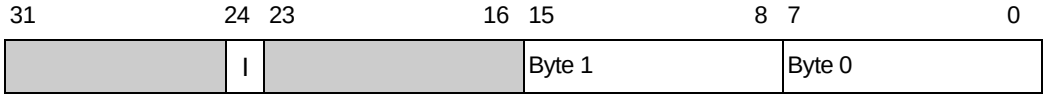
Bit	Description
1	**Soft Reset** – This bit controls the internal reset for the AN3042. 1 = reset active 0 = not reset (default)
0	**Local Processor Reset** – This bit controls the RSTOUTD# and RSTOUTD pins 1 = reset active (default state, RSTOUTD# pin is low, RSTOUTD pin is high) 0 = not reset (RSTOUTD# pin is high, RSTOUTD pin is low)

Host Interrupt Control and Status Register – HINT **0x04E4**



Bit	Description
25:16	**Interrupt Mask** 00 0000 0000 = no interrupts enabled (default) xx xxxx xxx1 = I_2O AI FIFO overflow interrupt enabled xx xxxx xx1x = I_2O PCI FIFO overflow interrupt enabled xx xxxx x1xx = reserved - always read as 0 xx xxxx 1xxx = Local to host, mailbox interrupt enabled xx xxx1 xxxx = Local to host, external signal interrupt enabled xx xx1x xxxx = DMA complete interrupt enabled xx x1xx xxxx = I_2O inbound post FIFO not empty interrupt enabled (read only at this address, compliment of I2OLIMR) xx 1xxx xxxx = I_2O outbound post FIFO not empty interrupt enabled (read only at this address, compliment of I2OHIMR) x1 xxxx xxxx = target abort interrupt enabled 1x xxxx xxxx = master abort interrupt enabled Note: All status bits are initially cleared.
9:0	**Interrupt Control/Status** 00 0000 0000 = no interrupt sources active xx xxxx xxx1 = I_2O AI FIFO overflow interrupt xx xxxx xx1x = I_2O PCI FIFO overflow interrupt xx xxxx x1xx = reserved - always read as 0 xx xxxx 1xxx = Local to host mailbox interrupt xx xxx1 xxxx = Local to host external signal interrupt xx xx1x xxxx = DMA complete xx x1xx xxxx = I_2O inbound post FIFO not empty interrupt (read only at this address, compliment of I2OLISR) xx 1xxx xxxx = I_2O outbound post FIFO not empty interrupt (read only at this address, compliment of I2OHISR) x1 xxxx xxxx = target abort interrupt 1x xxxx xxxx = master abort interrupt Note: When an interrupt is active, writing a 1 to that bit location will end the interrupt. All status bits are initially cleared.

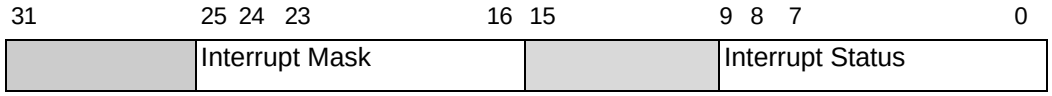
Host to Local Data Mailbox – HLDATA **0x04E8**



Bit	Description
24	**Interrupt to Local** This bit enables the host to send an interrupt to the Local. When it is set to 1 by the host, it triggers a mailbox interrupt to the local processor. The interrupt remains active until it is cleared by writing to the Local Interrupt Control Register. 0 = inactive 1 = active This bit is write only.
15:8 7:0	**Data byte** Two bytes of data that can be written by the host and read by the local processor.

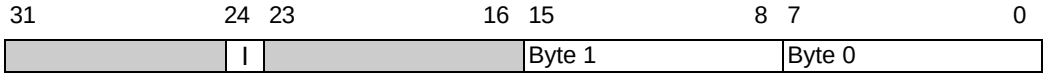
Local Control and Status Registers

Local Processor Interrupt Control Status Register - LINT **0x04F4**



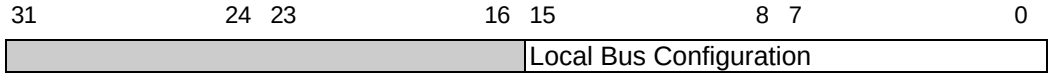
Bit	Description
25:16	**Interrupt Mask** 00 0000 0000 = no interrupts enabled (default) xx xxxx xxx1 = I_2O AI FIFO overflow interrupt enabled xx xxxx xx1x = I_2O PCI FIFO overflow interrupt enabled xx xxxx x1xx = reserved - always read as 0 xx xxxx 1xxx = Host to Local mailbox interrupt enabled xx xxx1 xxxx = reserved - always read as 0 xx xx1x xxxx = DMA complete xx x1xx xxxx = I_2O inbound post FIFO not empty interrupt enabled (read only at this address) xx 1xxx xxxx = I_2O outbound post FIFO not empty interrupt enabled (read only at this address) x1 xxxx xxxx = target abort interrupt enabled 1x xxxx xxxx = master abort interrupt enabled
9:0	**Interrupt Command/Status** 00 0000 0000 = no interrupt xx xxxx xxx1 = I_2O AI FIFO overflow interrupt xx xxxx xx1x = I_2O PCI FIFO overflow interrupt xx xxxx x1xx = reserved - always read as 0 xx xxxx 1xxx = Host to Local mailbox interrupt xx xxx1 xxxx = reserved - always read as 0 xx xx1x xxxx = DMA operation complete xx x1xx xxxx = I_2O inbound post FIFO not empty interrupt (mirror of I2OLISR[3] - read only at this address) xx 1xxx xxxx = I_2O outbound post FIFO not empty interrupt (mirror of I2OHISR[3] - read only at this address) x1 xxxx xxxx = target abort interrupt 1x xxxx xxxx = master abort interrupt Note: When an interrupt is active, writing a 1 to that bit location will end the interrupt.

Local to Host Data Mailbox - LHDATA **0x04F8**



Bit	Description
24	**Interrupt to Host** When this bit is written to 1 by the local processor, it causes a mailbox interrupt to the host. The interrupt will remain active until it is cleared by the host in the host interrupt register. 0 = inactive 1 = active This bit is write only.
15:8 7:0	**Data bytes** Two bytes of data written by the host and read by the local processor.

Local Bus Configuration Register - LBUSCFG **0x04FC**



Bit	Description
15	**XTND_RDY_OUT:** Defines the RDY_OUT# output signal relation to the final data phase. 0 = Normal. RDY_OUT# goes inactive after the final data phase (default) 1 = Extended Ready Out. RDY_OUT# remains active after the final data phase until the internal address strobe (typically STROBE) goes inactive. (see fields RWMODE and ASMODE for defining characteristics of the internal address strobe)
14	**BURST_STYLE:** Defines the data ordering protocol of bursts on the local bus. 0 = normal linear bursts (default) 1 = 486 style burst (byte ordering in a burst of DWORD -- 048C; 40C8; 8C04; C840)
13	**INT_POL:** Defines the polarity of the IRQ_OUT# output signal. 0 = Active Low interrupt to the local processor (default) 1 = Active High interrupt to the local processor
12	**BLAST_POL:** Defines the polarity of the BLAST# input signal. 0 = Active Low (default) 1 = Active High
11	**ALE_POL:** Defines the polarity of the ALE input signal. 0 = Active Low 1 = Active High (default)
10	**RDYOUT_POL:** Defines the polarity of the RDY_OUT# output signal. 0 = Active Low (default) 1 = Active High
9:8	**BW:** Defines the bus width of the local processor. 00 = 8 bit 01 = 16 bit 10 = 32 bit 11 = 32 bit with encoded byte enables (Motorola Mode) (default)
7	**BLASTMODE:** Determines the function of the BLAST# input signal. 0 = BLAST# is active only during the last transaction of the burst (default) 1 = BLAST# is active throughout the entire burst, and goes inactive with RDY_IN# and RDY_IN on the last read or write of the burst
6	**BEMODE:** Determines the byte enable encoding for 16 and 32 bit Motorola modes. 0 = normal byte enables; 1 = Motorola byte enable encoding. (default)
5:4	**RWMODE:** Defines how the READ#, WRITE#, and address STROBE input signals are interpreted internally and defines the internal address strobe.

Lite Pin Name	RWMODE 00	RWMODE 01	RWMODE 10	RWMODE 11
READ#	W_R#	Not Used	READ# data; used as internal address strobe	READ# data; used as internal address strobe
WRITE#	Not Used	R_W#	WRITE# data; used as internal address strobe	WRITE# data; used as internal address strobe
STROBE	Used as internal address strobe	Used as internal address strobe	Not used as internal address strobe	Not used as internal address strobe

3:2	**ASMODE:** Defines the polarity of STROBE input signal and the timing used to sample the ready input signals and the internal address strobe. (see field RWMODE for a defining characteristic of the internal address strobe) x0 = STROBE is active low (default) x1 = STROBE is active high 0x = Internal address strobe and RDY_IN# and RDY_IN are sampled on the rising edge (default) 1x = Internal address strobe and RDY_IN# and RDY_IN are sampled on the falling edge
1	**EDIN:** Defines protocol for validated input data. 0 = input data is valid during the current cycle when rdyin and rdyout are both active (default) 1 = input data is valid one cycle later
0	**EDOUT:** Defines protocol for validated output data. 0 = output data is valid during current cycle when rdyin and rdyout are both active (default) 1 = output data is valid one cycle later

Performance Characteristics

Absolute Maximum Ratings

Storage Temperature	-55 to +125 degrees C.
Voltage on any pin referenced to V_{SS}	-0.5 V to +7.0 V

Recommended Operating Environment

Ambient Operating Temperature	0 to 70 degrees C.
Power Dissipation, Estimated Maximum Operating	1.1 Watts

Recommended Operating DC Parameters -- Local Bus and Other non-PCI Signals

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{DD}	Supply Voltage	V_{SS} = 0.0V	3.0	3.6	V	
V_{IH}	Input High Voltage	V_{SS} = 0.0V	$0.7V_{DD}$	5.25	V	
V_{IL}	Input Low Voltage	V_{SS} = 0.0V	-0.5	$0.3V_{DD}$	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DD}$		+/-10	uA	
V_{OH}	Output High Voltage	I_{OUT} = -0.8mA	$0.9V_{DD}$		V	1
V_{OL}	Output Low Voltage	I_{OUT} = 0.8 mA		$0.1+V_{SS}$	V	2
C_{IN}	Input Pin Capacitance			10	pF	
C_{CLK}	CLK Pin Capacitance		5	12	pF	
C_{IDSEL}	IDSEL Input Pin Capacitance			8	pF	
L_{PIN}	Pin Inductance			20	nH	

NOTES:

1) Except INTA# and IRQ_OUT# which are open drain.

2) 1.5 mA drivers are used for AD[31:2], C/BE#[3:0], and PAR, FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, and INTA#. 4 mA drivers are used for DQ[31:0], RDY_OUT#, IRQ_OUT#, PCLKOUT[2:0], RSTOUT#, RSTOUTD, and RSTOUTD#. And, 2 mA drivers are used for SCL and SDA.

Recommended Operating DC Parameters -- PCI Bus Signals

The AN3042 is compatible with the PCI requirements for 3.3V and 5V signaling. Refer to the PCI Local Bus Specification, Revision 2.1 for details. Reference URL: http://www.pcisig.com/

Timing Parameters -- Local Bus Signals

The parameters for the local bus are specified here.

Symbol	Parameter	Min	Max	Units	Notes
t_{LOCAL}	CLKIN Cycle Time (Local clock)	20		ns	1
t_{high}	CLKIN High Time	40	60	%	2
t_{low}	CLKIN Low Time	40	60	%	2
t_{su}	Input Set up Time to CLKIN	8		ns	3
t_{hold}	Input Hold Time to CLKIN	3		ns	
t_{out}	CLKIN to Output valid	2	10	ns	4
$t_{on\text{-}da}$	DQ[31:0] Float to Active Delay from CLKIN	2	14	ns	
$t_{out\text{-}da}$	DQ[31:0] Output Delay from CLKIN	2	10	ns	
$t_{off\text{-}da}$	DQ[31:0] Active to Float Delay from CLKIN	2	14	ns	
$t_{su\text{-}adr}$	ADR[14:2] Input Setup Time to CLKIN	6			
$t_{h\text{-}adr}$	ADR[14:2] Input Hold Time from CLKIN	3		ns	
$t_{su\text{-}ale}$	ADR[14:2] Input Setup Time to ALE	1			
$t_{h\text{-}ale}$	ADR[14:2] Input Hold Time from ALE	3		ns	
$t_{min\text{-}ale}$	Minimum Active Pulse width for ALE	5		ns	5

NOTES:

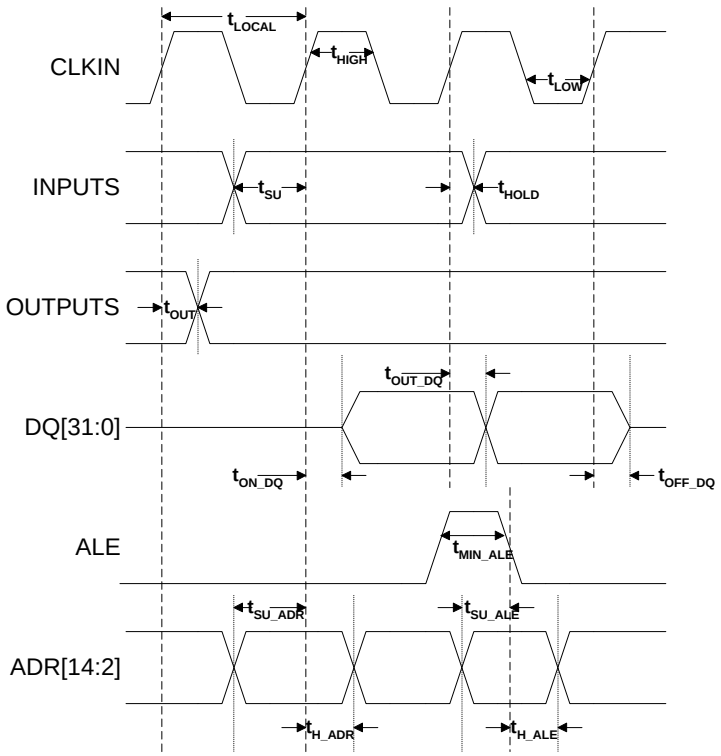
1) V_{TEST} = 1.5 V.

2) Voltage threshold for high is 2.0 V; Voltage threshold for low is 0.8 V.

3) Inputs are STROBE, SELECT#, READ#, WRITE#, RDY_IN, RDY_IN#, BE#[3:0], DQ[31:0], BLAST, and IRQ_IN#.

4) C_L = 50 pF. Outputs are RDY_OUT#, IRQ_OUT#, RSTOUTD, and RSTOUTD#.

5) Voltage threshold for high is 2.0 V.



Timing Parameters -- I²C Serial Port Bus Signals

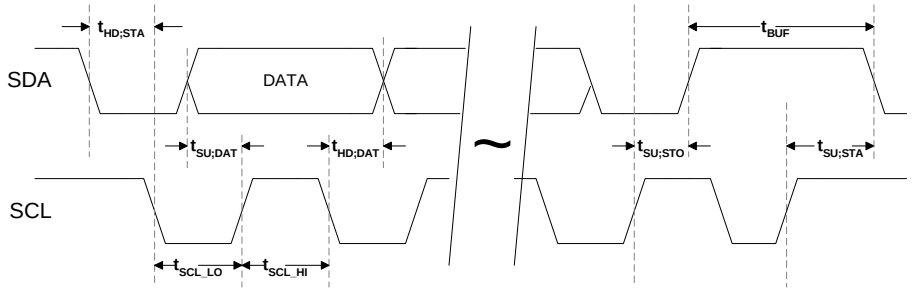
The I²C serial interface is designed for a 100Kbit/s transfer rate. The interface clock is referenced to the local clock, CLKIN. The table below gives the parameters of the AN3042's I²C serial interface with respect to the number of local clock periods and the equivalent number of microseconds if the clock is run at 50 MHz. The 100Kbit/s rate is accomplished with a CLKIN rate of 50 MHz. For CLKIN rates other than 50 MHz, use the Minimum Clocks column to calculate the Minimum Time for each parameter.

Symbol	Parameter	Minimum Clocks (Clock Periods)	Minimum Time (microseconds)	Notes
t_{SCL_LO}	Low Period of SCL	250	5.00	
t_{SCL_HI}	High Period of SCL	250	5.00	
t_{BUF}	Bus Free time between 'Start' & 'Stop'	500	10.00	1, 2
$t_{SU;STA}$	Set up time for repeated 'Start'	250	5.00	1
$t_{HD;STA}$	Hold time for 'Start'	250	5.00	
$t_{SU;DAT}$	Set up time for Data	125	2.50	
$t_{HD;DAT}$	Hold time for Data	125	5.00	
$t_{SU;STO}$	Set up time for 'Stop'	250	5.00	2

NOTES:

1) 'Start' condition is a high-to-low transition on SDA while SCL is high.

2) 'Stop' condition is a low-to-high transition on SDA while SCL is high.



Timing Parameters -- PCI Bus Signals and AN3042 Derived Signals

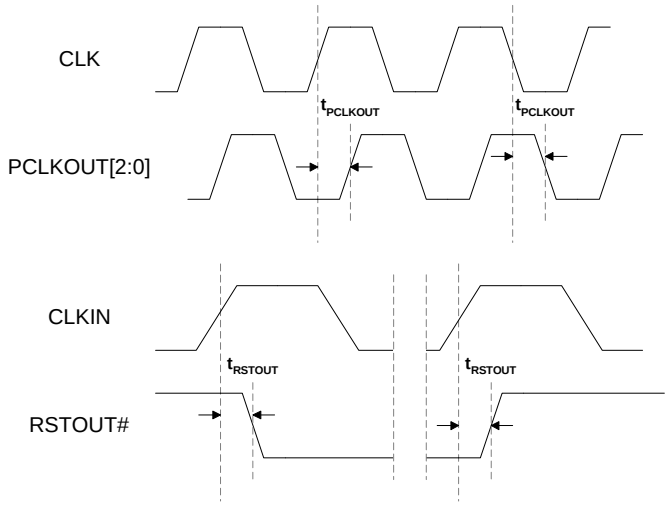
The AN3042 is fully compatible with the PCI requirements for 3.3V and 5V signaling. Refer to the PCI Local Bus Specification, Revision 2.1 for details. Reference URL: http://www.pcisig.com/

The AN3042 provides copies of the PCI clock input, CLK, on the PCLKOUT[2:0] pins. The system level function and timing of these outputs are the same as those of the CLK input. The AN3042 also provides a registered copy of the PCI reset input, RST#, on the RSTOUT# pin. The PCI reset is synchronized to the Local bus clock, CLKIN. RSTOUT# will follow RST# by no more than two CLKIN cycles. The detailed timing characteristics of the PCLKOUT[2:0] and RSTOUT# signal outputs is shown below.

Symbol	Parameter	Min	Max	Units	Notes
$t_{pclkout}$	PCLKOUT delay from CLK	2	10	ns	1
t_{rstout}	CLKIN to RSTOUT# valid	2	10	ns	1

NOTES:

1) 50 pF load.



AN3042 Operations

Local Bus Configurations

The AN3042 interfaces to several processor families. Suggested local bus configurations for some processors are indicated here. The 16-bit Local Bus Configuration Operations register, LBUSCFG, can be written via the I^2C serial interface upon chip initialization to prepare the AN3042 local bus for the proper interface protocol.

Processor	LBUSCFG value
Motorola Power QUICC MPC860	0x0B50 (default)
Motorola QUICC 68360	0x8B18
Motorola 68040	0x0B50 (default)
Intel i960	0x0A00
Intel i486	0x6A00
Intel 80186	0x2D21
Texas Instruments TMS320C30	0x0A91

PCI Bus Mastering

Burst transfers between the AN3042 16KB shared memory and the PCI bus system are performed by the direct memory access (DMA) controller. Setup for the DMA controller is accomplished by programming the Operations Registers of the AN3042 from either the PCI bus interface or the Local bus interface. An indication of a completed DMA is available by polling an Operations register or servicing an interrupt. Ownership of the DMA controller by either the PCI or Local bus interfaces is arbitrated by software using the Operations Registers.

The address and transfer size registers operate with DWORD resolution. The lower two bits of each of the address and transfer size fields are ignored. Transfers over the PCI bus are DWORD so all four byte enables of the bus are active when transferring data mastered by the AN3042. The full 32-bit PCI address space is supported by the DMA controller. The direction of transfer is determined by the 'W' bit in the DMA Control Register. 'W' is the "Write" bit and is with respect to the AN3042 "writing" to the PCI bus. The basic sequence to setup a DMA is as follows:

1) Enable the Interrupt Mask for the desired interface if an interrupt on DMA completion is required. e.g., LINT[21] = 1 will enable the interrupt onto the IRQ_OUT# pin.

2) Load the address for the beginning of the transfer block of AN3042 shared memory. This is the DMA Local Base Address Register, DMALBASE.

3) Load the address for the beginning of the transfer block of PCI bus space. This is the DMA Host Base Address Register, DMAHBASE.

4) Load the size of the transfer block. This is the DMA Size Register, DMASIZE.

5) To initiate the DMA, a write to the least significant byte of the DMA Control Register, DMACTL, will start the controller. Writing a '1' to bit 0 will transfer data from the AN3042 shared memory, (pointed to by DMALBASE), to the PCI bus space, (pointed to by DMAHBASE). This causes

write bursts on the PCI bus. Writing a '0' to bit 0 will transfer the other direction and cause read bursts on the PCI bus. The AN3042 bus mastering logic will use the most efficient PCI command available for all of its bursts during the transfer.

6) When the DMA is complete, LINT[5] will be set. If interrupts are enabled for DMA completions, then an interrupt will be generated. If not, LINT[5] can be polled.

An additional option of a PCI bus mastered read transfer involves setting the option to perform non-prefetchable PCI reads during transfers into AN3042 shared memory. This option is set in the DMA Control Register with the PF flag. Also, ownership of the controller can be arbitrated in software with assistance of the L and P bits in the DMA Control Register; these are the Local Bus Ownership and PCI Bus Ownership flags, respectively. See the section AN3042 Operations Registers for details.

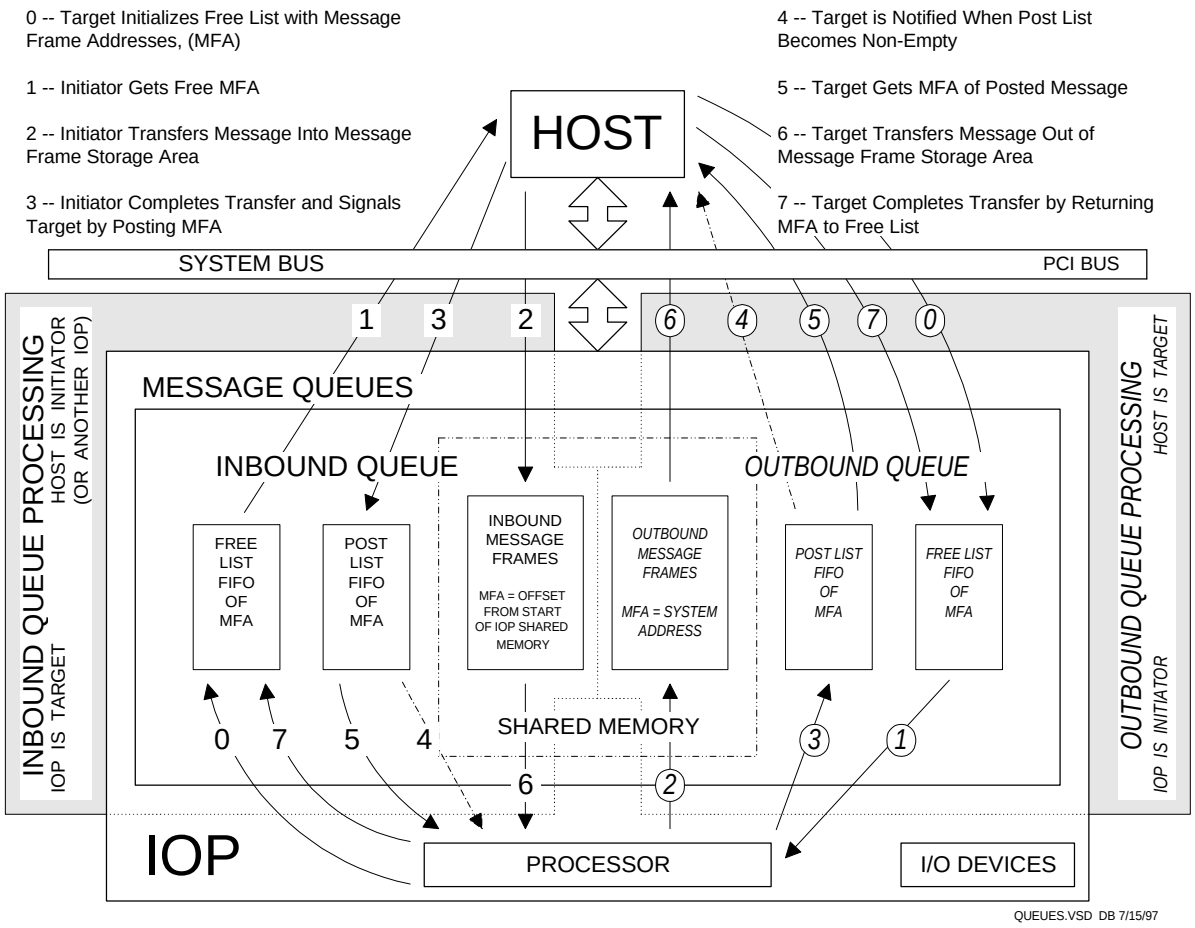
I_2O Message Unit

The I_2O Specification describes a messaging unit consisting of four FIFO, a shared memory to store message frames, and an interrupt function. The structure of this unit is described in the I_2O Architecture Specification, version 1.5 on pages 4-2 through 4-7. This capability is fully integrated within the AN3042. Reference URL: http://www.i2osig.org/

There is no need for external circuitry to manage the FIFO operations. If I_2O functionality is not desired, then the FIFO are available for general purpose use. Each of the four FIFO are 32 DWORD deep, are accessible from both the PCI and Local bus interfaces, and can generate interrupts to both bus interfaces.

The unit operates in two clock domains, that of the PCI bus and that of the Local bus. I_2O message frames for transfer between the PCI and the Local domains are located within the 16K byte AN3042 Shared Memory, which is a general purpose dual port memory. There is no restriction upon where in the 16K byte space that the message frames reside, however, to satisfy I_2O requirements, the message frames must begin at DWORD boundaries. Neither bus's access is dependent upon the operational state of the other bus. This is governed by the nature of the AN3042 Shared Memory. Operations of the I_2O FIFO and the I_2O Interrupt functions occur completely within the clock domain of the Local bus, however access is available to both the PCI and Local bus interafaces.

From a system perspective, the following diagram illustrates the I_2O Message Unit transfer function supported by the AN3042. The AN3042 is represented by the "Message Queues" block of the diagram and consists of both Inbound and Outbound Queues and the Shared Memory. For more description of the terminology used in the diagram, refer to the I_2O Architecture Specification. Reference URL: http://www.i2osig.org/



Direct Access

Direct Access allows the local processor to access the PCI bus directly, bypassing the shared memory. In this mode the local processor can generate the following PCI bus master cycles:

- Configuration Read C/BE#[3:0] = 0xA
- Configuration Write C/BE#[3:0] = 0xB
- I/O Read C/BE#[3:0] = 0x2
- I/O Write C/BE#[3:0] = 0x3
- Memory Read C/BE#[3:0] = 0x6
- Memory Write C/BE#[3:0] = 0x7
- Special Cycle C/BE#[3:0] = 0x1
- Interrupt Acknowledge C/BE#[3:0] = 0x0

To operate in this mode, the local processor programs the Direct Access register. Programming sets the base address for the PCI master access and the type of PCI command to be generated. Then the local processor writes to the Direct Access space of the AN3042 Memory Map. Offsets into the Direct Access region of the

memory map are added to the PCI base address of the Direct Access register and become the address for the PCI bus master access. The type of PCI command generated is defined in the Direct Access register. A local bus read to the Direct Access area of the memory map becomes a PCI bus master read. Likewise, a local bus write to the memory map becomes a PCI bus master write.

Host Bridge

The AN3042 can be used as a host bridge. The processor on the AN3042 Local bus is therefore the host processor in the system. A host processor configures the other PCI devices on the PCI bus. The AN3042 provides the I^2C Serial Port and Auto-Configuration mechanism to setup for host bridge operations. Most aspects of Auto-Configuration apply to non-host use of the AN3042, as well.

The AN3042 must master cycles onto the PCI bus to be a host bridge. The Master Enable bit located in the PCI configuration space is the means to enable AN3042 PCI mastering. Since the AN3042's default value for the Master Enable bit is de-asserted, it is necessary to use the AN3042 Auto-Configuration mechanism to enable PCI mastering. During the power-up reset sequence, the I^2C serial interface loads data from a non-volatile memory, (typically a serial EEPROM), to set the Master Enable bit in the PCI configuration space. Some, but not all, of the PCI configuration values are loaded using this mechanism. These values can be read by other devices in the system to identify the host bridge, (e.g., Device ID, Vendor ID, Class Code, etc).

Another part of the Auto-Configuration mechanism is to setup the Local bus interface with the host processor and, optionally, provide reset control to the host processor. The Local Bus Configuration register is loaded from the serial EEPROM image. This will set the protocol of the Local interface. The Host Control register is loaded by the Auto-Configuration mechanism and can control reset to the host processor. Utilization of the AN3042 RSTOUTD# output signal, (or its complement, RSTOUTD), is how the AN3042 can control host processor reset. The Host Control register image is stored in the serial EEPROM and indicates if the reset will remain asserted or will release after Auto-Configuration is complete. Normally, it should release the host from reset. If it is not released, then an external PCI master will be required to release the host processor.

Finally, the AN3042 uses the Direct Access function to configure PCI devices on the PCI bus. The first device that it configures is typically itself. It is important that the Master Enable bit is set. Without this bit asserted, the AN3042 cannot configuration itself (or any other devices) via the PCI bus.

Dual Port Shared Memory

In order to perform concurrent target access to shared memory from the PCI and Local bus interfaces it is generally necessary to devise a handshake protocol and/or address access allocation scheme to prevent corrupting memory locations. That is, a location within the AN3042 dual port memory may be corrupted if a read from one interface occurs simultaneously with a write from the other interface to that same location. The AN3042 assists the user in managing concurrent access to the shared memory.

The AN3042 PCI and Local bus are high performance interfaces. Internal logic performs read pre-fetching in order to maintain a full speed, zero wait-state, burst access to the shared memory. For managing memory access, the AN3042 performs a disconnect or wait for target reads at each 64-byte boundary. If a user is allocating sections of memory to PCI and Local space and intends to execute simultaneous access to the shared memory from both interfaces, then this 64-byte boundary can be used to place PCI and Local sections of memory adjacent to each other. In other words, the AN3042 has special logic that detects incoming burst addresses and will initiate the disconnect or wait at each 64-byte boundary. In this way, if the transaction is to end at the boundary, then no further pre-fetching occurs since time has been given to the master to end the bus transaction. For the PCI bus, this is performed by a target disconnect. For the Local bus, this is wait states.