SL811HS/T

USB Host/Slave Controllers

Hardware Specification

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CONVENTIONS **6**

DEFINITIONS **6**

REFERENCES **7**

REVISION HISTORY **7**

1 INTRODUCTION **8**

1.1 BLOCK DIAGRAM 8
1.2 SL811HS/SL811HST HOST OR SLAVE MODE SELECTION [MASTER/SLAVE MODE] 8
1.3 DATA PORT, MICROPROCESSOR INTERFACE. 9
1.4 INTERRUPT CONTROLLER 10
1.5 BUFFER MEMORY 10
1.6 PLL CLOCK GENERATOR 11
1.6.1 Typical Crystal requirements *12*
12 MHz Crystals: *13*
48 MHz Crystals: *13*
1.7 USB TRANSCEIVER 13

2 SL811HS/SL811HST REGISTERS **14**

2.1 USB CONTROL REGISTERS 15
SL811HS/SL811HST CONTROL REGISTER MAP 16
2.1.1 USB-A/USB-B Host Control Register [00H, 08H] *17*
2.1.2 Example of SL11H/SL11HT USB Packet Transfer: *18*
2.1.3 Example – SL11H USB Transaction to Transfer 128-bytes of Data to a Peripheral: *18*
2.1.4 Example of SL811HS/SL811HST USB packet transfer *19*
2.1.5 SOF Packet Generation *19*
2.1.6 USB-A/USB-B Host Base Address [01H, 09H] *19*
USB-A/USB-B Host Base Length [02H, 0AH] *19*
2.2 SL811HS/SL811HST CONTROL REGISTERS 21
2.2.1 Control Register 1, Address [05H] *22*
2.2.2 J-K Programming states, [bit 3 and 4 of Control Register 05H] *22*
2.2.3 Low Speed/Full Speed modes. [bit 5 and bit 6 of Control Register 05H] *23*
2.2.4 Low Power modes [bit 6 Control Register 05H] *23*
2.2.5 Interrupt Enable Register, Address [06H] *23*
2.2.6 USB Address Register, Reserved, Address [07H] *25*
2.2.7 Interrupt Status Register, Address [0DH] *25*
2.2.8 Current Data Set Register/Hardware Revision/SOF Counter Low, Address [0EH] *26*
2.2.9 SOF Counter High/Control2 Register, Address [0FH, READ/WRITE] *26*
Master/Slave SL811HS selection mode, Read Register 0FH *27*

3 SL811HS / SL811HST PHYSICAL CONNECTION **29**

3.1 28-PIN PLCC MECHANICAL DIMENSIONS 30
3.2 SL811HS USB HOST CONTROLLER PINS DESCRIPTION 30

3.3 PACKAGE MARKINGS (SL811HS) 32
3.4 SL811HST PIN LAYOUT 34
3.5 MECHANICAL DIMENSIONS 48 PIN LQPFP 35
3.6 SL811HST PIN ASSIGNMENTS AND DEFINITIONS 35
3.7 PACKAGE MARKINGS (SL811HST) 37

4 ELECTRICAL SPECIFICATIONS 38

ABSOLUTE MAXIMUM RATINGS 38
4.1 EXTERNAL CLOCK INPUT CHARACTERISTICS (X1) 40
4.2 DC CHARACTERISTICS 40
4.3 USB HOST TRANSCEIVER CHARACTERISTICS 42
4.4 BUS INTERFACE TIMING REQUIREMENTS 43
I/O Write Cycle 43
4.5 I/O READ CYCLE 45
4.6 SL811S DMA WRITE CYCLE (SL811 SLAVE MODE ONLY) 46
4.7 SL811S DMA READ CYCLE (SL811 SLAVE MODE ONLY) 47
4.8 RESET TIMING 48
Clock Timing Specifications 48

Figure 1: Full-Speed 48 MHz Crystal Circuit 11
Figure 2: optional 12 Mhz Crystal Circuit 12
Figure 3: SL811HS USB Host/Slave Controller - Pin layout 29
Figure 4: SL811HST USB Host/Slave Controller Pin Layout 34

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CONVENTIONS

1,2,3,4	Numbers without annotations are decimals
Dh, 1Fh, 39h	Hexadecimal numbers are followed by an "h"
0101b, 010101b	Binary numbers are followed by a "b"
bRequest, n	Word in *italics* indicate terms defined by USB Specification or by this Specification

DEFINITIONS

USB	**U**niversal **S**erial **B**us
SL811HS/T	The SL811HS is a Cypress USB Host/Slave Controller, providing multiple functions on a single chip. The SL811HS is available in a 28-Pin PLCC package, and the SL811HST is available in a 48-Pin LPQFP package. **Note:** This chip does not include CPU.
SL11	The SL11 is a Cypress **USB** Peripheral Device Controller, providing multiple functions on a single chip. The SL11 is available in a 28-Pin PLCC Package. **Note:** This chip does not include a CPU.
SL11T	The SL11T is a Cypress **USB** Peripheral Device Controller, providing multiple functions on a single chip. The SL11T is available in a 48-Pin LPQFP Package. **Note:** This chip does not include CPU.
LSB	**L**east **S**ignificant **B**it
MSB	**M**ost **S**ignificant **B**it
R/W	**R**ead/**W**rite
PLL	**P**hase **L**ock **L**oop
RAM	**R**andom **A**ccess **M**emory
SIE	**S**erial **I**nterface **E**ngine

ACK	Handshake packet indicates a positive acknowledgment.
NAK	Handshake packet indicating a negative acknowledgment
USBD	**U**niversal **S**erial **B**us **D**river
SOF	Start of Frame is the first transaction in each frame. It allows endpoints to identify the start of the frame and synchronize internal endpoint clocks to the host.
CRC	Cyclic Redundancy Check
HOST	The host computer system where the USB Host Controller is installed

REFERENCES

[Ref 1] USB Specification 1.1: http://www.usb.org

REVISION HISTORY

Name and Version	Date Issue	Comments
First Draft	02/05/00	Preliminary spec.
Revise	04/12/00	Update to match with HW
Revise for release	06/21/00	Edits for first time product release.
Released	07/31/00	Final Edits
Revise	08/03/00	Added DMA timing diagrams for SL811S.
Revise	09/19/00	Fixed timing parameters
Revise	09/27/00	Fixed pin 40 and 41 signal definition
Revise	11/08/00	Added Typical Requirements for Crystals, page 12
Revision	01/05/01	Corrected I/O Write and Read timing values.
Revised	03/20/01	Clarified Power Consumption.
Rev. 1.3	05/11/01	Rev. Sync., correct twasu
Rev. 1.31	05/24/01	Changed logo, formatted text and index
Rev. 1.32	05/25/01	Added Package Markings
Rev. 1.33	05/29/01	Changed table
Rev. 1.34	05/30/01	Changed font and format
Rev. 1.35	06/01/01	"Cleaned up" format

1 INTRODUCTION

1.1 Block Diagram

The SL811HS USB Host embedded Controller is a single chip USB embedded host device solution that can communicate with either Full-speed USB peripherals or low-speed Peripherals. The SL811HS can interface to devices such as microprocessors, microcontrollers, DSPs or directly to a variety of buses such as ISA, PCMCIA and others. The SL811HS USB Host Controller conforms to USB Specification 1.1

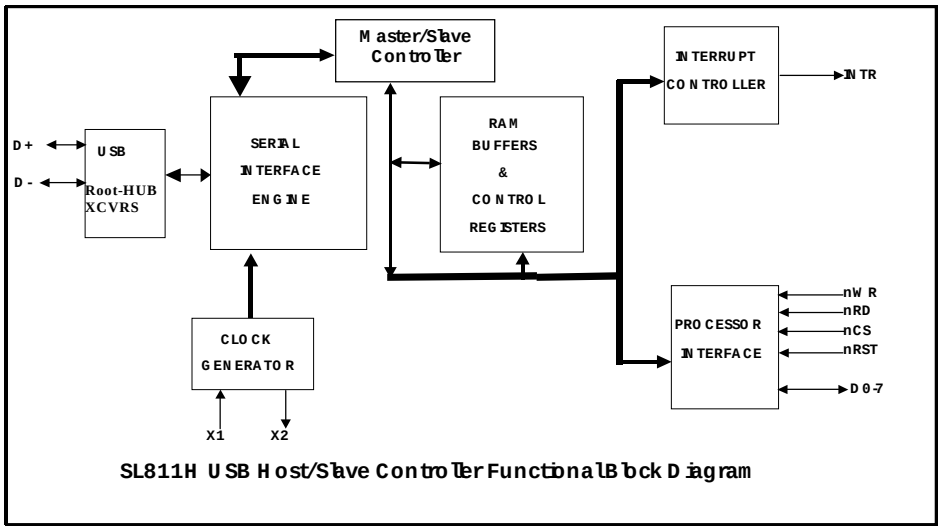
The SL811HS USB Host/Slave Controller incorporates USB Serial Interface functionality along with internal Full/low-speed transceivers. The SL811HS supports and operates in USB full speed mode at 12Mbits/sec, or at low speed 1.5Mbits/sec mode.

The SL811HS data port and microprocessor interface provide an 8-bit data path I/O or DMA bi-directional, with interrupt support to allow easy interface to standard microprocessors or microcontrollers such as Motorola or Intel CPUs and many others. Internally, the SL811HS contains a 256-byte RAM data buffer, which is used for control registers and data buffer.

Internally, the SL811HS/SL811HST contains a 256-byte RAM data buffer. The RAM contains Pin PLCC (SL811HS) and a 48 Pin LPQFP package (SL811HST). Both products operate at 3.3 VDC. The I/O interface logic is 5V tolerant.

1.2 SL811HS/SL811HST Host or Slave Mode Selection [Master/Slave mode]

SL811HS/SL811HST can work in two modes – host or slave. For Slave mode operation and specification, please refer to the SL811S/SL811ST specification.



SL811H USB Host/Slave Controller Functional Block Diagram

Features

- The only USB host/Slave controller for embedded system in the market with a standard microprocessor bus interface.
- Supports both Full speed (12Mbps) and low speed (1.5Mbps) USB transfer

➢ *USB Specification Compliance*

- Conforms to USB Specification 1.1

➢ *CPU Interface*

- Operates as a Single USB Host, or Slave under Software control
- Low Speed 1.5Mbps, and Full Speed 12Mbps, in both Master and Slave modes
- Automatic Detection of either Low/Full speed devices
- 8 bit Bi-directional Data, port I/O (DMA supported in slave mode)
- On-Chip SIE and USB transceivers
- On-Chip Single Root HUB support
- 256 bytes Internal SRAM buffer, Ping-Pong operation
- Operates from 12 MHz or 48 MHz crystal or oscillator (Built-in DPLL)
- 5 V tolerant Interface
- Suspend/resume, wake up and low power modes are supported
- Auto Generation of SOF, and CRC5/16
- Auto Address increment mode, saves memory READ/Write Cycles
- Development kit including source code drivers is available
- Backward compatible with SL11H, both pin and functionality
- 3.3V power source, 0.35 micron CMOS Technology
- Available in both 28-Pin PLCC or 48-Pin LPQFP packages

1.3 Data port, Microprocessor Interface.

The SL811HS microprocessor interface provides an 8-bit bi-directional data path along with appropriate control lines to interface to external processors or controllers. The control lines, Chip Select, Read and Write input strobes and a single address line, A0, along with the 8-bit data bus, support programmed I/O or Memory mapped I/O designs.

Access to memory and control register space is a simple two step process, requiring an address write with A0 set = '0' followed by a register/memory read or write cycle with address line A0 set = '1'.

In addition, DMA bi-directional interface in slave mode is available with handshake signals such as DREQ, ACK, WR, RD, CS and INTR. Please refer to SL11/SL11T spec rev 1.6.

The SL811HS write or read operation terminates when either nWR or nCS goes inactive. For devices interfacing to the SL811HS/SL811HST, that deactivate the Chip Select nCS before the write nWR, the data hold timing should be measured from the nCS and will be the same value as specified. Thus, both Intel and Motorola type CPU's can work easily with the SL118H/SL811HST without any external glue logic requirements.

1.4 Interrupt Controller

The SL811HS interrupt controller provides a single output signal (INTRQ) that can be activated by a number of events that may occur as result of USB activity. Control and status registers are provided to allow the user to select single or multiple events, which will generate an interrupt (assert INTRQ), and lets the user view interrupt status. The interrupts can be cleared by writing to the appropriate register (the Status Register at address 0x0d).

1.5 Buffer Memory

The SL11H/SL11HT contains 256 bytes of internal buffer memory. The first 16 bytes of memory represent control and status registers for programmed I/O operations. The remaining memory locations are used for data buffering (max 240 Bytes).

Access to the registers and data memory is through an external microprocessor, 8 bit data bus, in either of two addressing modes, indexed or, if used with multiplexed address/data bus interfaces, direct access. With indexed addressing, the address is first written to the device with the A0 address line low, then the following cycle with A0 address line high is directed to the specified address. USB transactions are automatically routed to the memory buffer. Control registers are provided, so that pointers and block sizes in buffer memory can be can set up.

Auto Address Increment Mode
The SL811H supports auto increment mode for Read or Write Cycles, A0 mode. In A0 mode, the Micro Controller sets up the address only once. On any subsequent DATA Read or Write access, the internal address pointer will advance to the next DATA location.

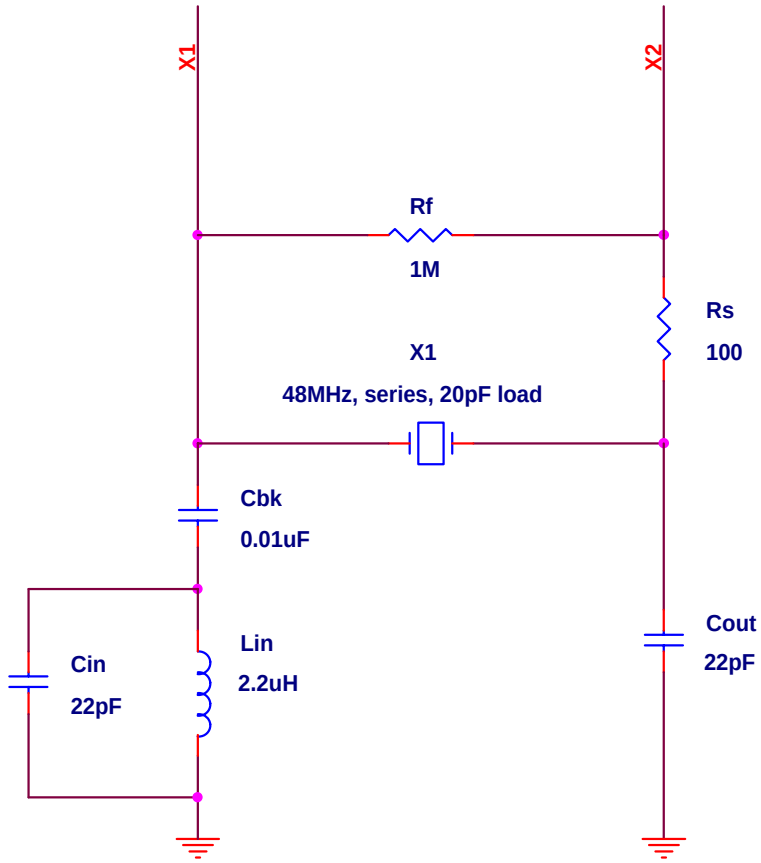
- *For example*

Write 0x10 to SL811HS in address cycle (A0 is set low)
Write 0x55 to SL811HS in data cycle (A0 is set high) -> write 0x55 to location 0x10
Write 0xaa to SL811HS in data cycle (A0 is set high) -> write 0xaa to location 0x11
Write 0xbb to SL811HS in data cycle (A0 is set high) -> write 0xbb to location 0x12

The advantage of auto address increment mode is that it reduces the number of SL811HS memory read/write cycles required to move data to/from the device. For example, transferring 64-bytes of data to/from SL811HS using auto increment mode, will reduce the number of cycles to 1 Address Write and 64 Read/Write Data cycles, compared to 64 Address Writes and 64 Data Cycles for Random Access.

1.6 PLL Clock Generator

Either a 12 MHz or a 48 MHz external crystal can be used with the SL811H. Two pins, X1 and X2, are provided to connect a low cost crystal circuit to the device (Fig 2). If an external 48 MHz clock source is available in the application it can be used instead of the crystal circuit by connecting, the source directly to the X1 input pin. When a clock is used, the X2 pin is left unconnected.



Note: CM (Clock Mode) Pin of SL811 should be tied to Gnd. when 48 MHz Xtal circuit or 48 MHz clock source is used.

Figure 1: ***Full-Speed 48 MHz Crystal Circuit***

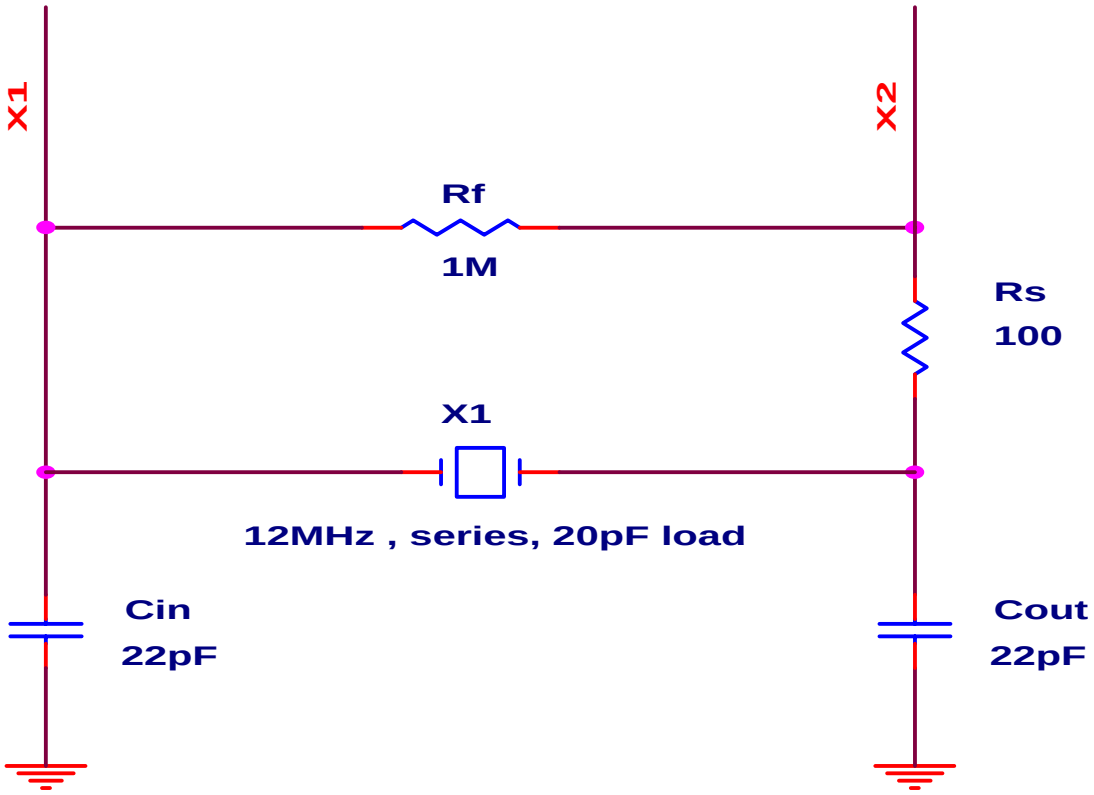


Figure 2*: optional 12 Mhz Crystal Circuit*

1.6.1 Typical Crystal requirements

The following are examples of "typical requirements". Please note that these specifications are generally found as standard crystal values and are therefore less expensive than custom

values. If crystals are used in series circuits, load capacitance is not applicable. Load capacitance of parallel circuits is a requirement.

12 MHz Crystals:

Frequency Tolerance:	+/- 100 ppm or better.
Operating Temperature Range:	0 to 70 degrees C.
Frequency:	12 MHz.
Frequency Drift over Temperature:	+/- 50 ppm.
ESR (Series Resistance):	60 Ohms
Load Capacitance:	10 Pf Min.
Shunt Capacitance:	7 Pf Max
Drive Level:	0.1 - 0.5 mW.
Operating Mode:	Fundamental

48 MHz Crystals:

Frequency Tolerance:	+/- 100 ppm or better.
Operating Temperature Range:	0 to 70 degrees C.
Frequency:	48 MHz.
Frequency Drift over Temperature:	+/- 50 ppm.
ESR (Series Resistance):	40 Ohms
Load Capacitance:	10 Pf Min.
Shunt Capacitance:	7 Pf Max
Drive Level:	0.1 - 0.5 mW.
Operating Mode:	3 rd Overtone

1.7 USB Transceiver

The SL811HS has a built in transceiver that meets USB Specification 1.1. The transceiver is capable of transmitting and receiving serial data at USB full speed (12 Mbits) and low speed (1.5Mbits). The driver portion of the transceiver is differential, while the receiver, section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine, **(SIE),** logic. Externally the transceiver connects to the physical layer of the USB.

2 SL811HS/SL811HST REGISTERS

Operation of the SL811HS is controlled through 16 internal registers. A portion of the internal RAM is devoted to the control register space, and access is through the microprocessor interface. The registers provide control and status information for transactions on the USB, microprocessor interface and interrupts.

The SL811HS full features bit will be enabled during any write to control register 0FH. For SL11H hardware backward compatibility, this register should not be accessed.

This table shows the memory map and register mapping of both the SL11H and SL811HS. The SL11H is shown for users upgrading to the SL811HS.

Register Name SL11H and SL811HS	SL11H (hex) Address	SL811HS (hex) Address
USB-A Host Control Register	00H	00H
USB-A Host Base Address	01H	01H
USB-A Host Base Length	02H	02H
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03H	03H
USB-A Host Device Address (Write)/Transfer Count (Read)	04H	04H
Control Register1	05H	05H
Interrupt Enable Register	06H	06 H
Reserved Register	Reserved	Reserved
USB-B Host Control Register	Reserved	08H
USB-B Host Base Address	Reserved	09H
USB-B Host Base Length	Reserved	0AH
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	Reserved	0BH
USB-B Host Device Address (Write)/Transfer Count (Read)	Reserved	0CH
Status Register	0DH	0DH
SOF Counter Low (Write)/HW Revision Register (Read)	0EH	0E H
SOF Counter High and Control Register2	Reserved	0F H
Memory Buffer	10H-FFH	10H-FFH

The registers in the SL811HS are divided into two major groups. The first group is referred to as USB Control registers. These registers enable and provide status for control of USB transactions and data flow. The second group of registers provides control and status for all other operations.

2.1 USB Control Registers

Communication and data flow on the USB uses the SL811H's USB A-B Control Registers. The SL811HS can communicate with any USB Device functions and any specific endpoints via the USBA or USBB register sets.

The USB A-B Host Control Registers can be used in a Ping-Pong arrangement to manage traffic on the USB. The USB Host Control Register also provides a means to interrupt an external CPU or Micro Controller when one of the USB protocol transactions is completed. The following table shows the two sets of USB Host Control Registers, the '**A**' set and '**B**' set. The two register sets allows for overlapped operation. When one set of parameters is being set up, the other is transferring. On completion of a transfer to an endpoint, the next operation will be controlled by the other register set.

Note: *On the SL11H, the USB-B set control registers are not used. The USB-B register set can be used only when SL811HS mode is enabled by initializing register 0FH.*

Register Name SL11H and SL811H	SL11H (hex) Address	SL811HS (hex) Address
USB-A Host Control Register	00H	00H
USB-A Host Base Address	01H	01H
USB-A Host Base Length	02H	02H
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03H	03H
USB-A Host Device Address (Write)/Transfer Count (Read)	04H	04H
Control Register1	05H	05H
Interrupt Enable Register	06H	06 H
Reserved Register	Reserved	Reserved
USB-B Host Control Register	Reserved	08H
USB-B Host Base Address	Reserved	09H
USB-B Host Base Length	Reserved	0AH
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	Reserved	0BH
USB-B Host Device Address (Write)/Transfer Count (Read)	Reserved	0CH
Status Register	0DH	0DH
SOF Counter Low (Write)/HW Revision Register (Read)	0EH	0E H
SOF Counter High and Control Register2	Reserved	0F H
Memory Buffer	10H-FFH	10H-FFH

The SL811HS USB Host Control has two groups of five registers each, which map in the SL811HS memory space. These registers are defined as follows:

SL811HS/SL811HST Host Control Registers

Register Name SL11H and SL811H	SL11H (hex) Address	SL811HS (hex) Address
USB-A Host Control Register	00H	00H
USB-A Host Base Address	01H	01H
USB-A Host Base Length	02H	02H
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03H	03H
USB-A Host Device Address (Write)/Transfer Count (Read)	04H	04H
USB-B Host Control Register	Reserved	08H
USB-B Host Base Address	Reserved	09H
USB-B Host Base Length	Reserved	0AH
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	Reserved	0BH
USB-B Host Device Address (Write)/Transfer Count (Read)	Reserved	0CH

SL811HS/SL811HST Control Register Map

Register Name SL11H and SL811H	SL11H (hex) Address	SL811HS (hex) Address
Control Register1	05H	05H
Interrupt Enable Register	06H	06 H
Reserved Register	07H	07 H
Status Register	0DH	0DH
SOF Counter Low (Write)/HW Revision Register (Read)	0EH	0E H
SOF Counter High and Control Register2	Reserved	0F H
Memory Buffer	10H-FFH	10H-FFH

2.1.1 USB-A / USB-B Host Control Register [00H, 08H]

Bit Position	Bit Name	Function
0	Arm	Allows enabled transfers when set =’1’. Cleared to '0' when transfer is complete.
1	Enable	When set = '1' allows transfers to this endpoint. When set "0 USB transactions are ignored. If Enable = '1' and Arm = '0' the endpoint will return NAK's to USB transmissions.
2	Direction	When set = '1' transmit to Host. When '0' receive from Host.
3	Reserved	(Note 2)
4	ISO	When set to '1' allows Isochronous mode for this endpoint.
5	SOF	‘1’ = Synchronize with the SOF transfer (Note1)
6	DATA Toggle Bit	'0' if DATA0, '1' if DATA1.
7	Preamble	If set = ‘1’ a preamble token is transmitted prior to transfer of low speed packet(note3). If set = ‘0’, preamble generation is disabled.

Notes:

- This bit was designated as a STALL bit in the SL11H implementation. The SL811HS uses the bit to enable transfer of a data packet after a SOF packet is transmitted. When this bit set ‘1’, the next enabled packet will be sent after next SOF. If set = ‘0’ the next packet is sent immediately if the SIE is free.

- This bit is reserved for future usage.

- The SL811HS automatically generates preamble packets when bit 7 is set. This bit is only used to send packets to a low speed device through a HUB. To communicate to a full speed device, this bit is set to zero. As an example:

  - When SL811HS communicates to a low speed device via the HUB:

    - SL811HS SIE should set to operate at 48 MHz, i.e. Bit 5 of register 05H should be set = ‘0’.
    - Bit 6 of register 0FH should be set = ‘0’, set correct polarity of DATA+ and DATA- state for Full Speed.
    - Bit 7, Preamble Bit, should be set = ‘1’ in Host Control register.

- When SL811HS communicates directly to low speed device

  - SL811HS. Bit 5 of register 05H should be set = '1'.
  - Bit 6 of register 0FH should be set ='1', DATA+ and DATA- polarity for low speed.
  - The state of bit 7 is ignored in this mode.

2.1.2 Example of SL11H/SL11HT USB Packet Transfer:

One byte PID and two bytes for USB Address and Endpoint and pre-calculated CRC5 needs to be included in the memory buffer for the Token packet.

➢ For example:

- *SL11H memory setup is set as follows:*

40h	PID
41h	USB Device Address in low byte
42h	Endpoint and CRC5 in high byte
43h-82h	USB Data, depending on the PID.

The CRC5 must be pre-computed by software. See the sample code.

The memory data can be pre-copied before the setup of the ARM bit on this register. The user can use the Ping-Pong scheme by reserving additional memory locations prior to the transfer. The USB Host "Base Address " and USB Host "Base Length" can be reprogrammed to adapt the Ping-Pong operation. See the example code.

2.1.3 Example – SL11H USB Transaction to Transfer 128-bytes of Data to a Peripheral:

➢ *SL11H/SL11HT Memory Allocation*

10H-52H	is buffer A

Where:

10h	PID=E1
11h	USB Device Address
12h	Endpoint and CRC5
13h-52h	64-byte of USB Data
53H-95H	is buffer A
53h	PID=E1
54h	USB Device Address
55h	Endpoint and CRC5
56h-95h	64-byte of USB Data.

2.1.4 Example of SL811HS/SL811HST USB packet transfer

- *SL11H memory setup as shown:*

  03h-04h Register will contain PID and Device endpoint and Device Address.
  10h-4Fh USB Data as required.

2.1.5 SOF Packet Generation

The SL811HS automatically computes CRC5 by hardware. No CRC or SOF is required to be generated by external firmware for SL811HS/T

2.1.6 USB-A/USB-B Host Base Address [01H, 09H]

The USB-A/USB-B Base Address is a Pointer to the SL811HS memory buffer location for USB reads and USB writes. When transferring data OUT (Host to Device), the USB-A and USB-B can be set up prior to setting ARM on the USB-A or USB-B Host Control register. See the software implementation example.

USB-A/USB-B Host Base Length [02H, 0AH]

The USB A/B host base register contains the maximum packet size to be transferred between the SL811HS and a slave USB peripheral. Essentially, this designates the largest packet size that can be transferred by the SL811H. Base Length designates the size of data packet to be sent. For example, in Bulk mode the maximum packet length is 64 bytes. In ISO mode, the maximum packet length is 1023, since the SL811HS only has an 8-bit length; the maximum packet size for the ISO mode using the SL811HS is 255 – 16 bytes. When the Host Base Length register is set to zero, a Zero-Length packet will be transferred.

USB-A/USB-B Host PID, Device Endpoint (Write)/USB Status (Read) [03H, 0BH]

➢ *This register has two modes:*

- When read, this register provides packet status and it contains information relative to the last packet that has been received or transmitted. The register is defined as follows:

Bit Position	Bit Name	Function
0	ACK	Transmission Acknowledge.
1	Error	Error detected in transmission.
2	Time-out	Time-out occurred.
3	Sequence	Sequence Bit. '0' if DATA0, '1' if DATA1.
4	Setup	'1' indicates Setup Packet
5	Overflow	Overflow condition - maximum length exceeded during receives.
6	NAK	Slave returns NAK
7	STALL	Slave set STALL bit

- When written, this register provides the PID and Endpoint information to the USB SIE engine to be used in the next transaction. All sixteen Endpoints can be addressed by the SL811HST.

D7	D6	D5	D4	D3	D2	D1	D0
PID3	PID2	PID1	PID0	EP3	EP2	EP1	EP0

PID3-0 4 bit PID Field (See Table Below)
EP3-0 4 Bit Endpoint Value in Binary.

PID TYPE	D7-D4
SETUP	1101 (D Hex)
IN	1001 (9 Hex)
OUT	0001 (1 Hex)
SOF	0101 (5 Hex)
PREAMBLE	1100 (C Hex)
NAK	1010 (A Hex)
STALL	1110 (E Hex)
DATA0	0011 (3 Hex)
DATA1	1011 (B Hex)

USB-A/USB-B Host Transfer Count Register (Read), USB Address (Write) [04H, 0CH]

➢ This register has two functions:

- When read, this register contains the number of bytes left over (from 'Length' field) after a packet is transferred. If an overflow condition occurs, i.e., the received packet from slave USB device was greater than the Length field specified, a bit is set in the Packet Status Register indicating the condition.

- When written, this register will contain the USB Device Address that the Host wishes to communicate to.

D7	D6	D5	D4	D3	D2	D1	D0
0	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA6-DA0 Device Address, up to 127 Device can be addressed
DA7 Reserved bit should be set zero.

2.2 SL811HS/SL811HST Control Registers

Register Name SL11H and SL811H	SL11H (hex) Address	SL811HS (hex) Address
Control Register1	05H	05H
Interrupt Enable Register	06H	06 H
Reserved Register	07H	07 H
Status Register	0DH	0DH
SOF Counter Low (Write)/HW Revision Register (Read)	0EH	0E H
SOF Counter High and Control Register2	Reserved	0F H
Memory Buffer	10H-FFH	10H-FFH

2.2.1 Control Register 1, Address [05H]

The Control Register 05H enables/disables USB transfer operation with control bits defined as follows:

Bit	Bit Name	Function
0	SOF ena/dis	'1' enable auto Hardware SOF generation, '0'=disable (Note1)
1	Reserved	
2	EOF2	'1' = Prevent sending packet during EOF2 time frame
3	USB Engine Reset	USB Engine reset = '1'. Normal set '0' (Note 3).
4	J-K state force	See the table below
5	USB Speed	'0' setup for full speed, '1' setup low speed.
6	Suspend	'1' enable, '0' =disable
7	Reserved	

NOTE: At power up this register will be cleared to all zero's.

- In the SL811HS, bit is used to enable HW SOF auto-generation. (Bit 0 was not used in the SL11H).
- Bit-2 allows enable/disable of packet transmission during EOF2 (End of Frame) time. This bit should be enabled for normal operation. The purpose of this bit is to prevent the host from initiating any transaction during EOF2. EOF2 duration is 42-bits prior to SOF packet transmission. Refer to chapters 5 and 11 in USB Spec Rev 1.1.

2.2.2 J-K Programming states, [bit 3 and 4 of Control Register 05H]

The J-K force state control and USB Engine Reset bits can be used to generate USB reset condition on the USB. Forcing K-state can be used for Peripheral device remote wake-up, Resume and other modes. These two bits are set to zero on power up.

JK-Force State	USB Engine Reset	Function
0	0	Normal operating mode
0	1	Force USB Reset, D+ and D- are set low
1	0	Force K-State, D- set high, D+ set low
1	1	Force J-State, D+ set high, D- set low

2.2.3 Low Speed/Full Speed modes. [bit 5 and bit 6 of Control Register 05H]

The SL811HS is designed to communicate with either full or low speed devices. At power up bit 5 will be set low, i.e. for full speed. There are two cases when communicating with a low speed device:

- When a low speed device is connected directly to the SL811H, bit-5 of Register 05H should be set to logic '1' and bit –6 of register 0FH, Output-Invert, needs to be set to "1" in order to change the polarity of D+ and D-.
- When a low speed device is connected via an HUB to SL811H, bit-5 of Register 05H should be set to logic '0' and bit -6 of register 0FH should be set to logic '0' in order to keep the polarity of D+ and D- for full speed. In addition, make sure that bit-7 of USB-A/USB-B Host Control Registers [00H, 08H] is set to "1".

2.2.4 Low Power modes [bit 6 Control Register 05H]

When bit-6 (Suspend) is set to '1', the power of transmit transceiver will be turned off, the internal RAM will be in the suspend mode and the internal clock of SIE will be disabled.

NOTE: To stop the SIE Clock, set bit 6 of register 05H to high and set bit-0 of register 05H to '0' (low).

2.2.5 Interrupt Enable Register, Address [06H]

The SL811HS provides an Interrupt Request Output, which can be activated on a number of conditions. The Interrupt Enable Register allows the user to select conditions that will result in an Interrupt being issued to an external CPU. A separate Interrupt Status Register is provided. It can be polled in order to determine those conditions that initiated the interrupt. (See Interrupt Status Register description). When a bit is set to '1' the corresponding interrupt is enabled.

Bit Position	Bit Name	Function
0	USB-A	USB-A done Interrupt.
1	USB-B	USB-B done Interrupt.
2	Babble Detection	1=enable interrupt on babble detection
3	Reserved	
4	SOF timer	1=enable interrupt on 1ms SOF timer
5	Inserted/Removed	Slave Insert/Remove detection
6	USB Reset/Resume	Enable USB Reset/Resume Interrupt.

- Bits 0-1 are used for the USB A/B controller interrupt.
- Bit 2 is a status bit for Babble detection.

- **Babble detection** is shown in the Status register 0DH. Babble is defined as bus activity after a Start of Packet and activity past the end of a Frame. The user should schedule transactions so that this condition does not occur. When bit 2 is set, Babble condition on the USB is checked for during EOF2 high time. The interrupt informs the user that the last frame had too many packets sent out during that specific frame. The user should recalculate the number of packets to be sent during one frame time to avoid transactions occurring during EOF2. Note the hardware will not prevent sending a packet when EOF2 is active. If a packet is sent when EOF2 is active, the packet should be resent after SOF packet. The max number of packets that can be sent within one frame depends on the type and size of packets to be sent. The user should match his requirements to the available bandwidth in a frame time. Refer to USB 1.1 specifications (Chapter 5 and 11).

- Bit-4 is used to enable/disable the SOF timer. To utilize this bit function, bit 0 of register 05H must be enabled and the SOF counter registers 0EH and 0FH must be initialized.

- Bit 5 may be used to detect device connection or removal.

- When bit-6 of register 05H is set = '1', this bit used as Resume Detect, otherwise, this bit is used for the USB_RESET detect.

2.2.6 USB Address Register, Reserved, Address [07H]

This register is reserved for the device USB Address in Slave operation. It should not be written by the user.

2.2.7 Interrupt Status Register, Address [0DH]

The ISR is a Read/Write register providing interrupt status. Interrupts can be cleared by writing to this register. To clear a specific interrupt, the register is written with corresponding bit set to "1".

Bit Position	Bit Name	Function
0	USB-A	USB-A done Interrupt.
1	USB-B	USB-B done Interrupt.
2	Babble Detection	1=enable interrupt on babble detection
3	Reserved	
4	SOF timer	1=enable interrupt on 1ms SOF timer
5	Insert/Remove	Slave Insert/Remove detection (Note 2)
6	USB Reset/Resume	Enable USB Reset/Resume Interrupt. (Note 1)
7	D+	Value of the Data+ pin

NOTE 1: This bit is shared between USB_RESET and Resume interrupts detection. When bit-6 of register 05H is set to one, this bit will be the Resume detection Interrupt bit. Otherwise, this bit is used to indicate detection of USB RESET.

NOTE 2: Bit-5 is provided to support USB cable Insertion/Removal for the SL811HS in Host Mode. This bit is set when there is any rising or trailing edge of the USB_RESET condition on the USB.

- Bit 7 provides continuous USB Data+ line status. Bit 7 in conjunction with bit 6 can be used to detect if a Low or Full speed device is connected after USB reset is issued.

2.2.8 Current Data Set Register/Hardware Revision/SOF Counter Low, Address [0EH]

➢ *This register has two modes:*

- A read from this register indicates currently selected data set for the selected Cypress USB controller set.

Bit Position	Bit Name	Function
0	USB-A	Data Toggle pin for USB-A
1	USB-B	Data Toggle pin for USB-B
2	Reserved	Read will be Zero.
3	Reserved	Read will be Zero.
4-7	HW Revision	SL11H read=0H, SL811HS read = 1H

- Writing to this register will setup auto generation of SOF to all connected peripherals. This counter is based on the 12 MHz clock. To setup a 1ms timer interval, the software must setup both SOF counter registers to the proper values.

Bit Position	Bit Name	Function
0-7	SOF Low Counter Register	Write Only to set SOF Low Counter Register, OEH

- Example: To set up SOF for 1ms interval, SOF counter register 0EH should be set to E0H.

2.2.9 SOF Counter High/Control2 Register, Address [0FH, READ/WRITE]

When writing to this register the bits definition are defined as follow:

Bit Position	Bit Name	Function
0-5	SOF High Counter Register	Write a value or read it back to SOF High Counter Register
6	SL811HS D+/D- Data Polarity Swap	Write/Read, set "1" change polarity, "0" no change of polarity
7	SL811HS Master/Slave selection	Write/Read, "1" is master, else Slave

NOTE: The SL811HS new feature bit will be enabled during any write to control register 0FH. The USB-B register set can be used when SL811HS mode is enabled. For the SL11H hardware backward compatible, this register should not be accessed.

- Example – To set up for 1 ms SOF Time:

  The register 0FH contains the upper 6-bits of the SOF timer. Register 0EH contains the lower 8-bits of the SOF timer. The timer is based on a 12 MHz clock and uses a counter, which counts down to zero from an initial value. To set the timer for 1 ms time, the register 0EH should be loaded with value E0H, register 0F, Bits 0-5 should be loaded with 2EH. To start the timer, bit 0 of register 05H should be set to "1". To load both high and low registers with the proper values the user must follow this sequence:

  - Write E0H to register 0EH
  - Write 2EH to register 0FH, Bits 0-5. Bits 6 and 7 should be set for appropriate function: polarity and Master/Slave.
  - Enable bit 0 in register 05H.

NOTE: Any write to the 0FH register will clear the internal frame counter. Register 0FH must be written at least once after power up. The internal frame counter is incremented after every SOF timer tick. The internal frame counter is an 11-bit counter, which is used to track the frame number. The frame number is incremented after each timer tick. Its contents are transmitted to the slave every millisecond in a SOF packet.

Master/Slave SL811HS selection mode, Read Register 0FH

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
C13	C12	C11	C10	C9	C8	C7	C6

C13-C6 Top 8 bits of 14 Bit SOF Counter.

When read, this register will return the value of the SOF Counter divided by 64. The software should use this register to determine the available bandwidth in the current frame before

initiating any USB transfer. In this way, the user will be able to avoid Babble conditions on the USB.
For example to determine the available bandwidth left in a frame:
Maximum number of clock ticks in 1ms time frame is 12000(1 count per 12 MHz clock period or approx. 84 ns.) The value read back in Register 0FH is the (count X 64) X 84 ns = time remaining in current frame. USB bit time = One 12 MHz period.

Value of register 0FH	**Available bit Times left are between**
BBH	12000 bits to (186 X 64) bits
BCH	(186 X 1/64) bits to (185 X 64) bits
BDH	(185 X 1/64) bits to (184 X 64) bits

3 SL811HS / SL811HST PHYSICAL CONNECTION

The diagrams below indicate pin assignments for both SL811HS 28-pin PLCC and SL811HST 48-Pin LPQFP Packages.

SL811HS Pin Layout

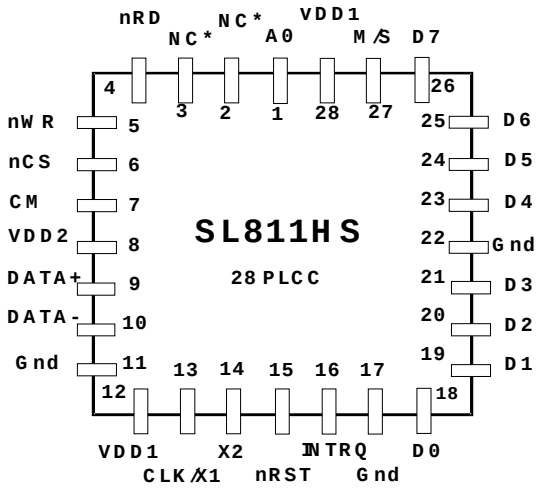
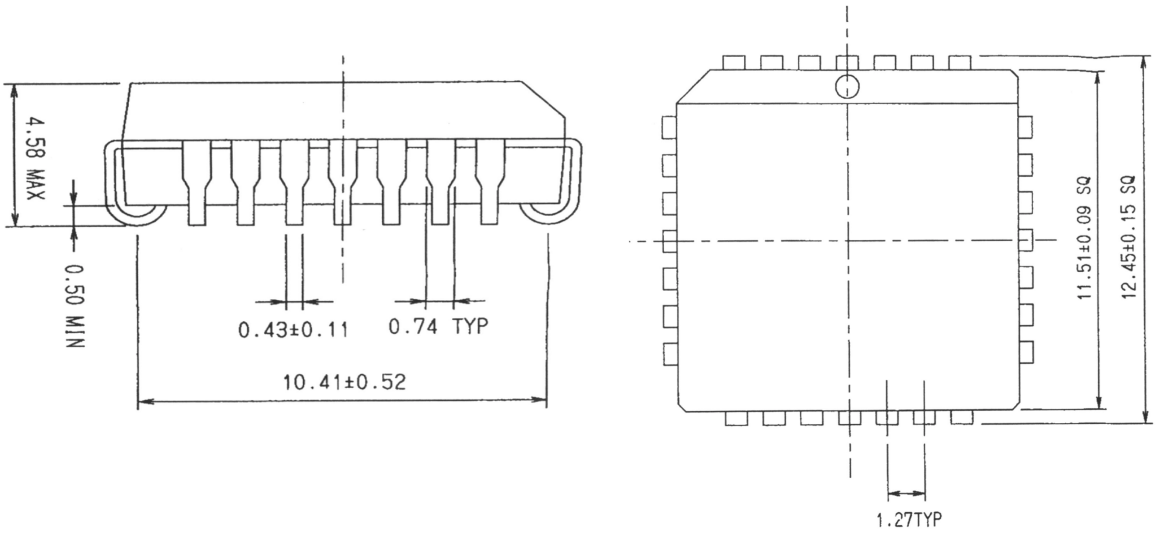


Figure 3: ***SL811HS USB Host/Slave Controller - Pin layout***

Note: Pins 2 and 3 should be no connects in Host Mode. See Pin and Signal Description

3.1 28-PIN PLCC Mechanical Dimensions



3.2 SL811HS USB Host Controller Pins Description

The SL811HS package is a 28 Pin PLCC. The device requires 3.3 VDC. Average typical current consumption is less then 20 mA for 3.3V.

SL811HS Pin Assignments and Definitions.

Pin No.	Pin Type	Pin Name	Pin Description
1	IN	A0	A0 = '0'. Selects Address Pointer. Reg. Write Only. Selects Data Buffer or Register. R/W. See Note 1.
2	IN	nDACK	DMA Acknowledge. An active low input used to interface to an external DMA controller. This works only in slave mode. In host mode, Pin should be tied to Logic '1' in Host Mode.
3	OUT	nDRQ	DMA Request. An active low output used with an external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers. In host mode, Pin must be left unconnected in Host Mode.
4	IN	nRD	Read Strobe Input. An active low input used with nCS to read registers/data memory.
5	IN	nWR	Write Strobe Input. An active low input used with nCS to write to registers/data memory.
6	IN	nCS	Active low SL811HS Chip select. Used with nRD and nWD when accessing SL811H.
7	IN	CM	Clock Mode. Select Internal 4 X Clock Multiplier. '1' Enables 4 X Clock Mutilplier. '0' Disables. See Note 2.
8	VDD1	+3.3 VDC	Power for USB Transceivers.

9	BIDIR	DATA +	USB Differential Data Signal High Side.
10	BIDIR	DATA -	USB Differential Data Signal Low Side.
11	GND	USB GND	Ground Connection for USB.
12	VDD	+3.3 VDC	SL811HS Device VDD Power.
13	IN	CLK/X1	12/48 MHz Clock or External Crystal X1 connection. See Note 3.
14	OUT	X2	External Crystal X2 connection.
15	IN	nRST	SL811HS Device active low reset input.
16	OUT	INTRQ	Active high Interrupt Request output to external controller.
17	GND	GND	SL811HS Device Ground
18	BIDIR	D0	Data 0. Microprocessor Data/(Address) Bus.
19	BIDIR	D1	Data 1. Microprocessor Data/(Address) Bus.
20	BIDIR	D2	Data 2. Microprocessor Data/(Address) Bus.
21	BIDIR	D3	Data 3. Microprocessor Data/(Address) Bus.
22	GND	GND	SL11H Device Ground.
23	BIDIR	D4	Data 4. Microprocessor Data/(Address) Bus.
24	BIDIR	D5	Data 5. Microprocessor Data/(Address) Bus.
25	BIDIR	D6	Data 6. Microprocessor Data/(Address) Bus.
26	BIDIR	D7	Data 7. Microprocessor Data/(Address) Bus.
27	IN	M/S	Master/Slave Select. Host = '0', Slave = '1'.
28	VDD	+3.3 VDC	SL811HS Device VDD Power.

Notes:

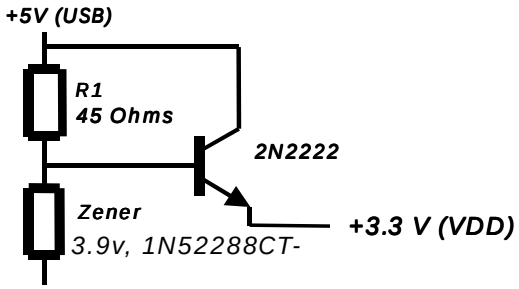
1 The A0 Address bit is used to access address register or data registers in I/O Mapped or Memory Mapped applications CM Clock Multiplier (SL811HS/SL811HST Only).

2 When a 12 MHz Clock Source is used, this pin should be tied high. In SL11H, this pin was designated as ALE input pin.

3 VDD can be derived from the USB supply. The diagram below shows a simple method to provide 3.3V/30mA. Another option is to use a Torex Semiconductor 3.3V SMD regulator P/N XC62HR3302MR.

4 The X1/X2 Clock requires external 12 or 48 MHz matching crystal or clock source.

The Diagram below illustrates a simple +3.3 V Voltage source:



Sample VDD Generator

3.3 Package Markings (SL811HS)

YYWW = Date code
XXXX = Product code

3.4 SL811HST Pin Layout

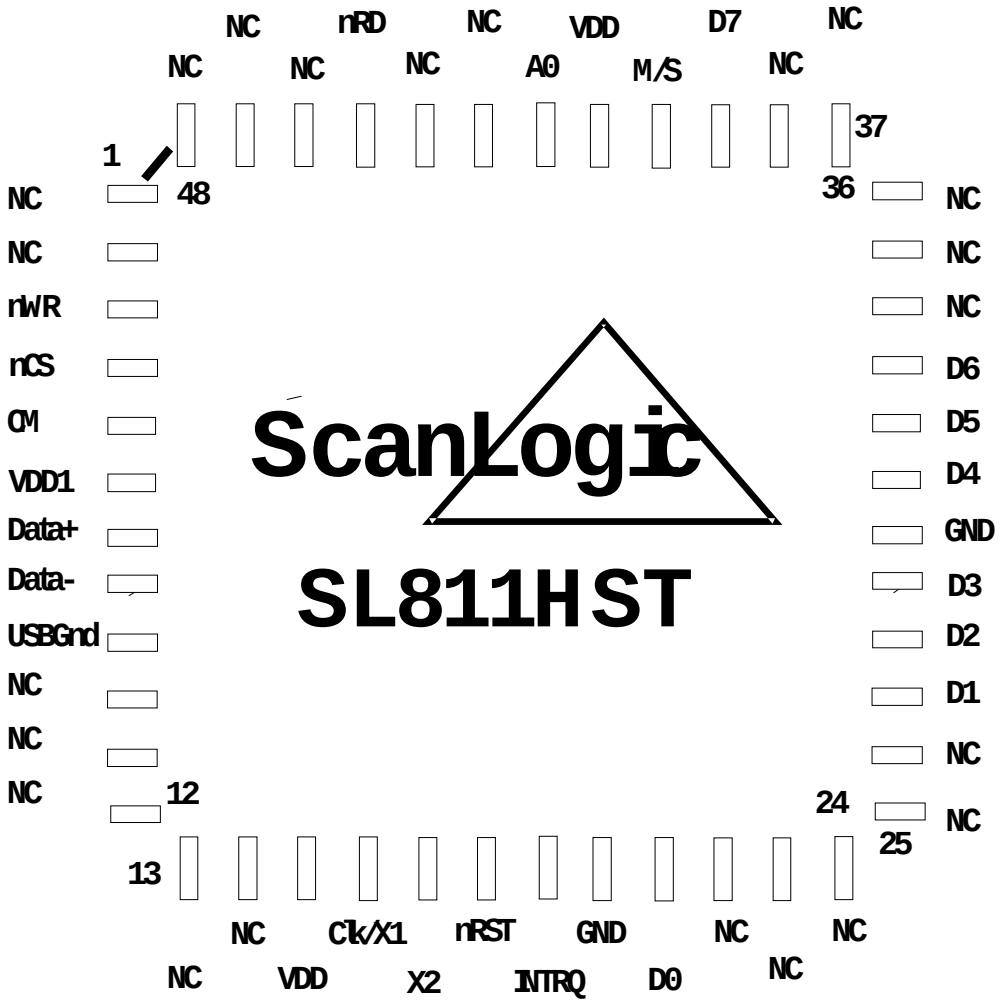
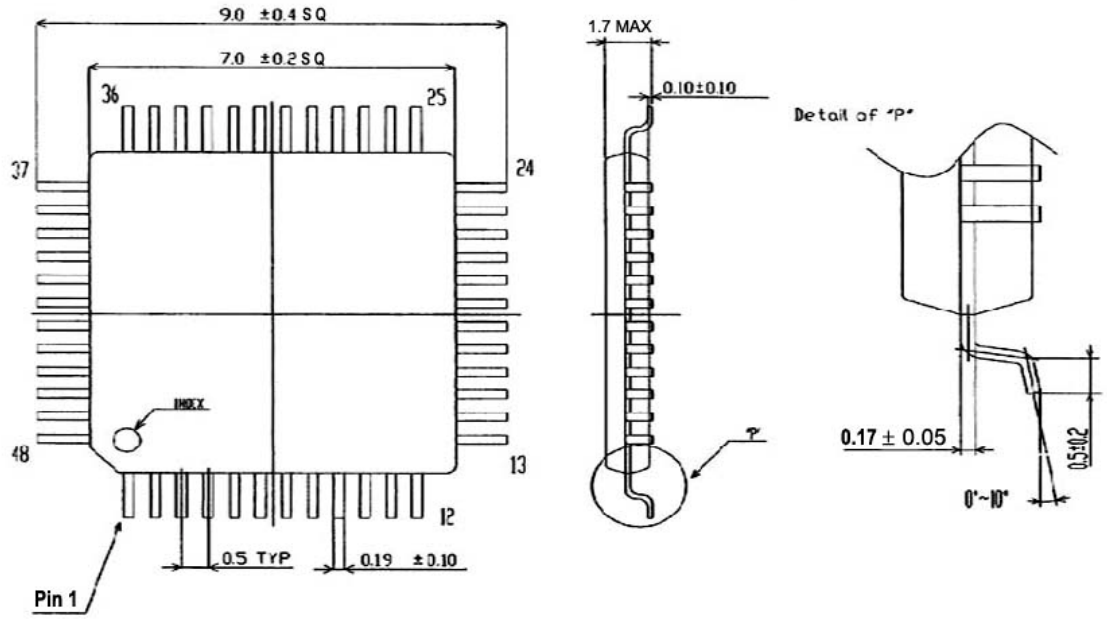


Figure 4: ***SL811HST USB Host/Slave Controller Pin Layout***

NC. Indicates No Connection. NC Pins should be left unconnected.

3.5 Mechanical Dimensions 48 Pin LQPFP



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SL811HST USB Host Controller Pins Description

The SL11HT is packaged in a 48 Pin LPQFP. The device requires a 3.3VDC power source. The SL811HST requires an external 12 or 48 MHz crystal or Clock.

3.6 SL811HST Pin Assignments and Definitions

Pin No.	Pin Type	Pin Name	Pin Description
1	NC	NC	NC
2	NC	NC	NC
3	IN	nWR	Write Strobe Input. An active low input used with nCS to write to registers/data memory.
4	IN	nCS	Active low SL811HST Chip select. Used with nRD and nWr when accessing SL811HT.
5	IN	CM	Clock Mode. Select 12 MHz/48 MHz Clock Source. Note 2
6	VDD1	+3.3 VDC	Power for USB Transceivers. VDD1 may be connected to VDD.
7	BIDIR	DATA +	USB Differential Data Signal High Side.
8	BIDIR	DATA -	USB Differential Data Signal Low Side.

9	GND	USB GND	Ground Connection for USB.
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	VDD	+3.3 VDC	SL811HST Device VDD Power.
16	IN	CLK/X1	Clock or External Crystal X1 connection.
17	OUT	X2	External Crystal X2 connection.
18	IN	NRST	SL811HST Device active low reset input.
19	OUT	INTRQ	Active high Interrupt Request output to external controller.
20	GND	GND	SL811HST Device Ground.
21	BIDIR	D0	Data 0. Microprocessor Data/(Address) Bus.
22	NC	NC	NC
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	BIDIR	D1	Data 1. Microprocessor Data/(Address) Bus.
28	BIDIR	D2	Data 2. Microprocessor Data/(Address) Bus.
29	BIDIR	D3	Data 3. Microprocessor Data/(Address) Bus.
30	GND	GND	SL811HST Device Ground.
31	BIDIR	D4	Data 4. Microprocessor Data/(Address) Bus.
32	BIDIR	D5	Data 5. Microprocessor Data/(Address) Bus.
33	BIDIR	D6	Data 6. Microprocessor Data/(Address) Bus.
34	NC	NC	NC
35	NC	NC	NC
36	NC	NC	NC
37	NC	NC	NC
38	NC	NC	NC
39	BIDIR	D7	Data 7. Microprocessor Data/(Address) Bus.
40	IN	M/S	Master/Slave Mode select. '1' selects Slave. '0' = Master

41	VDD	+3.3 VDC	SL811HST Device VDD Power.
42	IN	A0	A0 = '0'. Selects Addr. Pointer. Reg.A0 = '1'. Selects Data Buffer or Register. Note 1
43	IN	nDACK	DMA Acknowledge. An active low input used to interface to an external DMA controller. DMA is enabled only in slave mode. In host mode, Pin should be tied High (logic'1')
44	OUT	nDRQ	DMA Request. An active low output used with an external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers. In host mode, Pin must be left unconnected
45	IN	NRD	Read Strobe Input. An active low input used with nCS to read registers/data memory.
46	NC	NC	NC
47	NC	NC	NC
48	NC	NC	NC

- The A0 Address bit is used to access address register or data registers in I/O Mapped or Memory Mapped applications.
- CM Clock Multiplier (SL811HST Only). When a 12 MHz Clock Source is used this pin should be tied to 3.3 VDC. Tie to Gnd for 48 MHz Clock Source. (In SL11H this pin was designated as ALE input).
- VDD can be derived from the USB supply. See diagram.
- The X1/X2 Clock requires external 12 or 48 MHz matching crystal or clock source.

3.7 Package Markings (SL811HST)

YYWW = Date code
XXXX = Product code

4 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This section lists the absolute maximum ratings of the SL811H. Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Storage Temperature	-40 to 125 °C
Voltage on any pin with respect to ground	-0.3 V to 6.0 V
Power Supply Voltage (VDD)	3.3 V ± 10%
Power Supply Voltage (VDD1)	3.3 V ± 10%
Lead Temperature (10 seconds)	180^0 C

Recommended Operating Condition

Parameter	Min.	Typical	Max
Power Supply Voltage, VDD	3.0 V	3.3 V	3.6 V
Power Supply Voltage, VDD1	3.0 V		3.6 V
Operating Temperature	0° C		65° C

Crystal Requirements, (X1, X2)	Min.	Typical	Max
Operating Temperature Range	0° C		65° C
Parallel Resonant Frequency (note 1)		48 MHz	
Frequency Drift over Temperature			+/- 50 ppm
Accuracy of Adjustment			+/- 30 ppm
Series Resistance			100 ohms
Shunt Capacitance	3 pF		6 pF
Load Capacitance		20 pF	
Drive Level	20 uW		5 mW
Mode of Vibration 3rd overtone (note2)			

Note:

- The SL811HS can use a 12 MHz Crystal Oscillator or 12 MHz Clock Source.
- Fundamental mode for 12 MHz Crystal

4.1 External Clock Input Characteristics (X1)

Parameter	Min.	Typical	Max
Clock Input Voltage @ X1 (X2 Open)	1.5 V		
Clock Frequency *		48 MHz	

* The SL811HS can use a 12 MHz Clock Source

4.2 DC Characteristics

Symbol	Parameter	Min.	Typical	Max
V_{IL}	Input Voltage LOW	-0.3 V		0.8 V
V_{IH}	Input Voltage HIGH (5V Tolerant I/O)	2.0 V		6.0 V
V_{OL}	Output Voltage LOW(IoL=4ma)			0.4V
V_{OH}	Output Voltage HIGH(IoH=-4ma)	2.4 V		
I_{OH}	Output Current HIGH	4 mA		
I_{OL}	Output Current LOW	4 mA		
I_{LL}	Input Leakage			+/- 1 uA
C_{IN}	Input Capacitance			10 pF
I_{CC}	Supply Current (VDD) inc USB @FS		21 mA	25 mA
I_{CCsus1}	Supply Current (VDD) Suspend w/Clk & Pll Enb		4.2 mA	5 Ma
I_{CCsus2}	Supply Current (VDD) Suspend no Clk & Pll Dis.		50 uA	60 uA
I_{USB}	Supply Current (VDD1)			10 mA
I_{USBSUS}	Transceiver Supply Current in Suspend			10 uA

Note:

- Icc measurement includes USB Transceiver current (Iusb) operating at Full Speed.
- Iccsus1 measured with 12 MHz Clock Input and Internal PLL enabled. Suspend set – (USB transceiver and internal Clocking disabled).
- Iccsus2 measured with external Clock, PLL disabled, and Suspend set. For absolute minimum current consumption, ensure that all inputs to the device are at static logic level.

4.3 USB Host Transceiver Characteristics

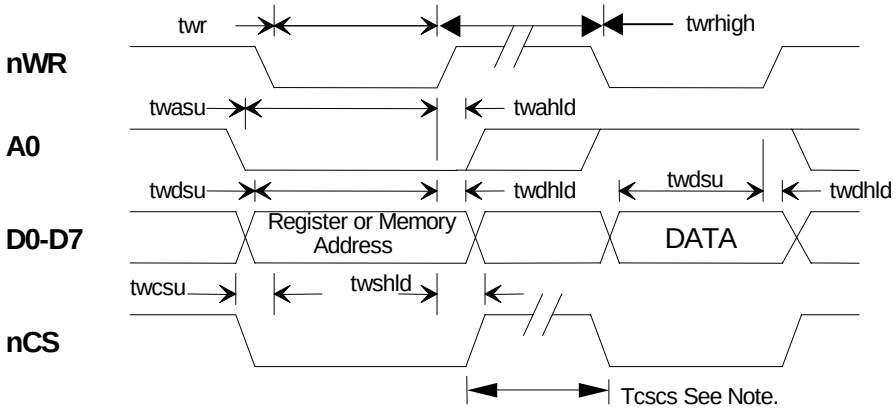
Symbol	Parameter	Min.	Typical	Max
V_{IHYS}	Differential Input Sensitivity (Data+, Data-)	0.2 V		200 mV
V_{USBIH}	USB Input Voltage HIGH Driven	2.0		
V_{USBIL}	USB Input Voltage LOW			0.8 V
V_{USBOH}	USB Output Voltage HIGH	2.0 V		
V_{USBOL}	USB Output Voltage LOW	0.0 V		0.3 V
Z_{USBH}	Output Impedance HIGH STATE	36 Ohms		42 Ohms
Z_{USBL}	Output Impedance LOW STATE	36 Ohms		42 Ohms
I_{USB}	Transceiver Supply p-p Current (3.3V)			10 mA @ FS

Notes:

- All typical values are VDD = 3.3 V and T_{AMB} = 25 ^{0} C.
- Z_{USBX} Impedance Values includes an external resistor of 33 Ohms ± 1%.

4.4 Bus Interface Timing Requirements

I/O Write Cycle



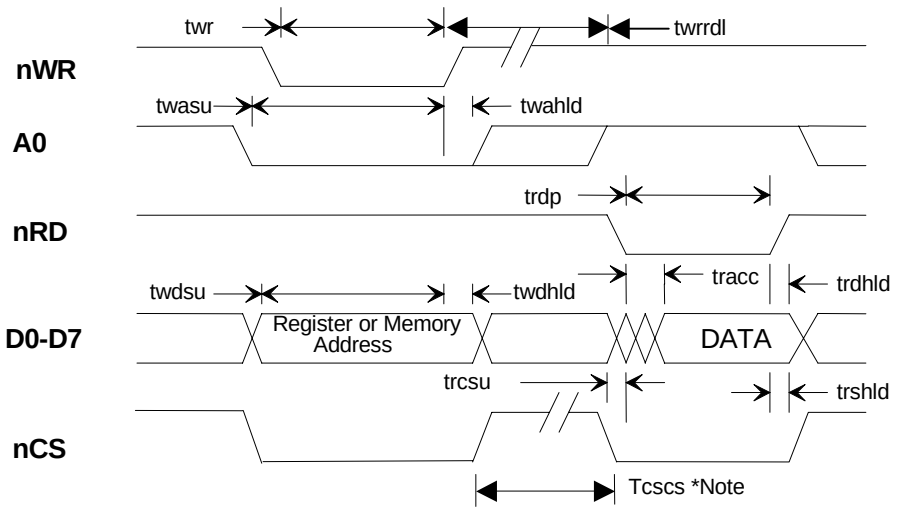
I/O Write Cycle to Register or Memory Buffer

Note: nCS an be held low for multiple write cycles provided nWR is cycled.

Symbol	Parameter	Min.	Typical	Max
twr	Write pulse width	65 ns		
twcsu	Chip select setup to nWR low	0 ns		
twshld	Chip select hold time After nWR high	0 ns		
twasu	A0 address setup time	65 ns		
twahld	A0 address hold time	10 ns		
twdsu	Data to write high setup time	60 ns		
twdhld	Data hold time after write high	5 ns		
tcscs	nCS inactive to nCS* asserted	85 ns		
twrhigh	NWR High	85 ns		

Write Cycle Time for Auto Inc Mode Writes is 150 nsec minimums.

4.5 I/O Read Cycle

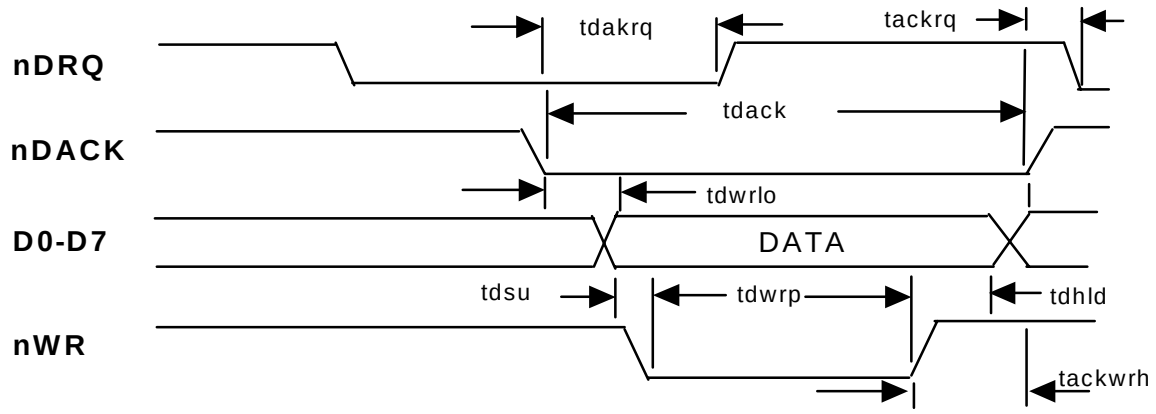


I/O Read Cycle from Register or Memory Buffer

Symbol	Parameter	Min.	Typical	Max
twr	Write pulse width	65 ns		
trd	Read pulse width	65 ns		
twcsu	Chip select setup to nWR	0 ns		
twasu	A0 address setup time	65 ns		
twahld	A0 address hold time	10 ns		
twdsu	Data to write high setup time	10 ns		
twdhld	Data hold time after write high	5 ns		
tracc	Data valid after read low	20 ns		25 ns
trdhld	Data hold after read high	5 ns		
trcsu	Chip select low to read low	0 ns		
trshld	NCS hold after read high	0 ns		
Tcscs*	nCS inactive to nCS *asserted	85 ns		
twrrdl	nWR high to nRD Low	85ns		

Note: NCS can be kept low during multiple read cycles provided nRD is cycled. Rd Cycle Time for Auto Inc Mode Reads is 150 nsec minimum.

4.6 SL811S DMA Write Cycle (SL811 Slave Mode Only)

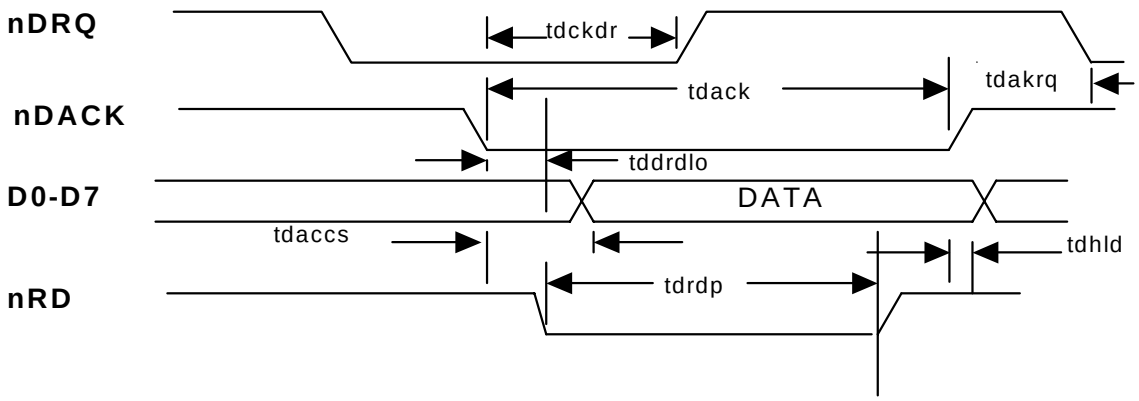


SL811 DMA WRITE CYCLE TIMING

Symbol	Parameter	Min.	Typ.	Max
tdack	nDACK low	65 ns		
tdwrlo	nDACK to nWR low delay	5 ns		
tdakrq	nDACK low to nDRQ high delay	5 ns		
tdwrp	nWR pulse width	65 ns		
tdhld	Data hold after nWR high	5 ns		
tdsu	Data setup to nWR strobe low	60 ns		
tackrq	NDACK high to nDRQ low	5 ns		
tackwrh	NDACK high to nDRQ low	5 ns		
twrcycle	DMA Write Cycle Time	150 ns		

Note: n**WR** must go low after n**DACK** goes low in order for n**DRQ** to clear. If this sequence is not implemented as requested, the next n**DRQ** will be not inserted.

4.7 SL811S DMA Read Cycle (SL811 Slave Mode Only)

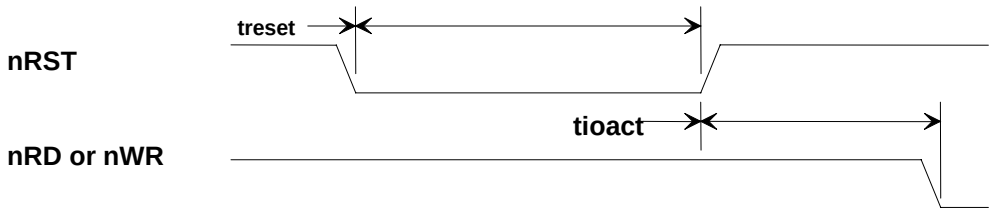


SL811 DMA READ CYCLE TIMING

Symbol	Parameter	Min.	Typ.	Max
tdack	nDACK low	80 ns		
tddrdlo	nDACK to nRD low delay	5 ns		
tdckdr	nDACK low to nDRQ high delay	5 ns		
tdrdp	nRD pulse width	65 ns		
Tdhld Note 1.	Date hold after nDACK high	5 ns		
tddaccs	Data access from nDACK low	65 ns		
tdrdack	nRD high to nDACK high	0 ns		
tdakrq	nDRQ low after nDACK high	5 ns		
trdcycle	DMA Read Cycle Time	150 ns		

Note 1: Data is held until nDACK goes high regardless of state of nREAD

4.8 Reset Timing

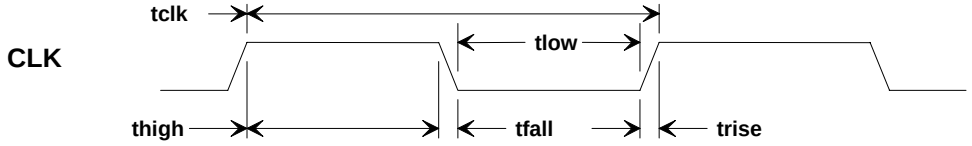


RESET TIMING

Symbol	Parameter	Min.	Typical	Max
treset	nRst Pulse width	16 clocks		
tioact	nRst high to nRD or nWR active	16 clocks		

Note: Clock is 48 MHz nominal.

Clock Timing Specifications



CLOCK TIMING

Symbol	Parameter	Min.	Typical	Max
tclk	Clock period (48 MHz)	20.0 ns	20.8 ns	
thigh	Clock high time	9 ns		11 ns
tlow	Clock low time	9 ns		11 ns
trise	Clock rise time			5.0 ns
tfall	Clock fall time			5.0 ns
	Clock Duty Cycle	45%		55%