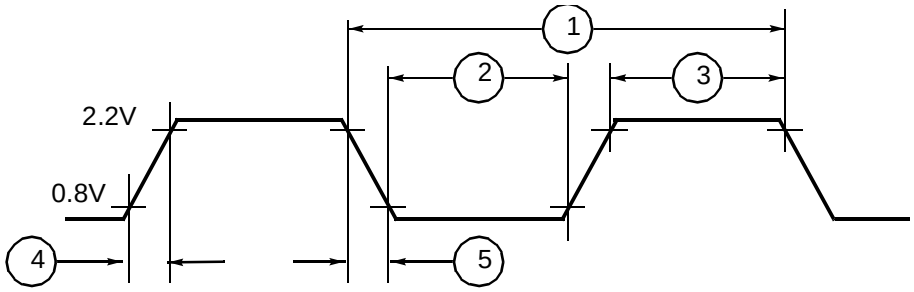
3.12
AC Parameters

This addendum contains waveforms that describe the behavior of the CY7C960/961/ CY7C964 interface for a variety of transaction types and timings. A table of AC parameters is referenced to the waveforms. Note that “T” refers to the CLK input period. Note also that parameters are not indicated on the waveforms everywhere they apply. These waveforms were captured during in-system simulation and reflect accurately the behavior that can be expected.

Clock Input



Num.	Characteristic	Min.	Max.
	Frequency of Operation (MHz)	30	80
1	Cycle Time (ns)	12.5	33.3
2, 3	Clock Pulse Width (Measured from 1.5V to 1.5V)	Note 1	Note 1
4, 5	Rise and Fall Time (ns)	—	5

Note:

1. A 60/40 to 40/60 duty cycle must be maintained.

Table 3-16. AC Parameters

Parameter	Description	Min	Max	Reference	Notes
p1	DECODE Delay	2T	5T		2
p2	RAS*/CAS* Delay	2T	9T		2
p3	CAS* Width/DBE Width	3T	18T		2, 7
p4	CAS* Precharge	1T	8T		2
p5	RAS* Precharge	5T	12T		2
t2	LD to D		19 ns	Waveform 5	3
t3	A to LA		20 ns	Waveform 5	3
t4	D to LD		22 ns	Waveform 20	3

Table 3-16. AC Parameters (continued)

Parameter	Description	Min	Max	Reference	Notes
t5	LD to A Propagation Delay		22 ns	Waveform 11	3
t7	ABEN* falling to A Output Enable Delay		12 ns	Waveform 11	3
t8	DENO* falling to D Output Enable Delay		16 ns	Waveform 5	3
t9	ABEN* falling to D Output Enable Delay		17 ns	Waveform 11	3
t11	LAEN rising to LA		12 ns	Waveform 18	3
t12	DENIN* falling to LD Output Enable Delay		18 ns	Waveform 9	3
t13	DENIN1* falling to LD Output Enable Delay		21 ns	Waveform 23	3
t15	ABEN* rising to A High-Z		12 ns	Waveform 22	3
t16	DENO* rising to D High-Z		15 ns	Waveform 3	3
t17	ABEN* rising to D High-Z		15 ns	Waveform 22	3
t19	LAEN falling to LA High-Z		15 ns	Waveform 18	3
t20	DENIN* rising to LD High-Z		18 ns	Waveform 9	3
t23	A valid to VCOMP* falling		21 ns	Waveform 3	3
t25	LD set-up to LEDO rising	7 ns		Waveform 22	3
t26	LD hold to LEDO rising	0 ns		Waveform 22	3
t28	LD set-up to DENO* falling	0 ns		Waveform 22	3
t29	LD hold to DENO* falling	7 ns		Waveform 22	3
t37	A, D set-up to LEDI rising	7 ns		Waveform 23	3
t38	A, D hold after LEDI rising	0 ns		Waveform 23	3
t45	LD set-up to STROBE rising	5 ns			3
t46	LD hold after STROBE rising	5 ns			3
t74	LDS rising to LD valid		24 ns	Waveform 23	3
t75	LDS falling to LD valid		24 ns	Waveform 23	3
t138	LADI falling to LA[31:8] valid		18 ns	Waveform 18	3
s1	CLK period	12.5ns	33.3ns	Waveform 4	
s2	CLK pulse width	5 ns		Waveform 4	
s3	AS* falling edge to CS	p1 + 1T	p1 + 2T	Waveform 1	
s4	DSA* falling edge to CS	1T	2T	Waveform 4	
s5	AS* falling edge to REGION valid		p1 – 1T	Waveform 18	
s6	AS* falling edge to RAS* falling	2T	3T	Waveform 6	
s7	ROW set-up to RAS* falling	1T		Waveform 3	
s8	PREN* falling to PCLK rising	80T		Waveform 26	
s9	COL set-up to CAS*, DBE falling	1T		Waveform 3	
s10	ROW deassertion to CAS* falling, DBE	1T		Waveform 6	
s11	LACK* rising set-up to prevent CAS* falling		p2 – 1T	Waveform 25	4
s12	LACK* falling to CAS* falling,DBE	2T	3T	Waveform 25	
s13	DSA* falling to CAS* falling,DBE	3T	4T	Waveform 4	
s14	SWDEN* set-up to CAS* falling,DBE	1T		Waveform 12	

Table 3-16. AC Parameters (continued)

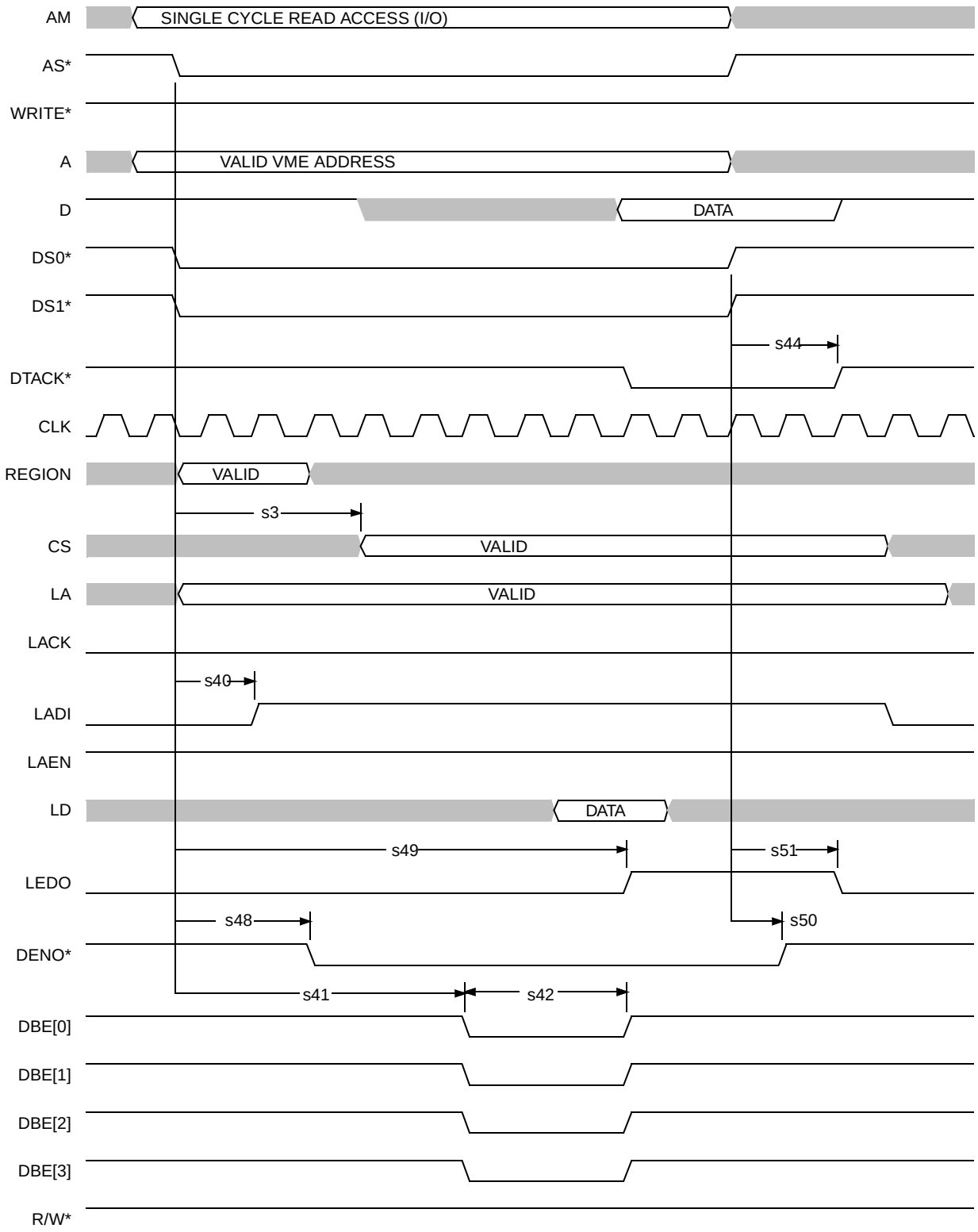
Parameter	Description	Min	Max	Reference	Notes
s15	SWDEN* hold after CAS* rising,DBE	0		Waveform 12	
s16	LA set-up to CAS* falling, DBE	1T		Waveform 12	
s17	LA hold after CAS* rising, DBE	0		Waveform 12	
s18	RAS*,COL,LAEN,R/W* hold after CAS* rising, DBE	1T		Waveform 12	
s19	DSA* falling to DTACK* falling	2T	3T	Waveform 20	
s20	RAS*,COL,LADI hold after AS* rising	2T	3T	Waveform 3	
s21	CAS* falling, DBE to DTACK* falling (read)	p3		Waveform 3	7
s22	CAS* falling, DBE to DTACK* falling (write)	p3 + 1T		Waveform 4	7
s23	DSA* rising to CAS* falling, DBE	2T	3T	Waveform 14	
s24	DSA* falling to CAS* falling,DBE	3T	4T	Waveform 16	
s25	WRITE* falling to R/W* falling		1T	Waveform 4	
s26	LACK* falling to DBE deassert	3T	4T	Waveform 24	
s27	LACK* set-up to DBE assert	0		Waveform 24	
s28	LD set-up to DBE deassert (read)	5 ns		Waveform 6	
s29	LD hold after DBE deassert (read)	5 ns		Waveform 6	
s30	LD set-up to DBE assert (write)	1T		Waveform 11	
s31	LD hold after DBE deassert (write)	0 ns		Waveform 11	6
s32	AM valid to DENIN*,DENIN1* falling	1T	2T	Waveform 9	
s33	DSA* rising to DENIN*,DENIN1* rising	1T	2T	Waveform 9	
s34	PREN* falling to PDATA valid		39T	Waveform 26	5
s35	PCLK period	1000T		Waveform 26	5
s36	PDATA set-up to PCLK falling	1T		Waveform 26	5
s37	PDATA hold after PCLK falling	3T		Waveform 26	5
s38	IACKIN* falling to LDEN* falling	2T	3T	Waveform 7	
s39	LDEN* falling to DTACK* falling	6T		Waveform 7	
s40	AS* falling to LADI rising	1T	2T	Waveform 1	
s41	AS* falling to DBE assertion	5T + p1	6T + p1	Waveform 1,2	
s42	DBE asserted width	p3		Waveform 1,2	7
s43	WRITE High to R/W* High		1T	Waveform 4	
s44	DSB High to DTACK* High	1T	2T	Waveform 1,2	
s45	AS* High to LADI High	1T	2T	Waveform 2	
s46	AS* High to CS deasserted	1T	2T	Waveform 2	
s47	AS* falling to DENIN* asserted	T + p1	2T + p1	Waveform 2	
s48	DSA* falling to DENO* asserted	2T + p1	3T + p1	Waveform 1	
s49	DSA* falling to LEDO rising	3T + p1 + p3	4T + p1 + p3	Waveform 1	7
s50	DSA* rising to DENO* rising	0	1T	Waveform 1	
s51	DSA* rising to LEDO falling	1T	2T	Waveform 1	

Table 3-16. AC Parameters (continued)

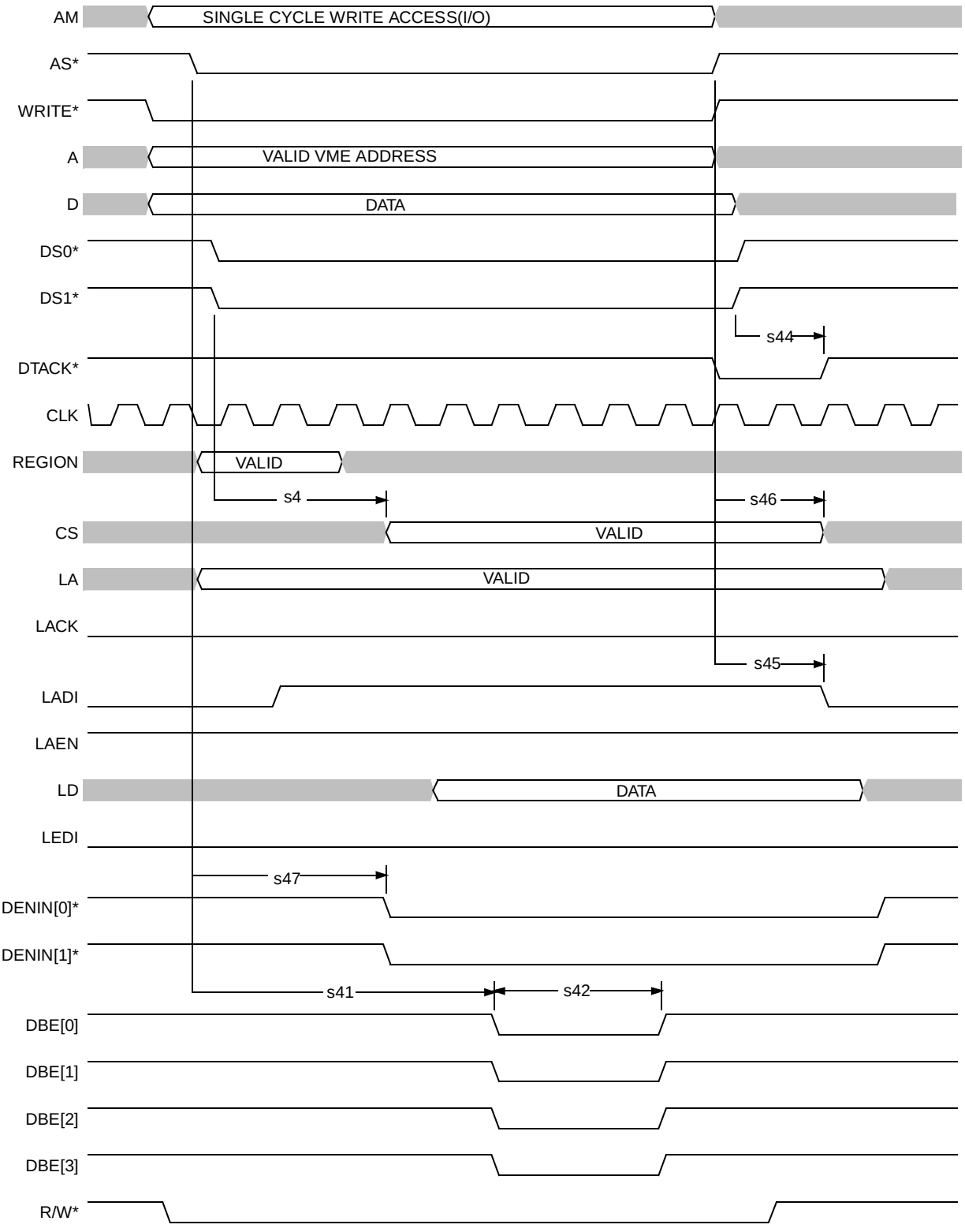
Parameter	Description	Min	Max	Reference	Notes
s52	RAS* rising to CAS* falling (Refresh)	(p5 – 3)T		Waveform 13	
s53	CAS* falling to RAS* falling (Refresh)	1T		Waveform 13	
s54	RAS* falling to CAS* rising (Refresh)	(p3 – 1)T		Waveform 13	
s55	CAS* rising to RAS* rising (Refresh)	(p5 – 3)T		Waveform 13	
s56	RAS* Precharge (Refresh)	(p5 – 2)T		Waveform 13	
s57	RAS* cycle time (Refresh)	(p3 + 2p5 – 5)T		Waveform 13	
s58	RAS* Precharge	p5		Waveform 13	
s59	AS* falling to REGION hold	3T		Waveform 18	
s60	LIRQ* to IRQ*	0	1T	Waveform 8	
s61	R/W*, LA, LD set-up to SELECTLM* falling	10 ns		Waveform 21	
s62	R/W*, LA, LD hold after SELECTLM* rising	0 ns		Waveform 21	
s63	SELECTLM* falling to LD valid	2T	3T	Waveform 21	
s64	SELECTLM* rising to LD Z	2T	3T	Waveform 21	
s65	LACK rising to LBERR* High	0	1T	Waveform 21	
s66	SELECTLM* falling to LBERR* falling	1T	2T	Waveform 21	
s67	SELECTLM* rising to LBERR* rising	1T	2T	Waveform 21	
s68	LACK falling to LBERR* Z	0	1T	Waveform 21	
s69	SELECTLM* minimum assertion	8T		Waveform 21	
s70	SYSRESET* falling to PREN falling			Waveform 19	
s71	PREN* pulse width			Waveform 19	
s72	SYSRESET* rising to IRQ* falling			Waveform 19	

Notes:

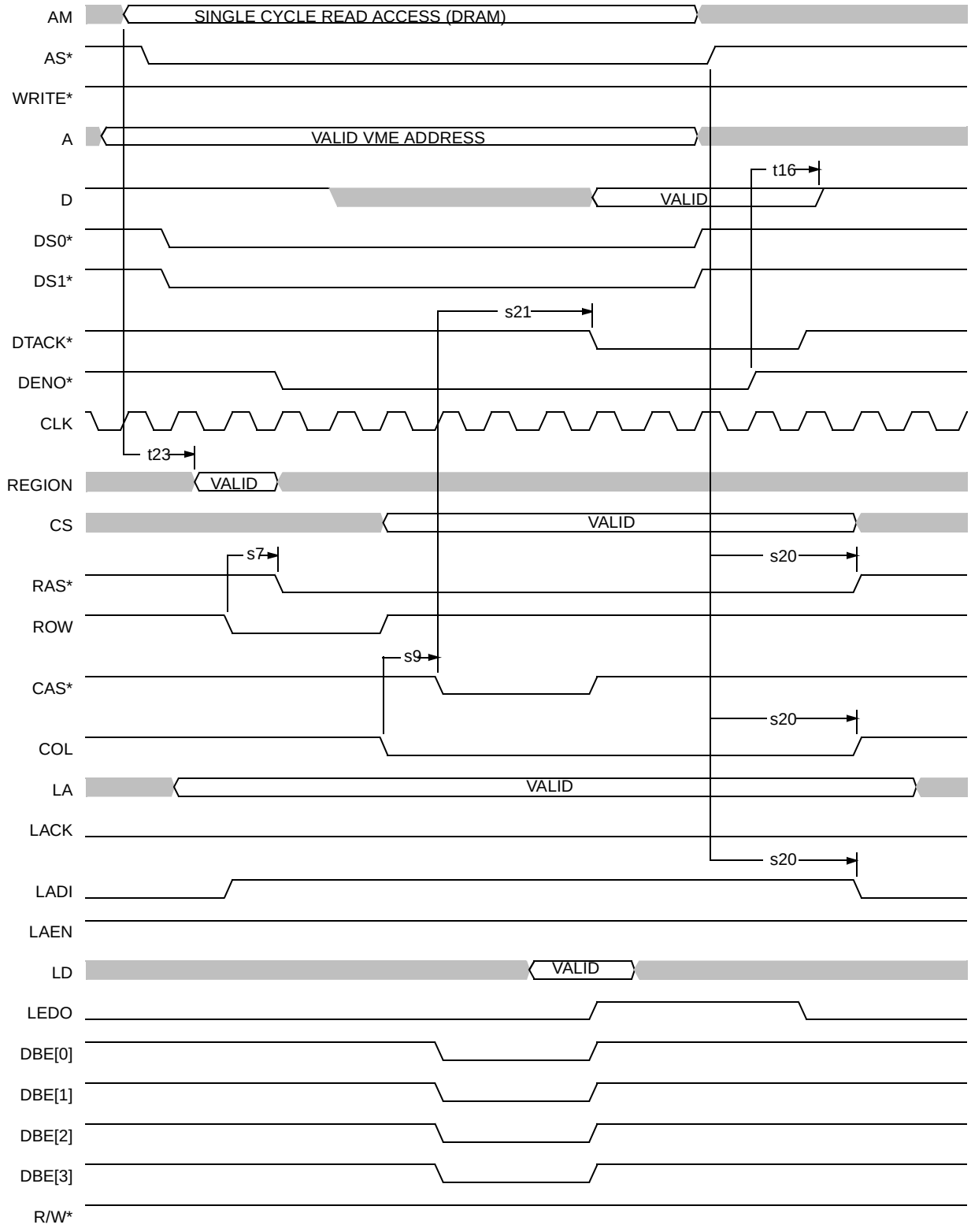
2. This parameter is a constant set when the CY7C960 is programmed at initialization.
3. This parameter is a CY7C964 performance parameter.
4. This parameter is timed from RAS falling and specifies the latest deassertion of LACK to inhibit the CAS burst.
5. This parameter applies when CY7C960 is sourcing PCLK.
6. Hold time is guaranteed by CY7C964 delay from LEDI, DENIN*, or LDS to LD. The CY7C960/CY7C964 design favors falling edge capture of data. LA, LD, and DBE differential delay must be carefully managed for rising edge capture.
7. p3 represents two independent programmable fields. CAS Assert width applies for DRAM access. DBE width is a program set. A unique value is associated with each “region” I/O access.



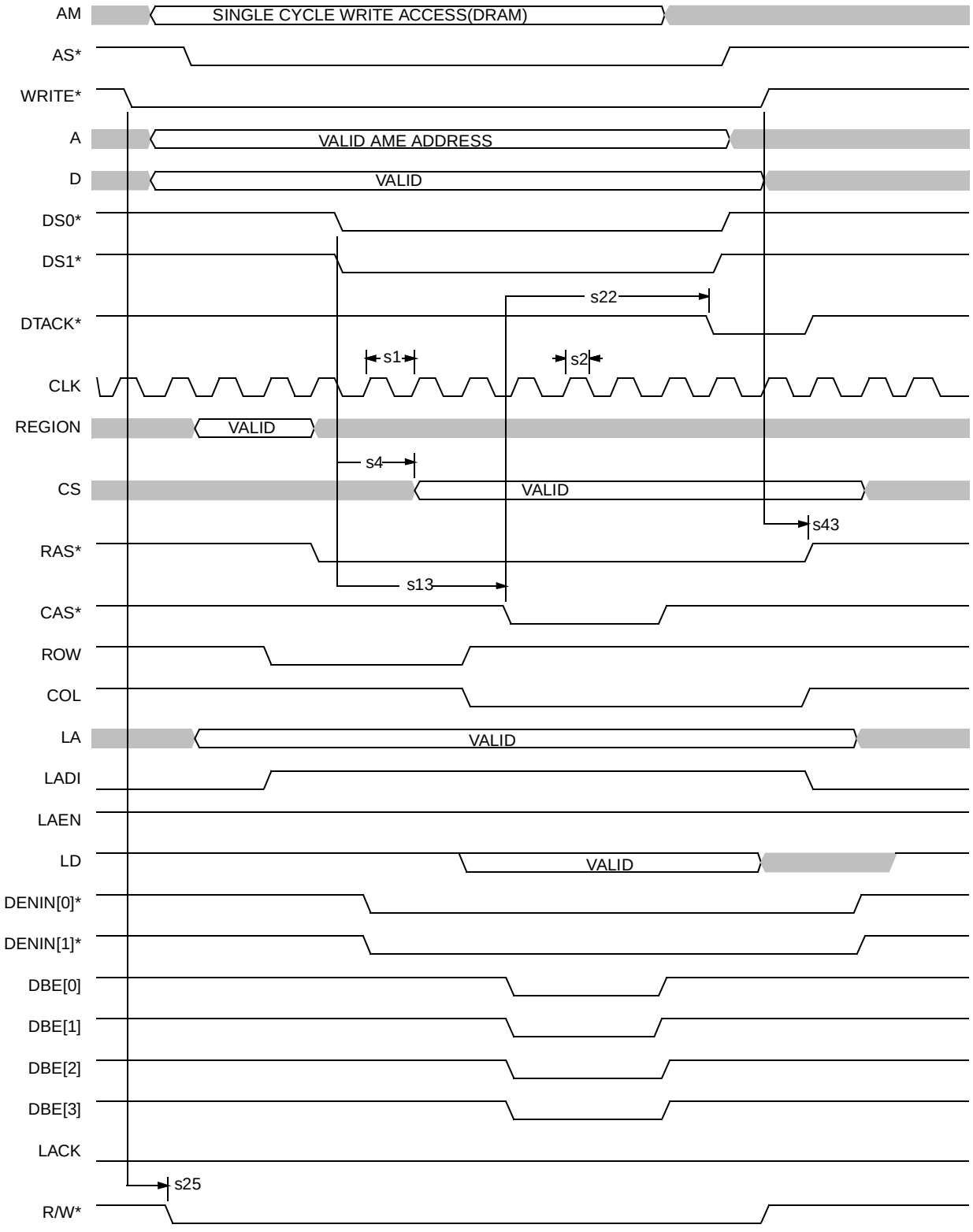
Waveform 1. Single Cycle Read Access (I/O Mode)



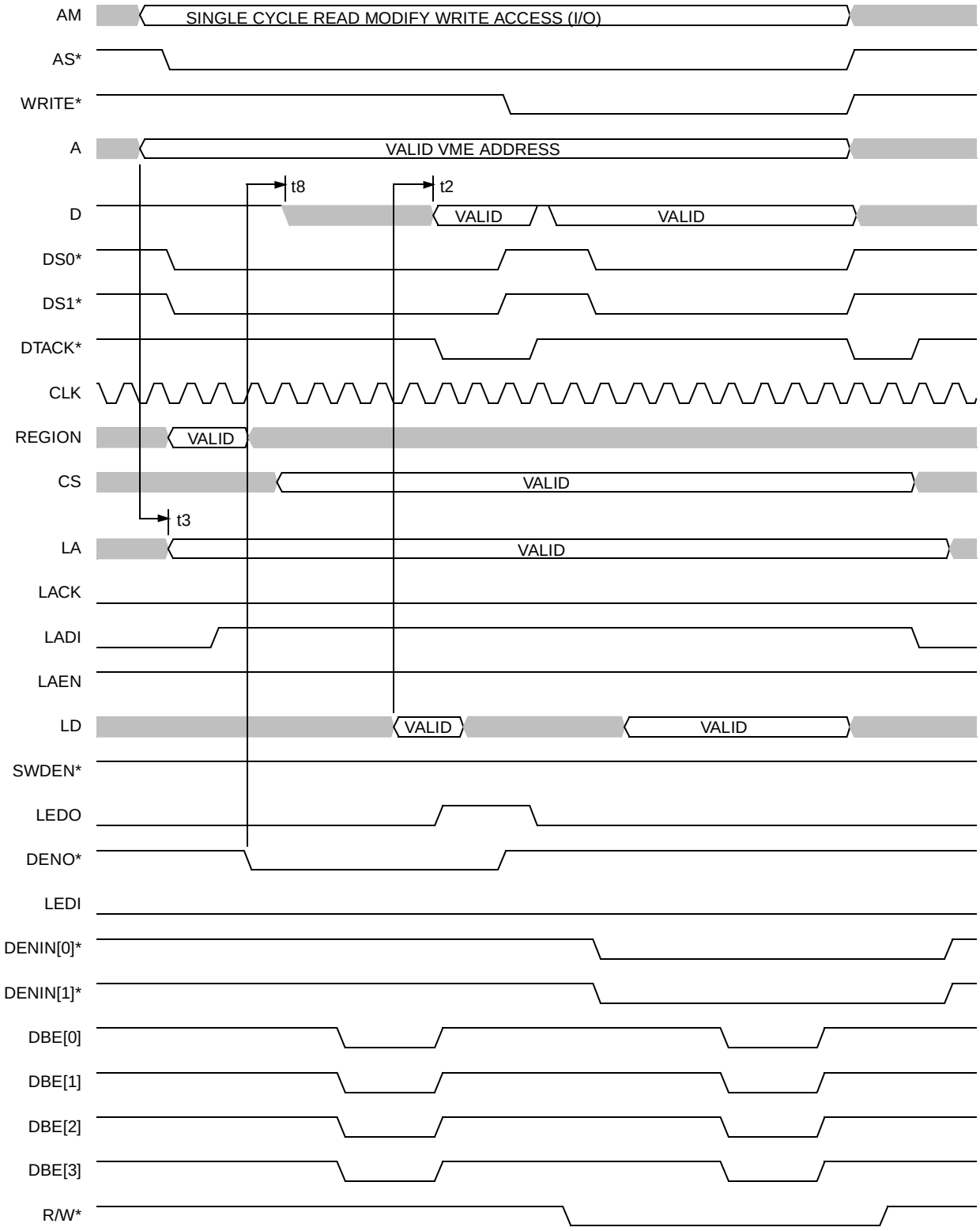
Waveform 2. Single Cycle Write Access (I/O Mode)



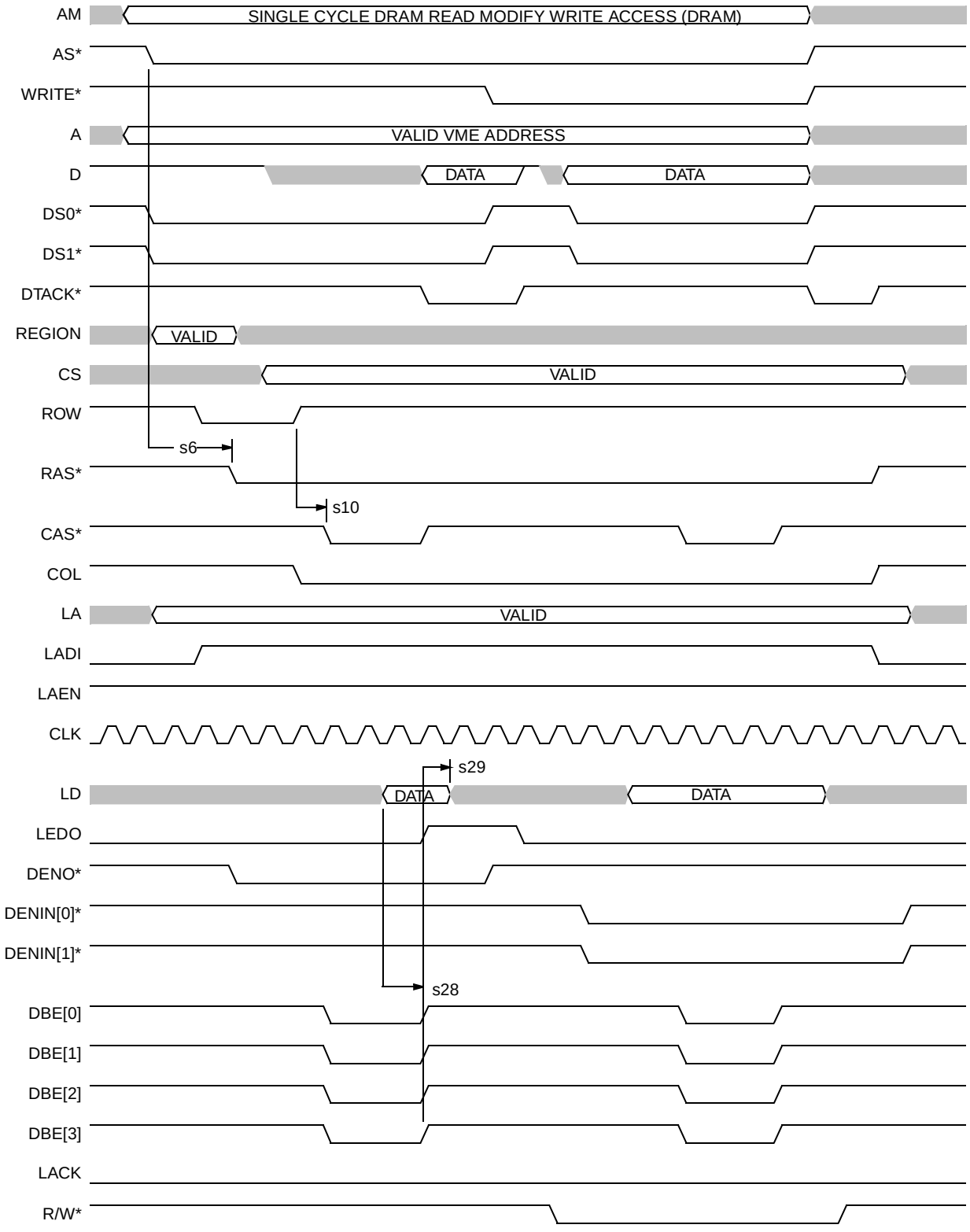
Waveform 3. Single-Cycle Read Access (DRAM Mode)



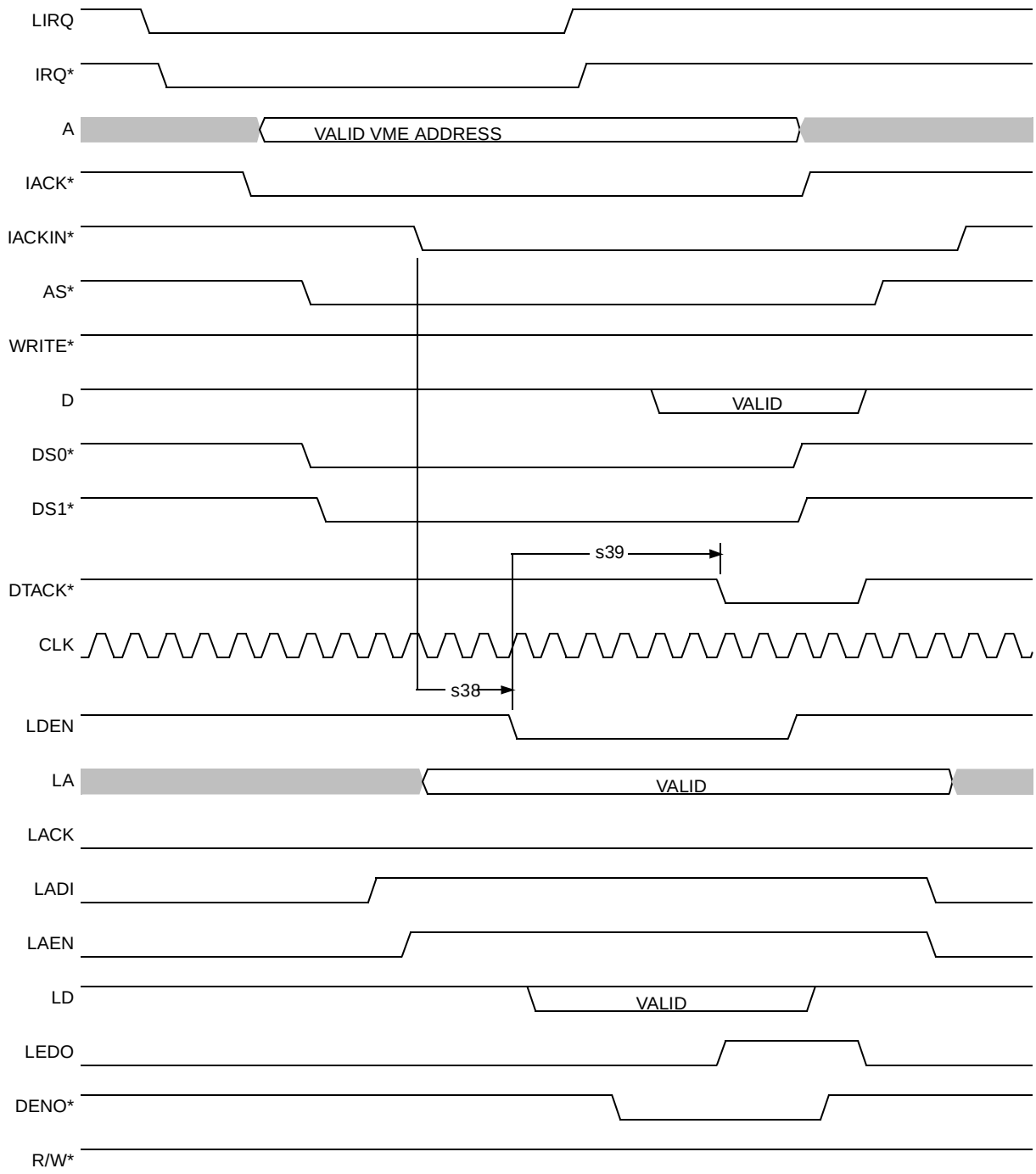
Waveform 4. Single Cycle Write Access (DRAM Mode)



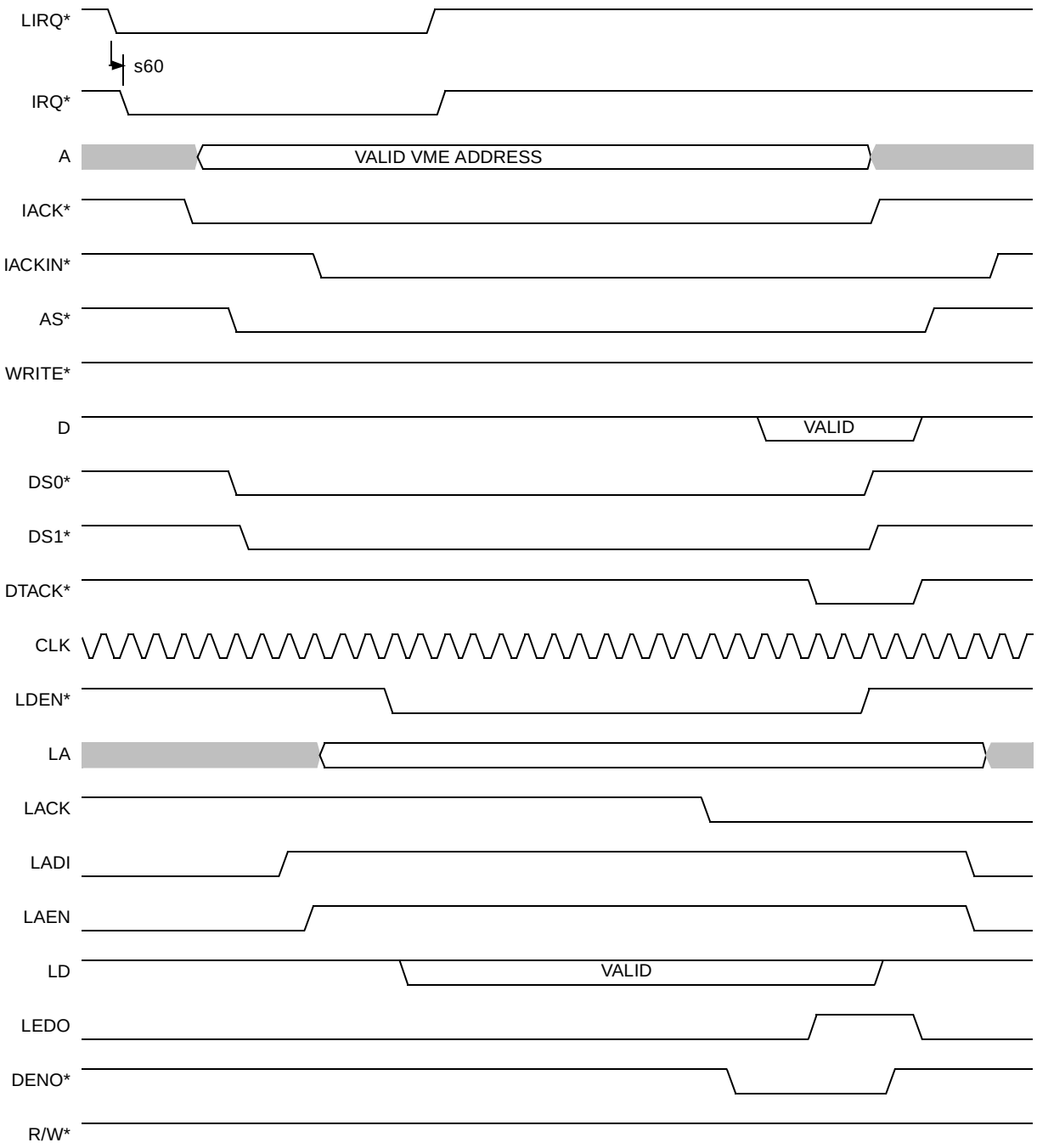
Waveform 5. Single-Cycle Read-Modify-Write Access (I/O Mode)



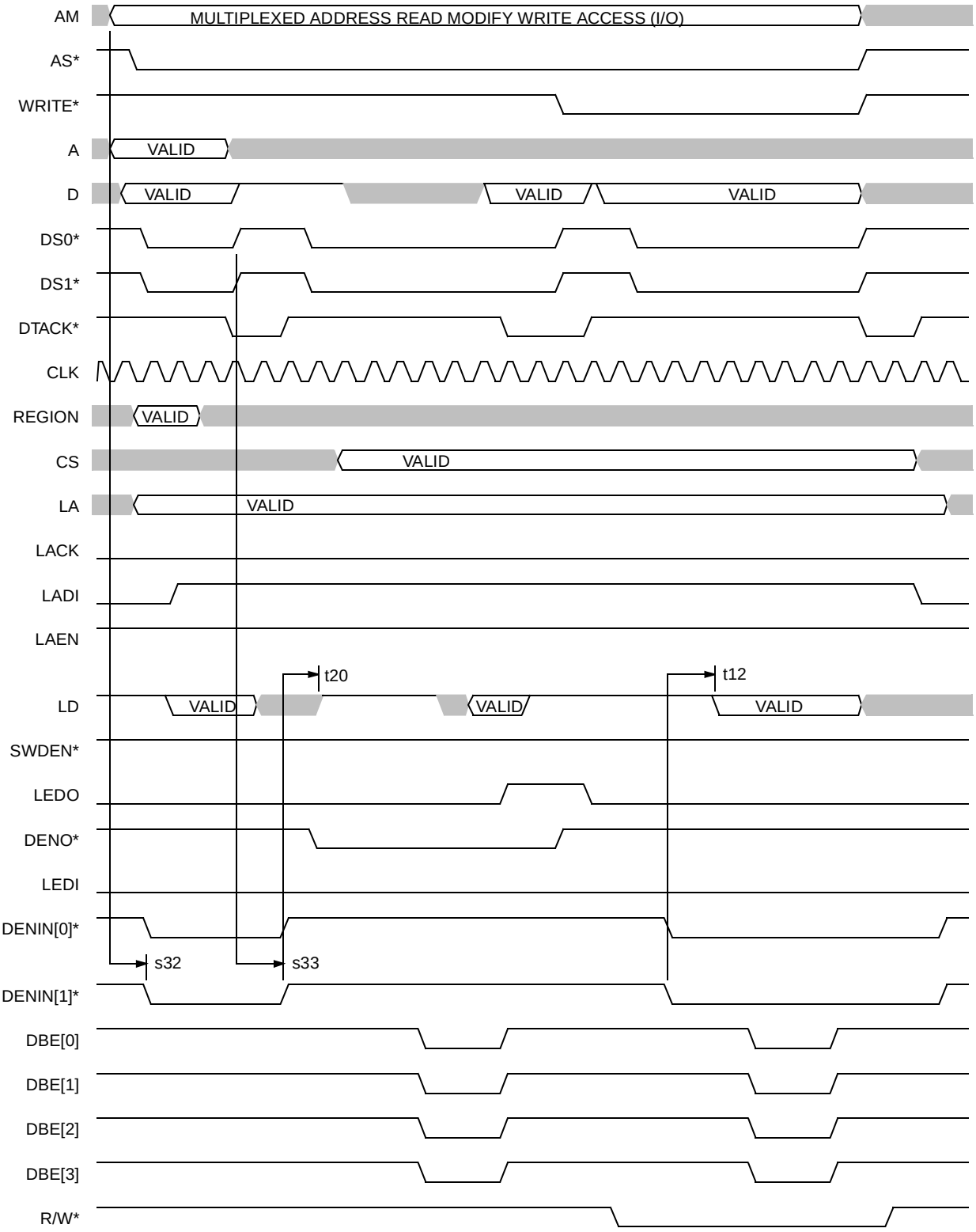
Waveform 6. Single-Cycle Read-Modify-Write Access (DRAM Mode)



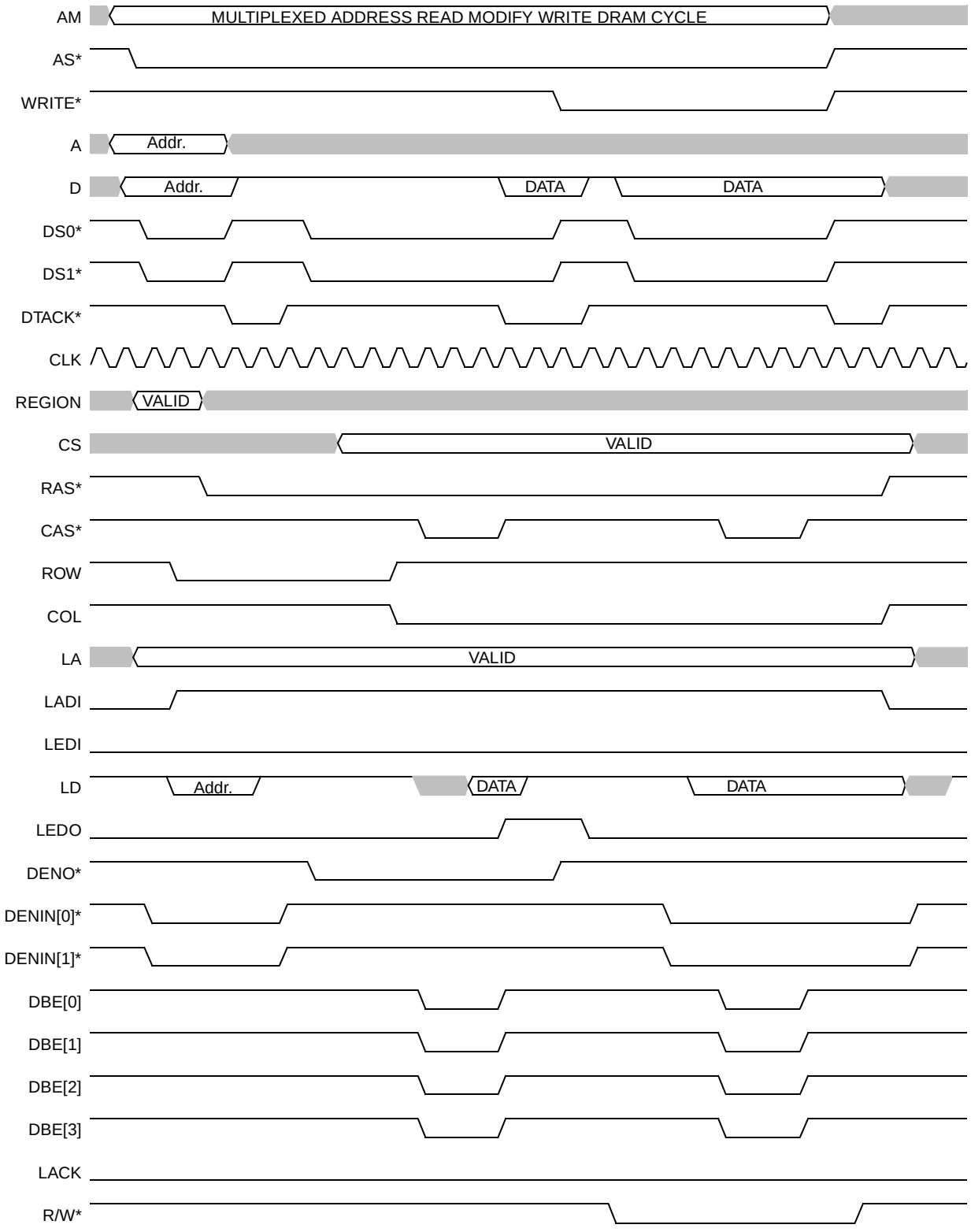
Waveform 7. IACK CYCLE Self-timed



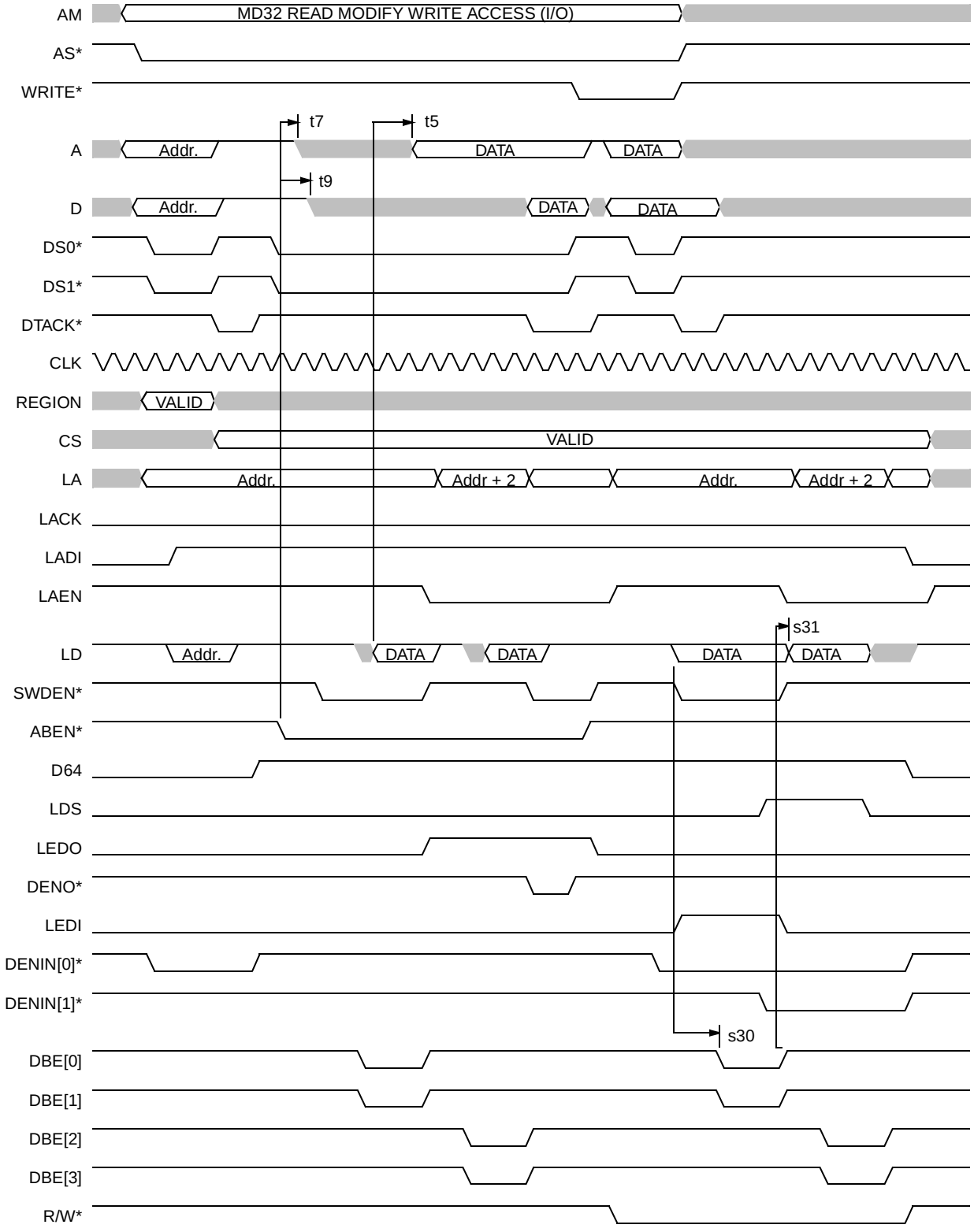
Waveform 8. IACK Cycle Handshake



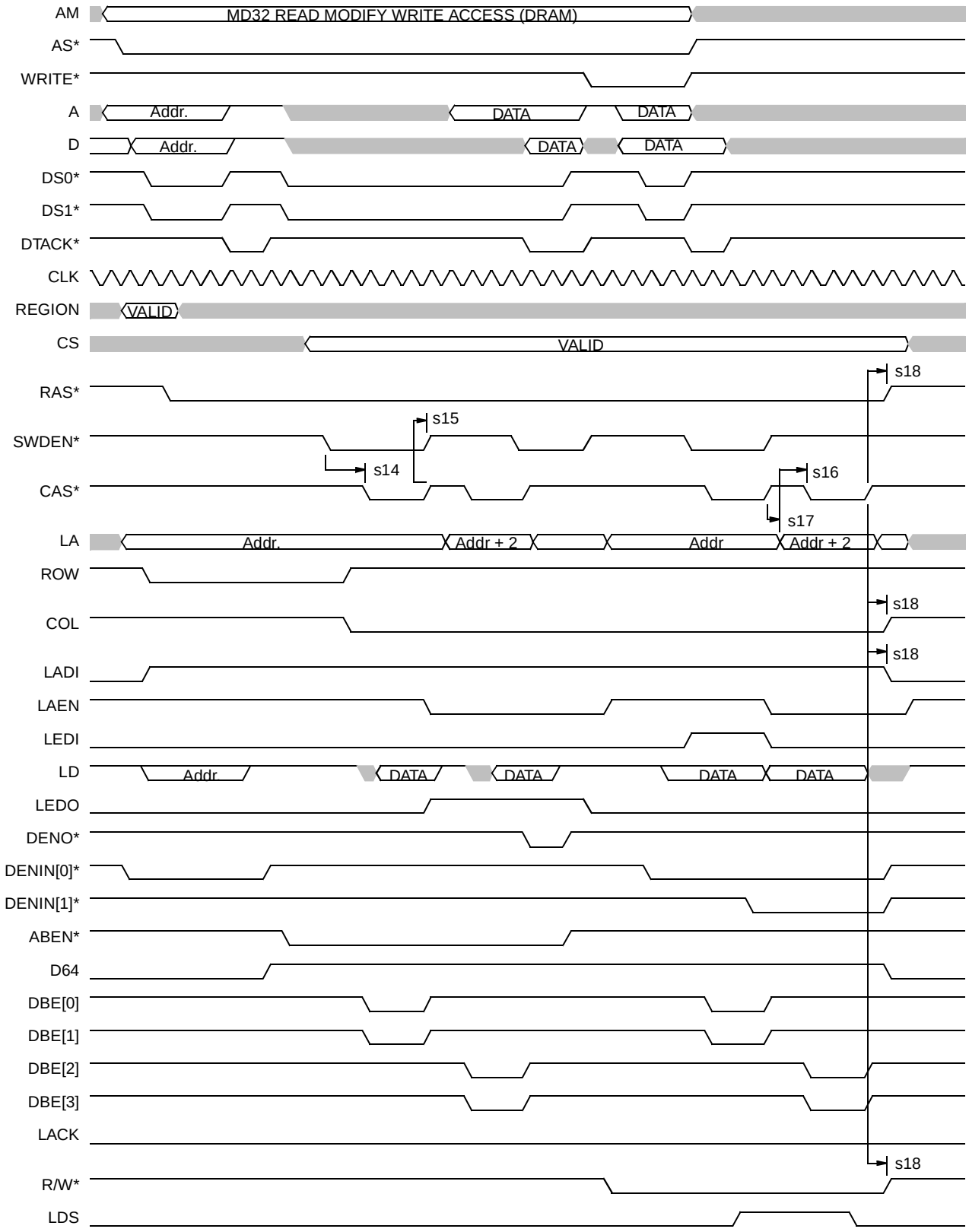
Waveform 9. Multiplexed Address Read-Modify-Write Access (I/O Mode)



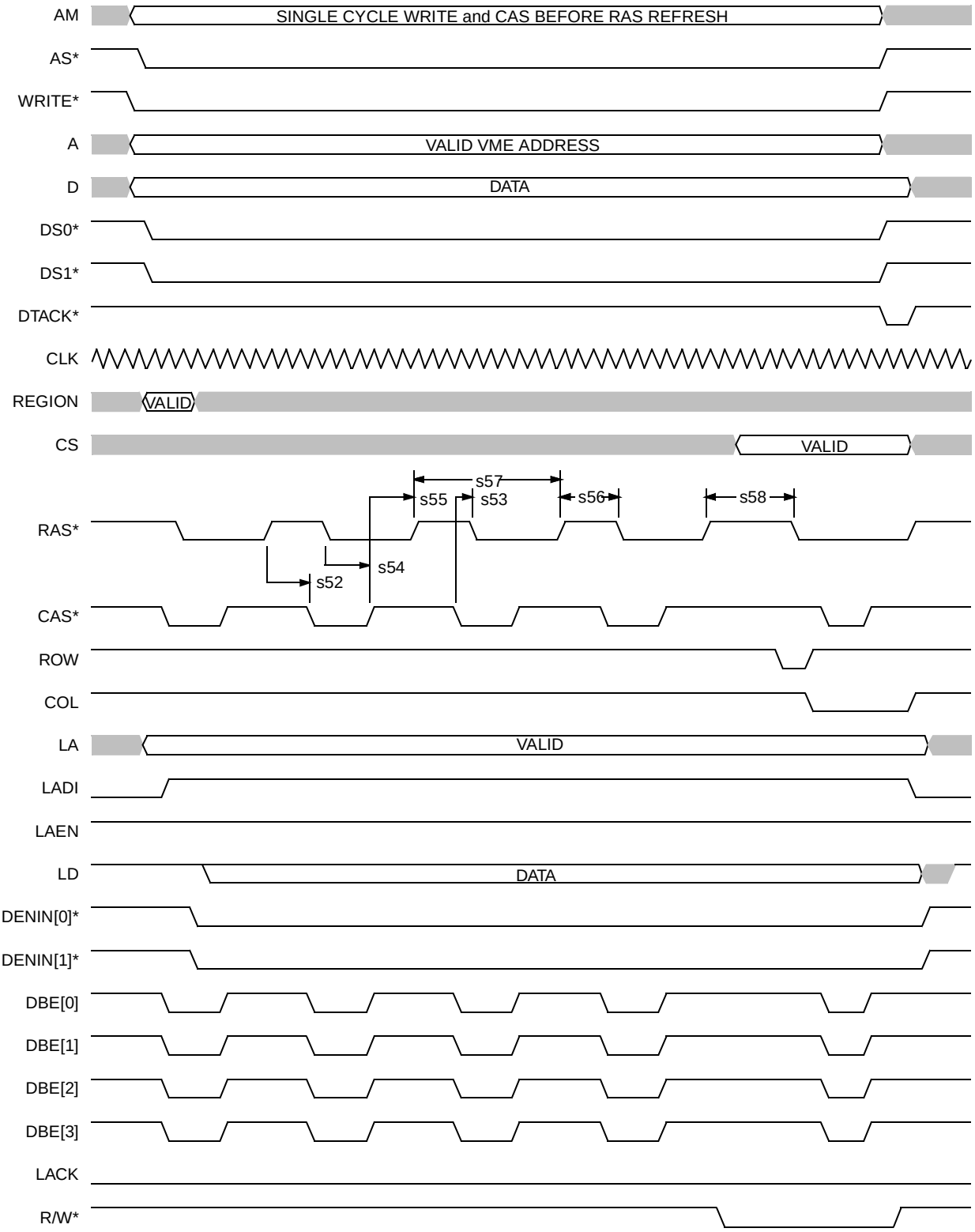
Waveform 10. Multiplexed Address Read-Modify-Write Access (DRAM Mode)



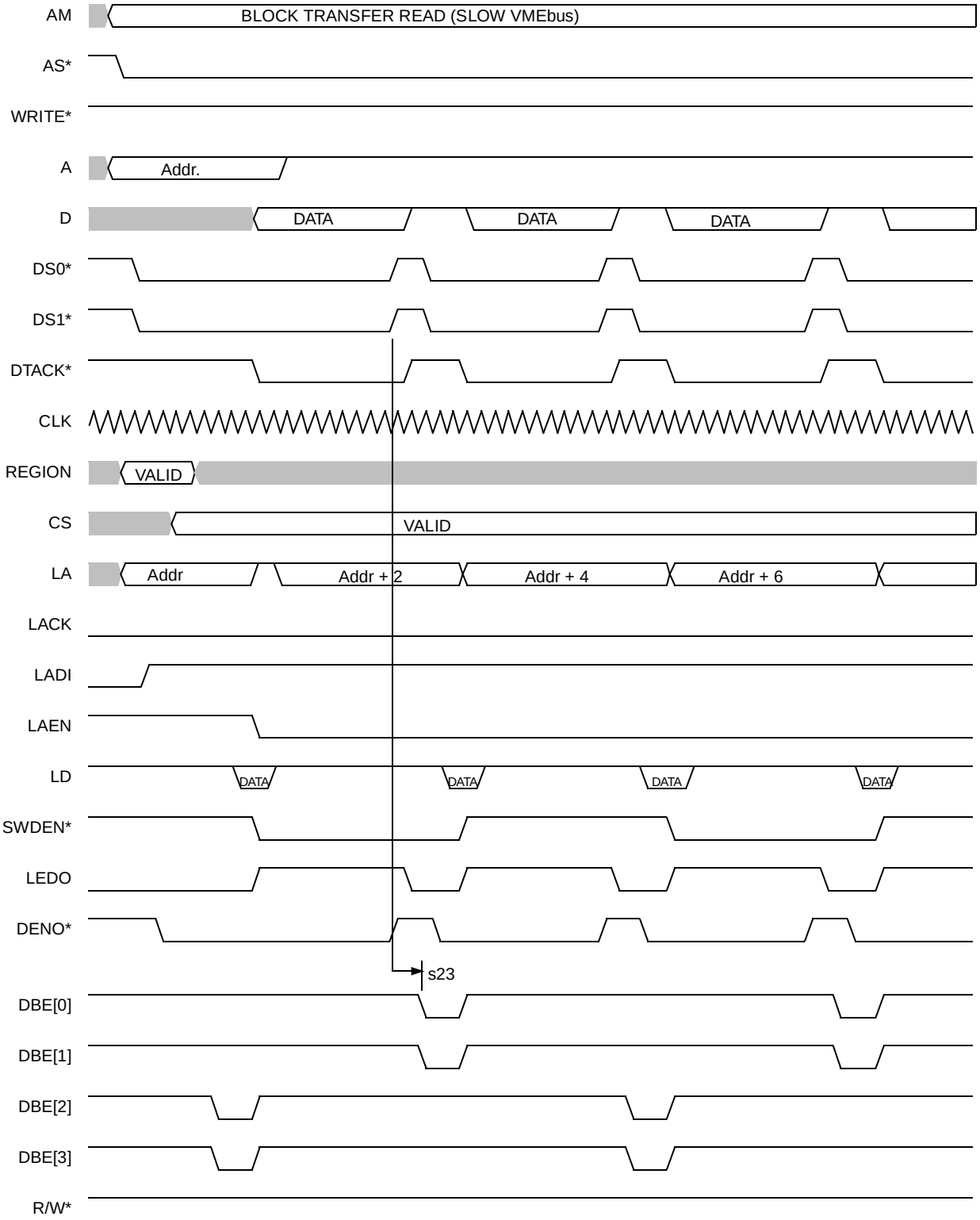
Waveform 11. MD32 Read-Modify-Write Access (I/O Mode)



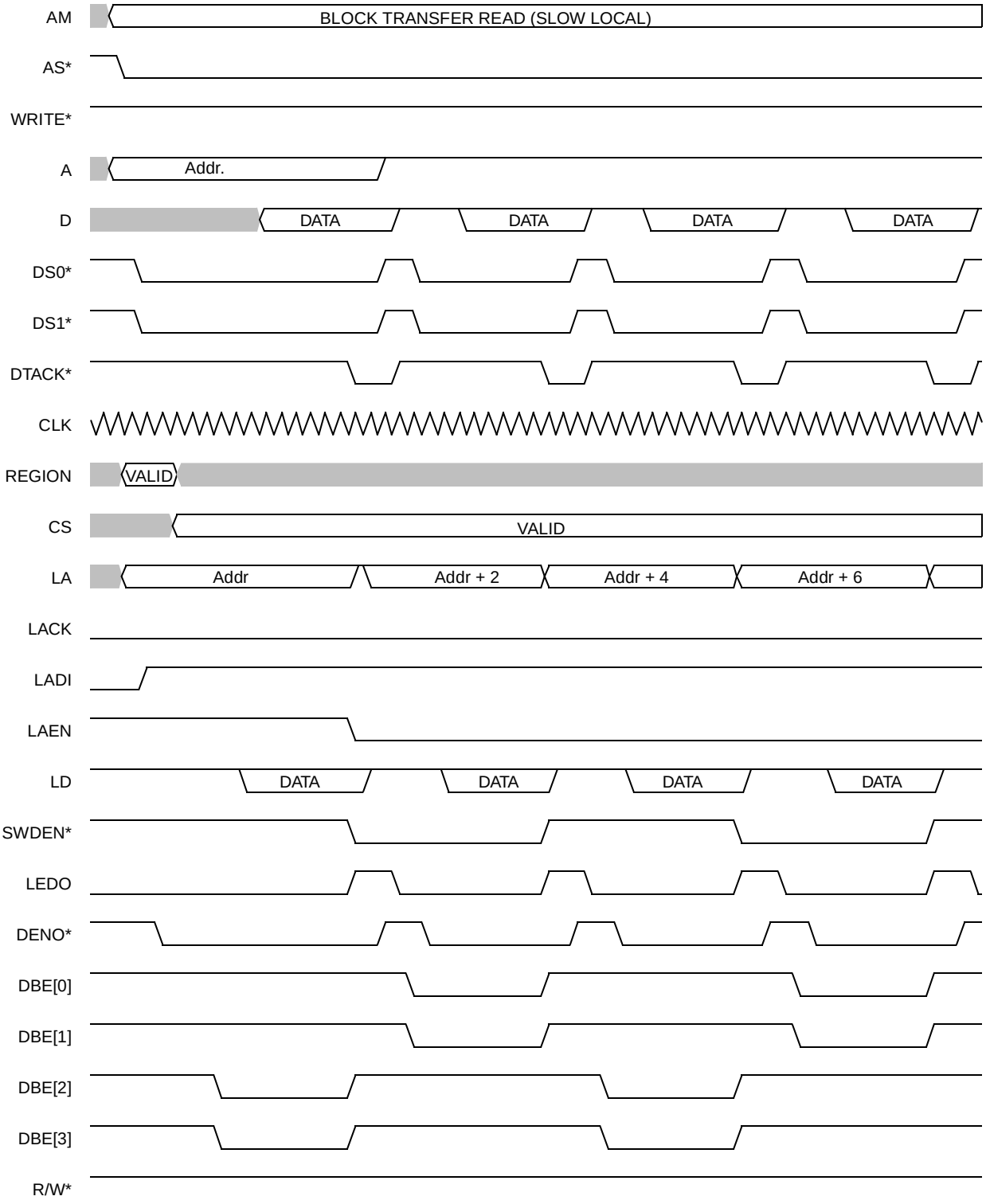
Waveform 12. MD32 Read-Modify-Write Access (DRAM Mode)



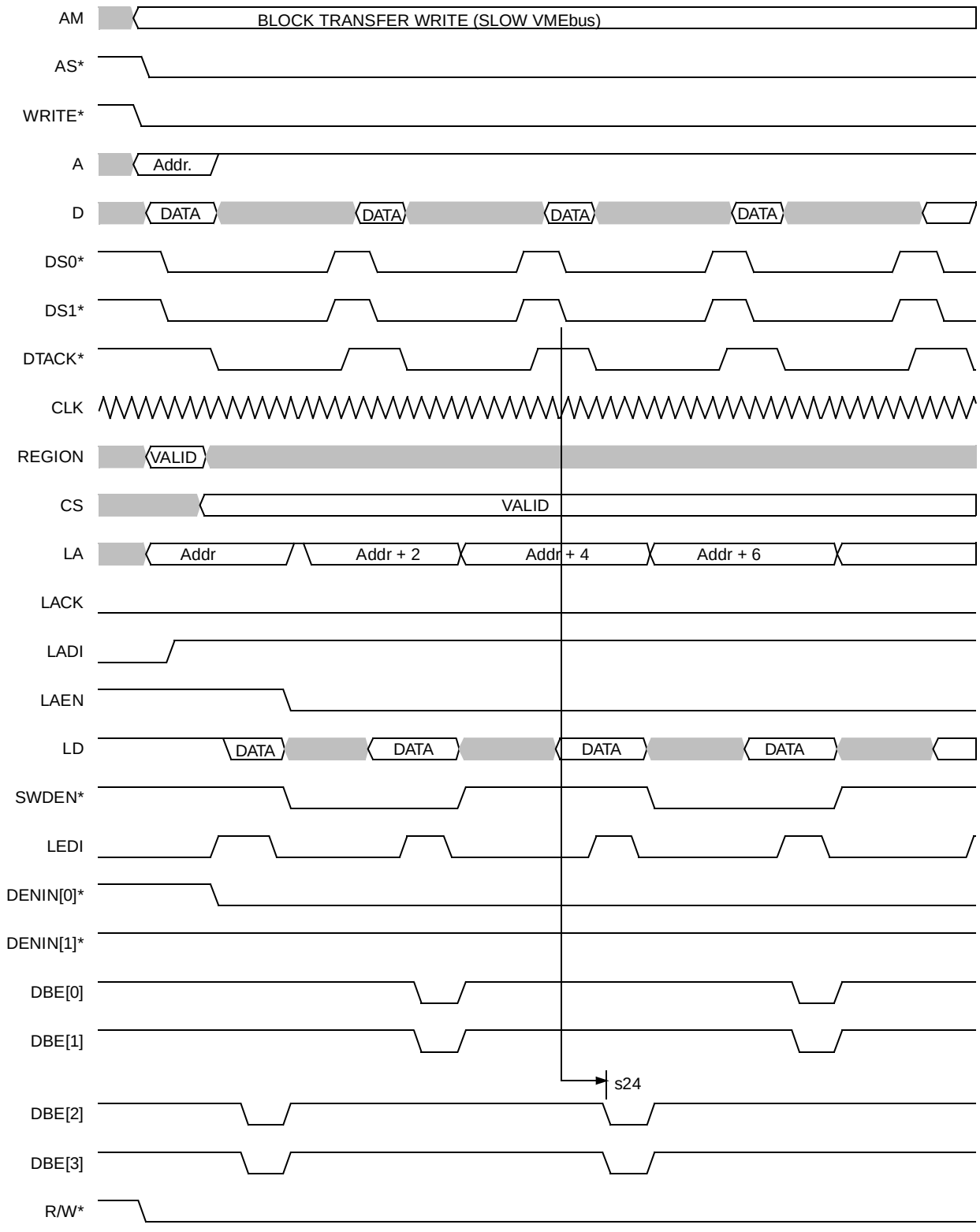
Waveform 13. Single-Cycle Write and CAS before RAS Refresh



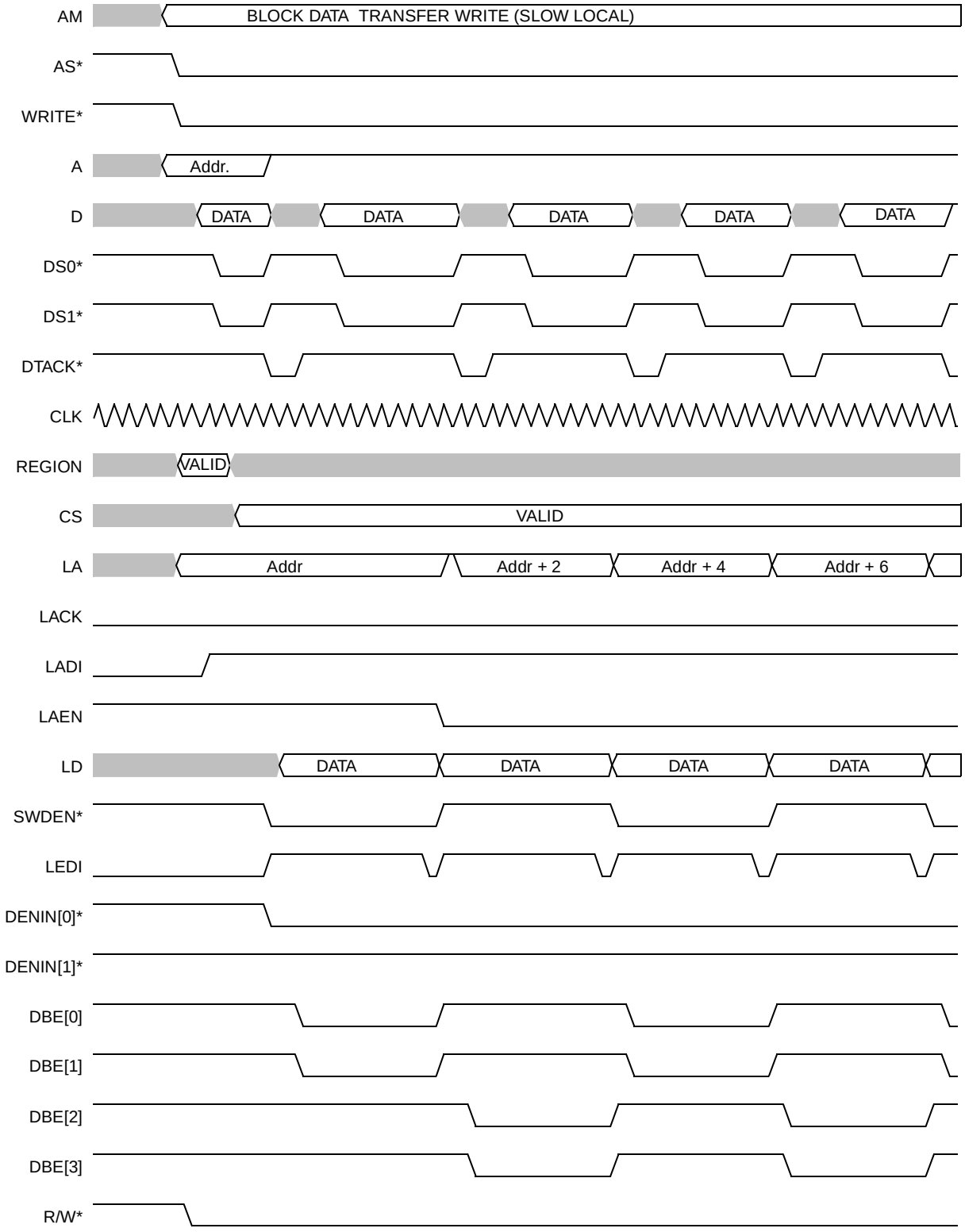
Waveform 14. Block Transfer Read (Slow VME)



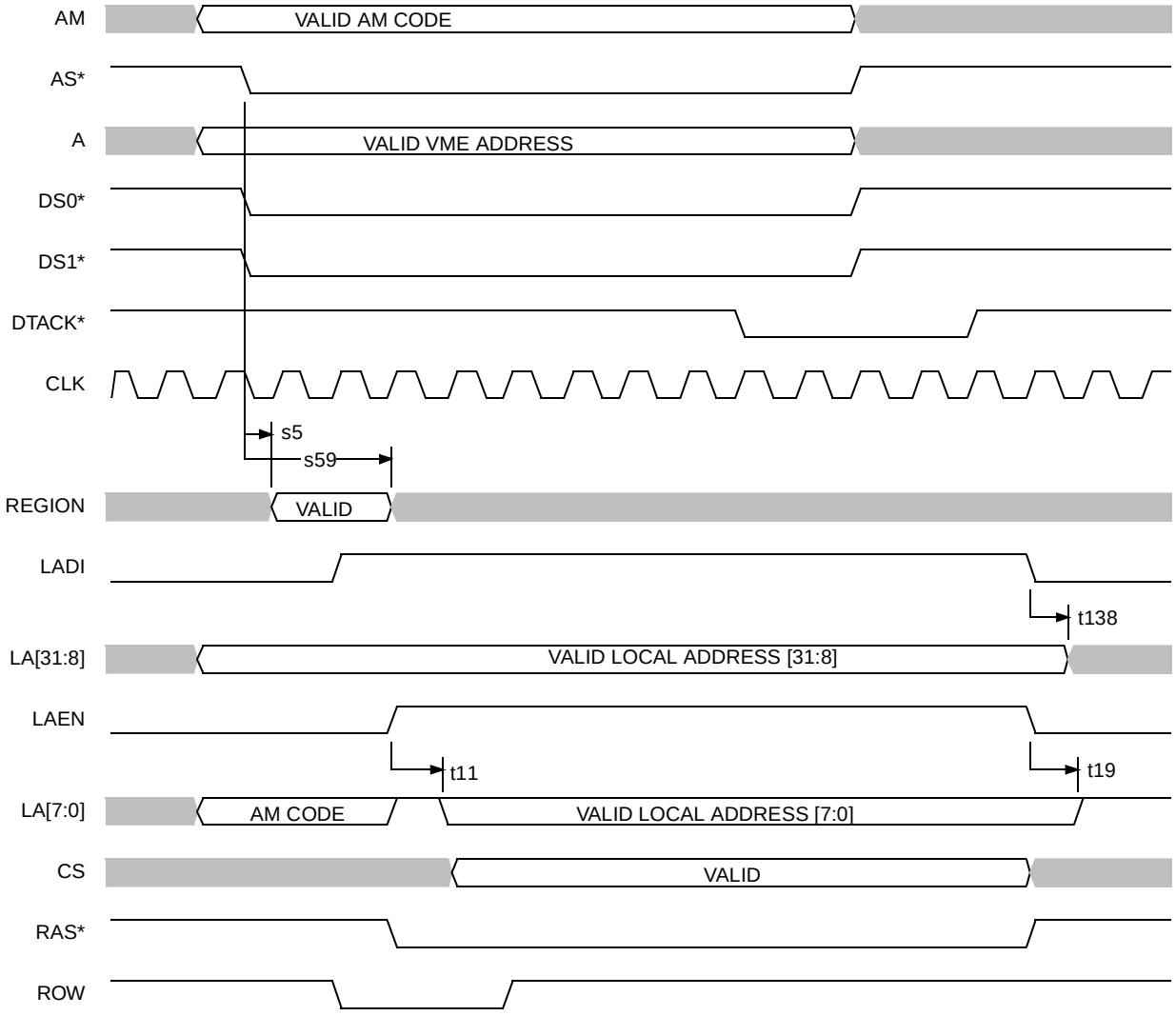
Waveform 15. Block Transfer Read (Slow Local)



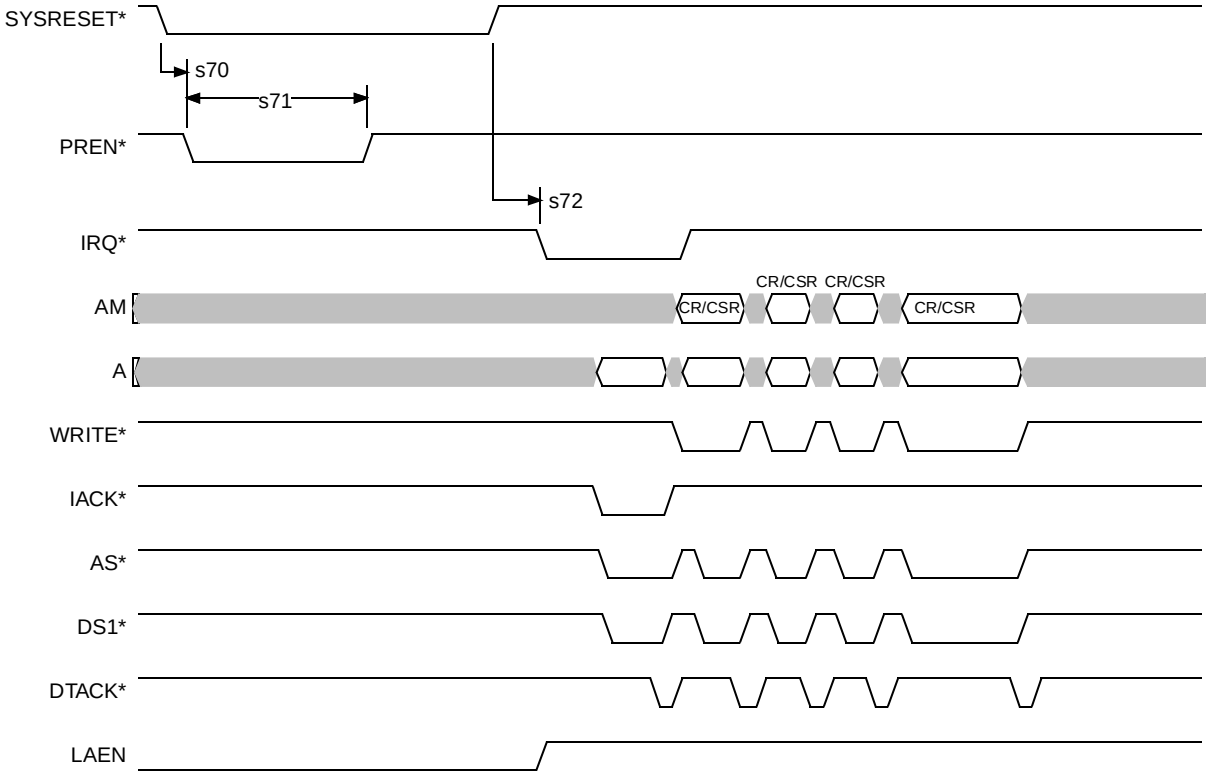
Waveform 16. Block Transfer Write (Slow VMEbus)



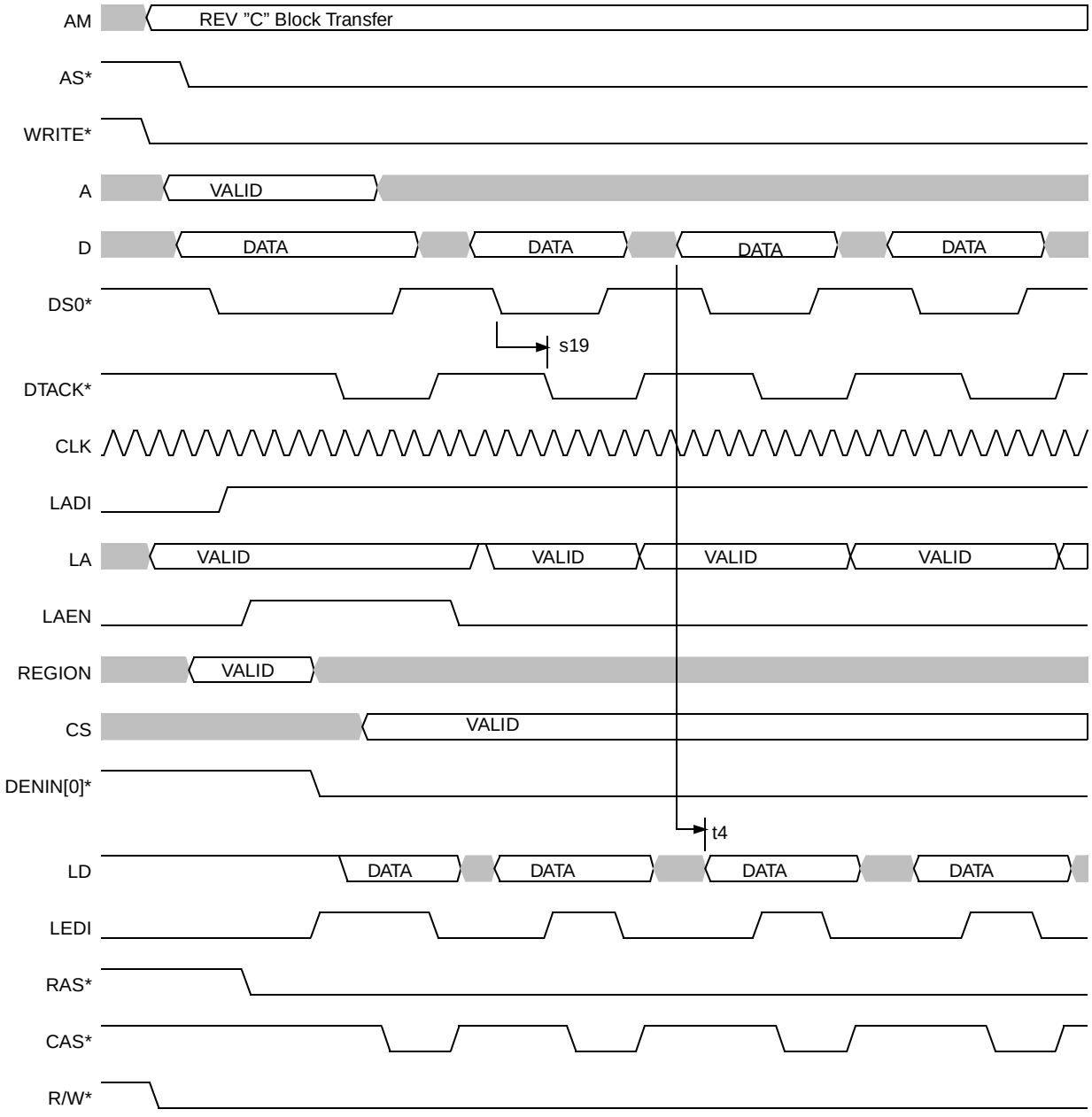
Waveform 17. Block Transfer Write (Slow Local)



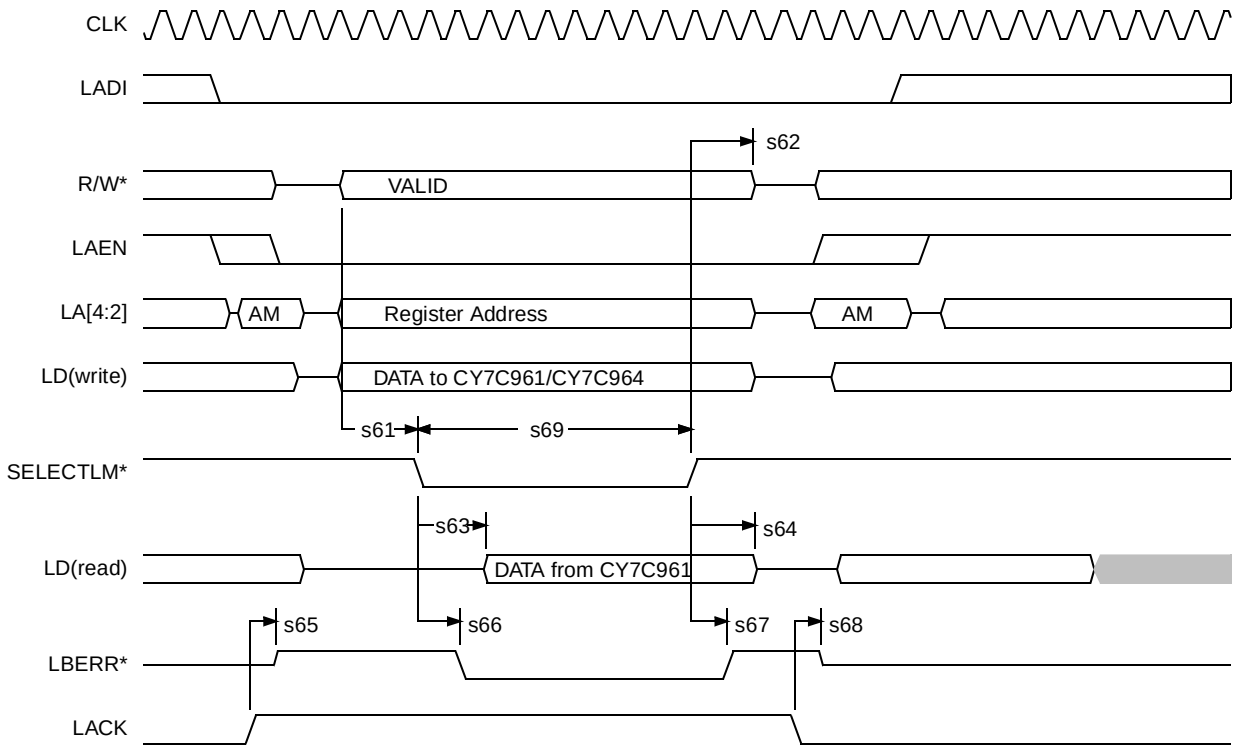
Waveform 18. AMCODE or LA and Decode Timing



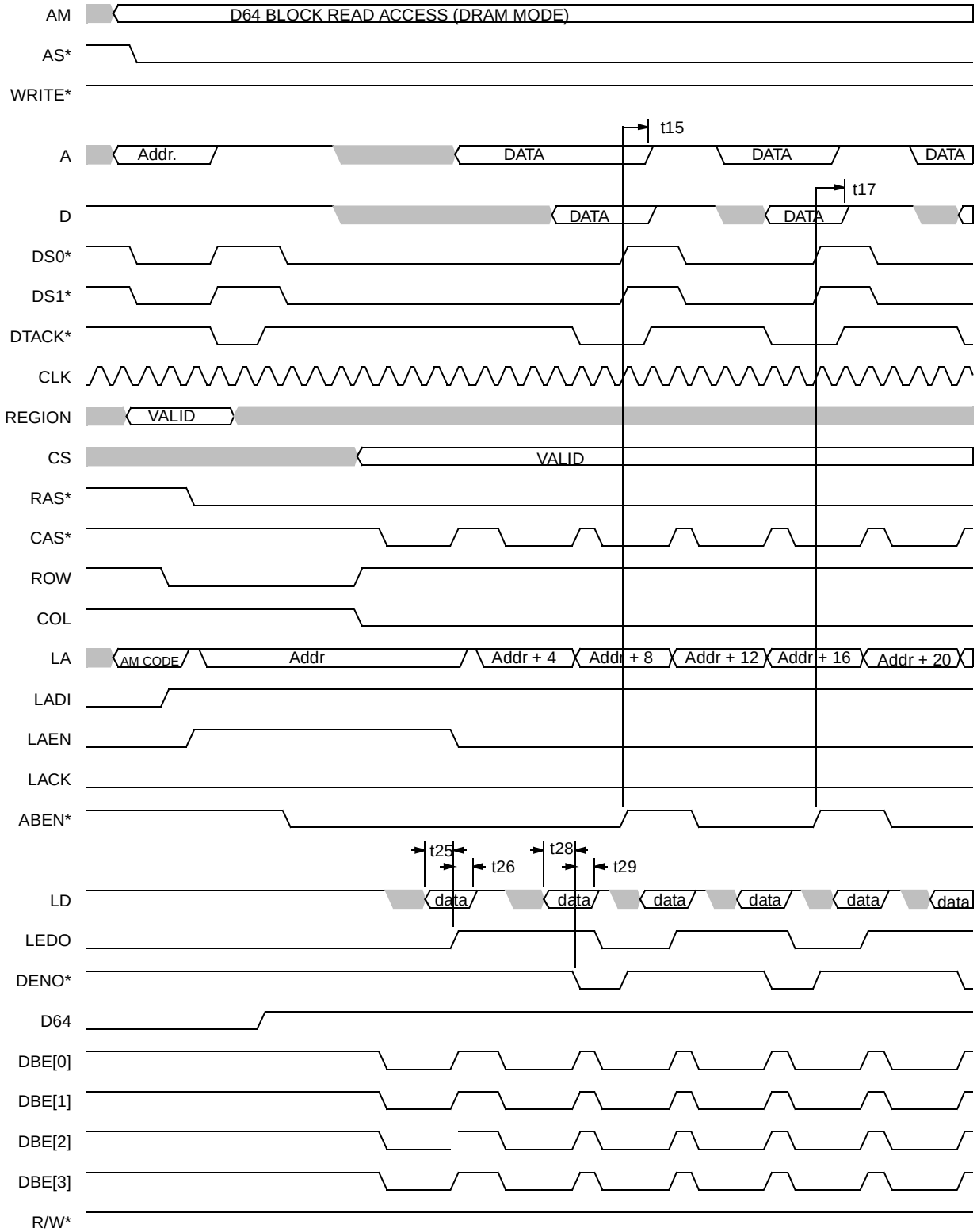
Waveform 19. VMEbus Initialization Method



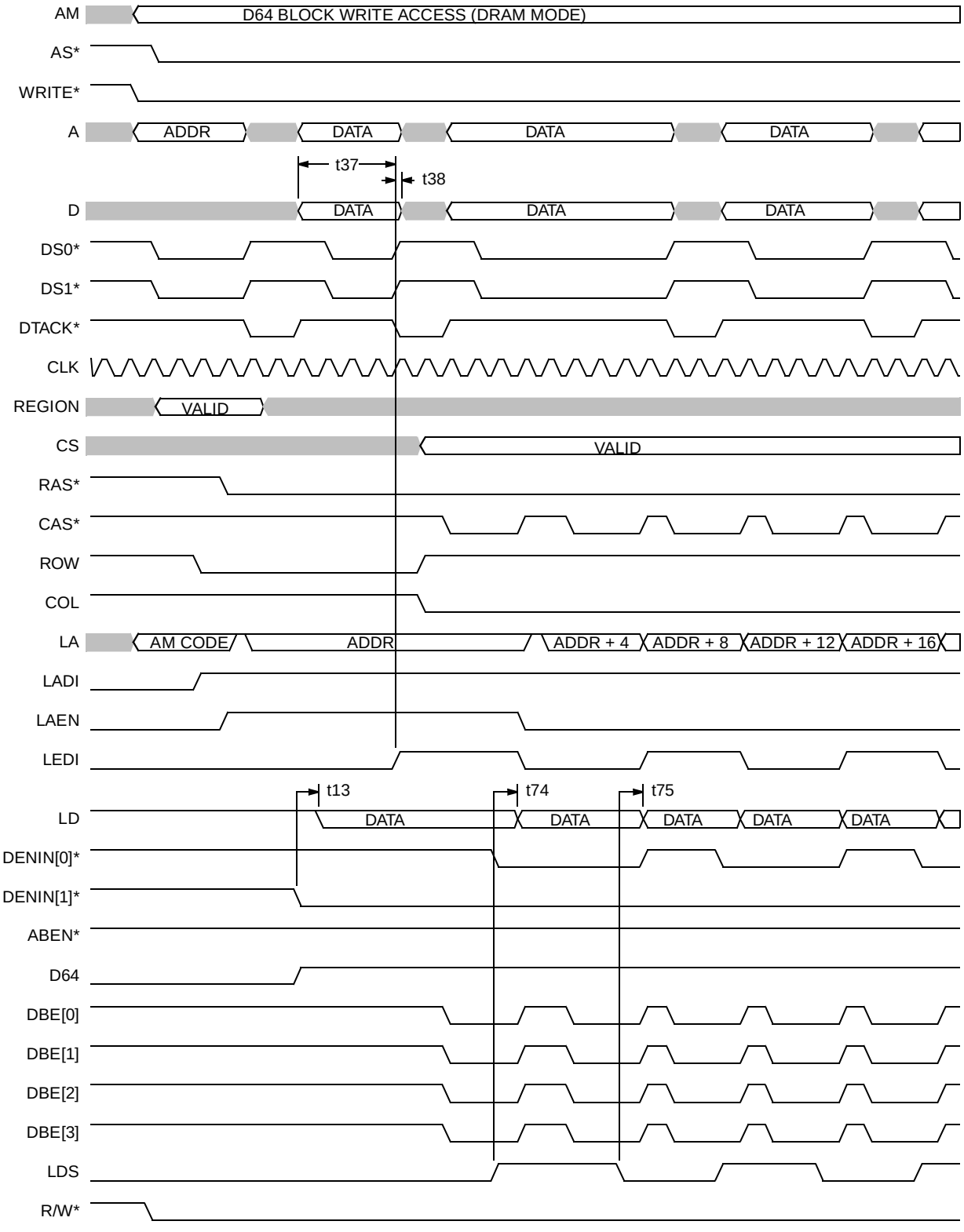
Waveform 20. Block Transfer Write (DRAM Mode)



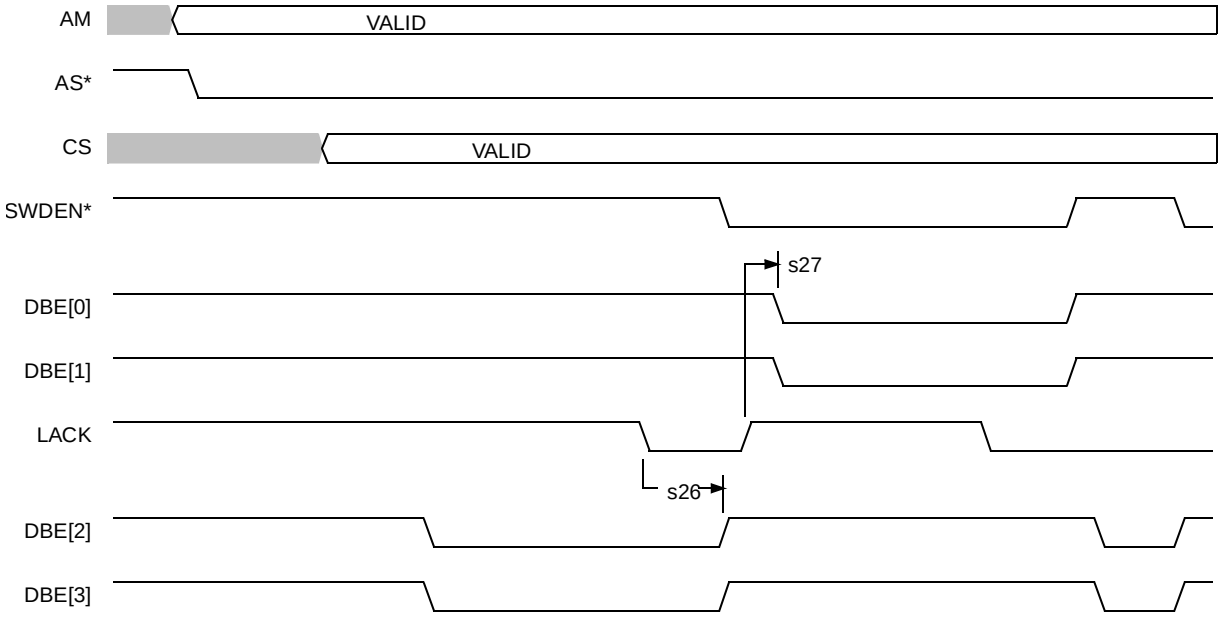
Waveform 21. Local Bus Holdoff (and CY7C961 Register Access)



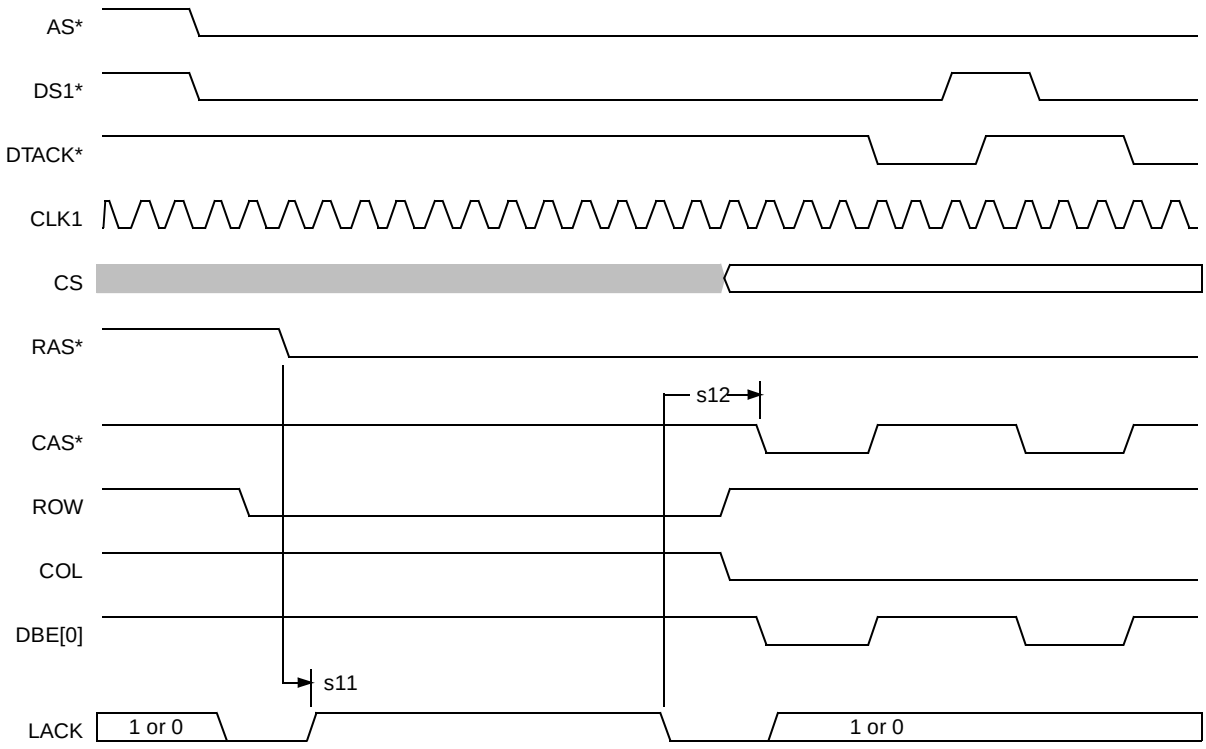
Waveform 22. D64 Block Read Access (DRAM Mode)



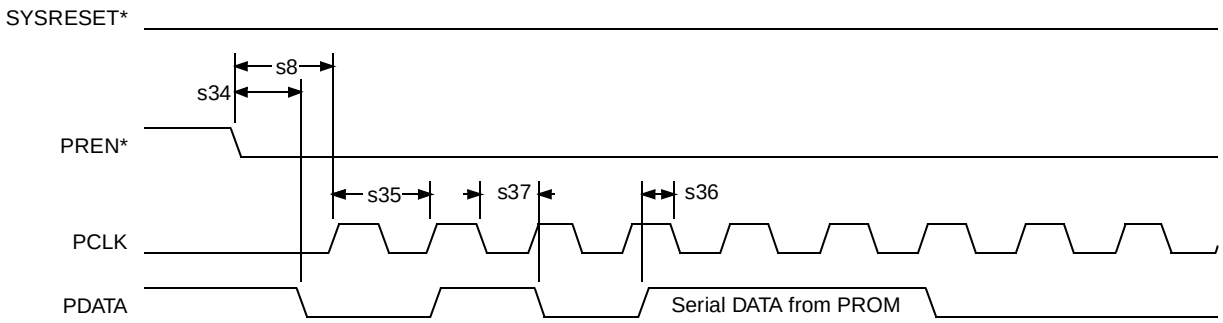
Waveform 23. D64 Block Write Access (DRAM Mode)



Waveform 24. LACK Handshake (I/O Mode)



Waveform 25. LACK Handshake (DRAM Mode)



Waveform 26. Local Initialization Method