

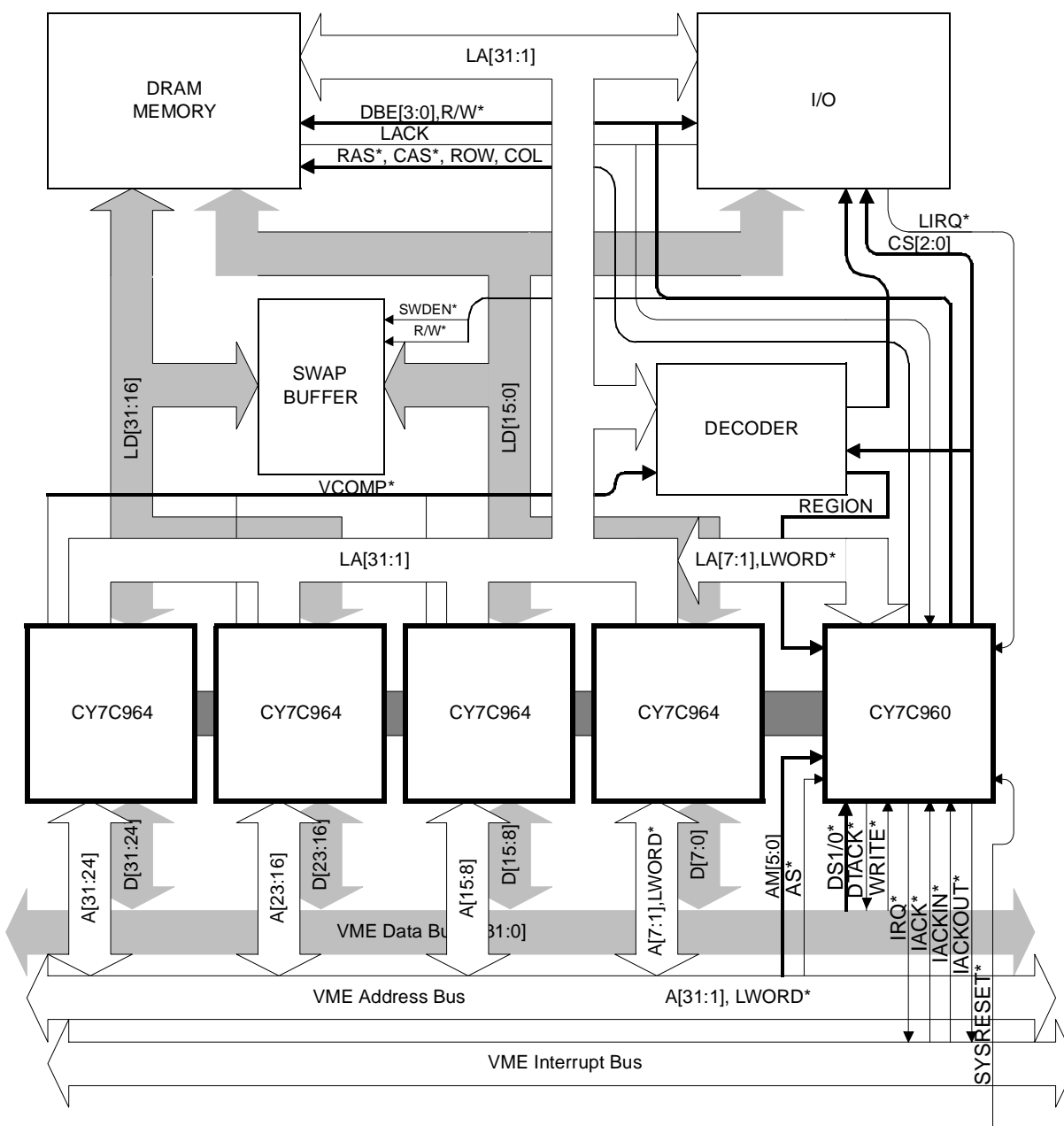


## 3.2 System Block Diagrams

Four examples of system diagrams are shown: a 6U example, a 3U example, a low cost 6U implementation, and a CY7C961 3U example.

*Figure 3-4* shows an example of a 6U form factor board design. The details of the local circuitry are at the option of the board designer: this diagram illustrates the simplicity of the CY7C960 VMEbus interface. Note that in this example, DRAM/IO mode is selected so there are three region inputs; the VMEbus is used for configuration as no serial PROM is shown; if AM Code multiplexing is used, the LA[7:2] pins should be connected to the external address decoder and LADI is used to latch the code in the decoder. As CY7C964s are used, LAEN is required to be active High, and hence the internal pull-down resistor is sufficient to define this signal at power-on. No resistors are shown for clarity: see the Pin Description section (Chapter 3.3) for details of which signals are required to be pulled up or down.

The four CY7C964s are controlled by the CY7C960. For more details concerning the connection of the CY7C964 to the CY7C960, see the section on CY7C964 Interface (Chapter 3.6). The CY7C960 connects directly to the control signals of the VMEbus as shown. The CY7C964s connect directly to the VMEbus Data and Address bus. If it is desired to support 8- and 16-bit VMEbus data transfers to 32-bit memory or peripherals, then the Swap Buffer provides the data path switching needed to transfer the bytes on the appropriate byte lanes. All timing and control for this comes from the CY7C960. If only 32- and 64-bit transfers are required, the swap circuitry is not needed. The decoder block provides the function of Slave Address Map decoding, and is user-defined. The CY7C960 ensures that the VMEbus Address is available on the local address pins at the appropriate times, and the decoder compares the value with user-defined inputs. It is the responsibility of the decoder block to provide the REGION[2:0] inputs to the CY7C960. In very simple systems the address comparators within the CY7C964s could be used in place of the external decoder block. In *Figure 3-4* the CY7C964s are shown providing part of the decoder function (VCOMP\* connections).



**Figure 3-4. CY7C960 6U Block Diagram**

The DRAM is controlled by the CY7C960, including refresh, and hence the standard connections, RAS\*, CAS\*, and R/W\* are shown. The signals ROW, COL, and DBE, are additional signals provided by the CY7C960 to facilitate control of the array. The local handshake, LACK, is shown connected to the DRAM array. In some cases it may be desirable to delay the progress of a DRAM access—LACK can accomplish this. LACK is also used to handshake I/O cycles if desired. The DBE signals connected to the I/O block provide byte addressing for peripherals greater than 8 bits wide.

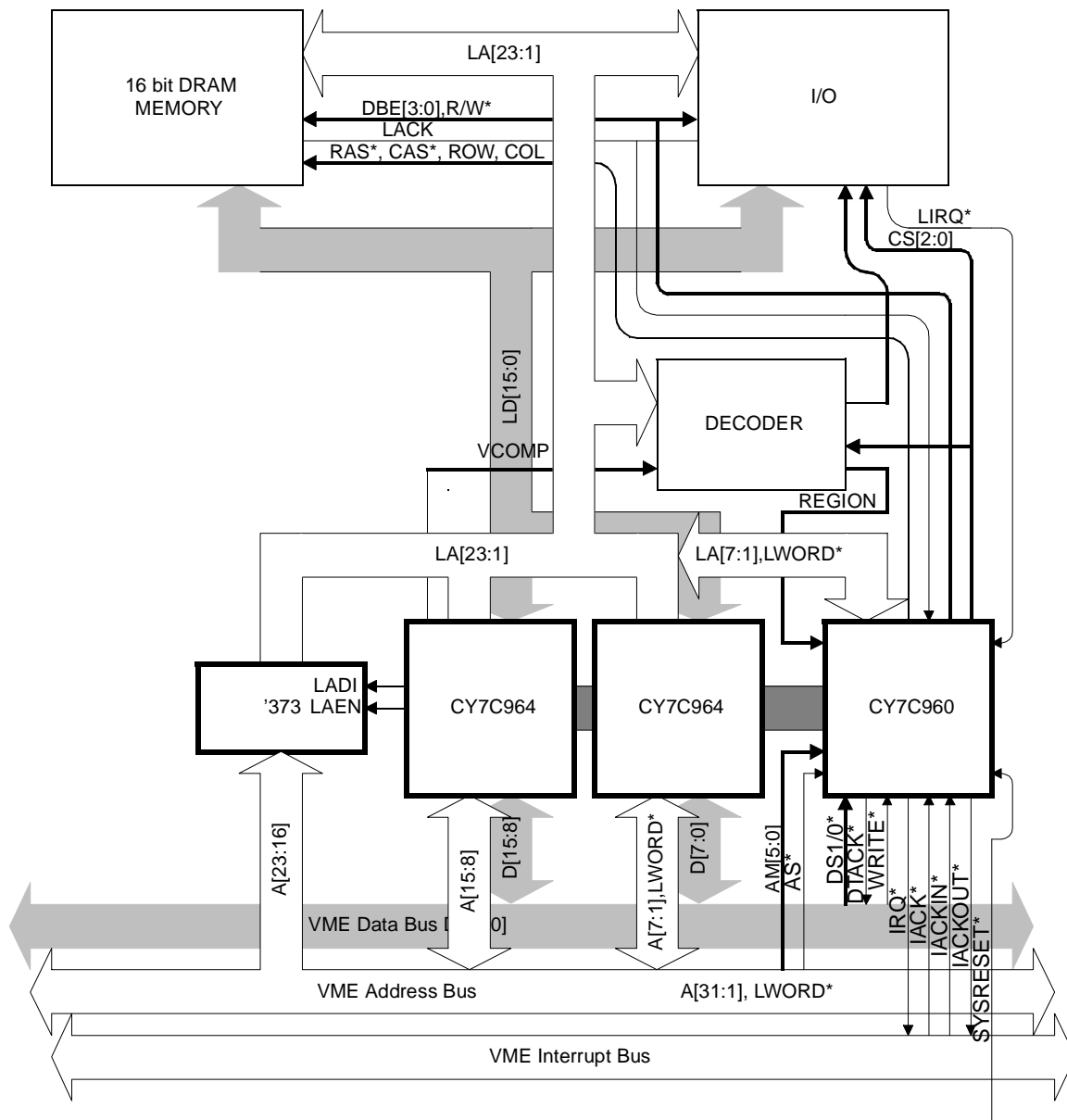
The I/O block is shown providing an interrupt, LIRQ\*. This signal causes the CY7C960 to provide a VMEbus Interrupt. It is the responsibility of the Interrupt Handler and local circuitry to remove the LIRQ\* signal at the appropriate time. The CY7C960 merely copies the value of the LIRQ\* through to its IRQ\* pin, and handles the IACK cycles appropriately.

The CY7C960 drives the Chip Select outputs in response to a VMEbus cycle. The pattern that is driven can be any binary pattern. In this example, the three available chip selects are programmed to provide a different binary pattern for each of the available eight Regions. They are connected to the decoder so as to provide a three-to-eight decoder. Thus up to eight peripherals could be selected in this manner.

*Figure 3-5* shows a 3U system diagram. In this case there are only two CY7C964s needed, along with one 8-bit address buffer. If the AM Code is connected to the external decoder on pins LA[7:2], then LADI is used to latch the AM Code value in the decoder at the appropriate time. LAEN is required to be active-High as in the 6U example.

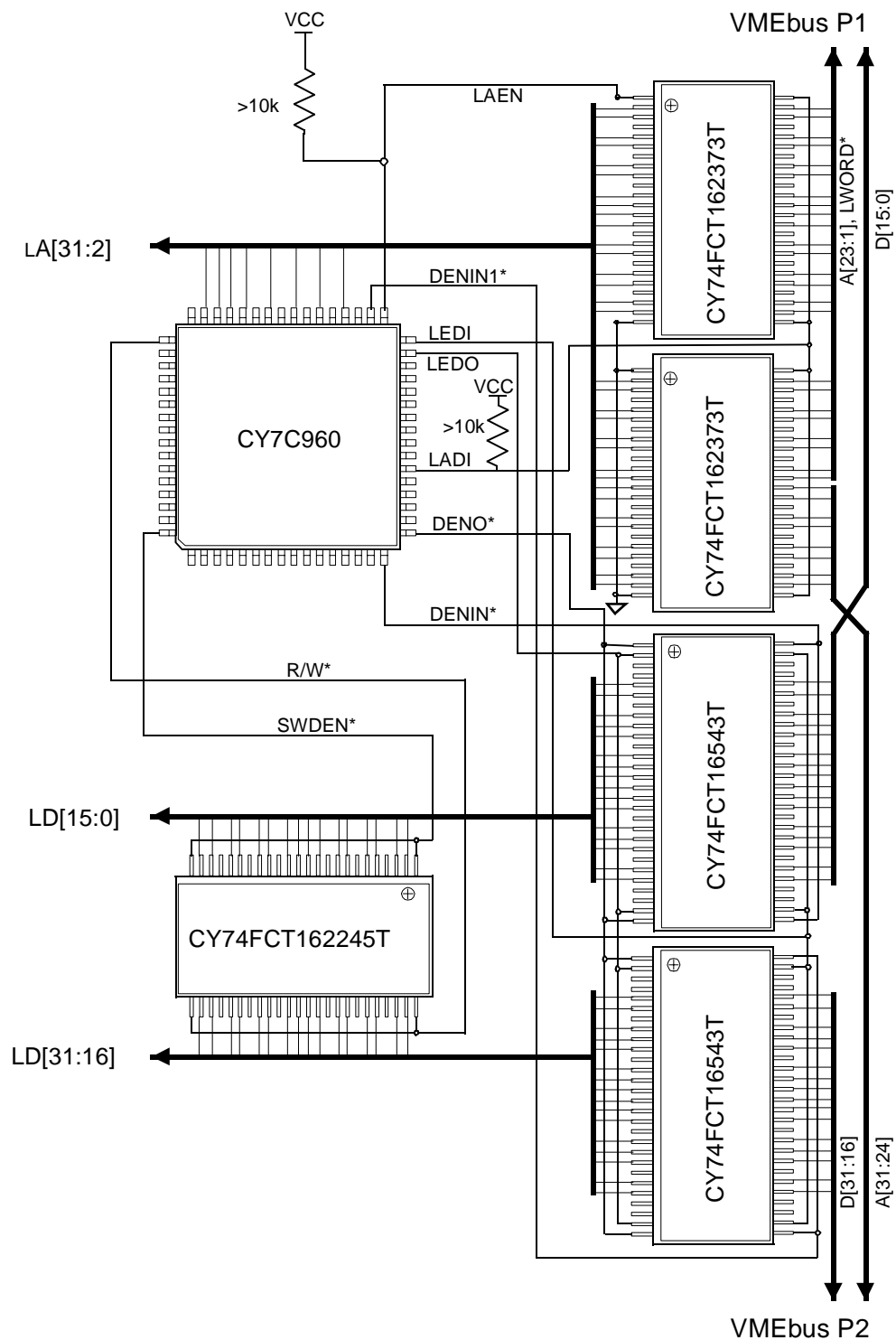
In order to add support for A40/MD32 operations the external decoder would use DENIN\* and DENIN1\* to enable the local data LD[15:0] into the decoder comparator, making up the upper 16 bits of A[39:0]. The CY7C964s provide the multiplexing for the upper 16 bits of the 32-bit data word. The controls for these transactions are provided automatically by the CY7C960. The DBE signals require combinational logic if the local memory or peripherals are 16 bits wide, as the CY7C960 is designed to control 32-bit local devices. Thus a VMEbus D16 block transfer would activate first DBE[1:0], then DBE[3:2], dependent upon the starting address. The DBEs should be logically combined to produce the desired result. Refer to section 3.6.3, Swap Buffer Control, for more information.

*Figure 3-6* shows a low-cost 6U implementation. The VMEbus address and data are buffered by Cypress FCT parts as shown, controlled by the CY7C960 without additional logic being required. In this case the LAEN is required to be active-Low, accomplished at power on using the pull-up resistor externally as shown. As CY7C964s are not used, the functions that this schematic provides are limited. For example, no multiplexed data transactions, or A64/A40 transactions are possible. The external address decoder cannot take advantage of the CY7C964's on-chip comparators in providing the slave address decode signals REGION[3:0].

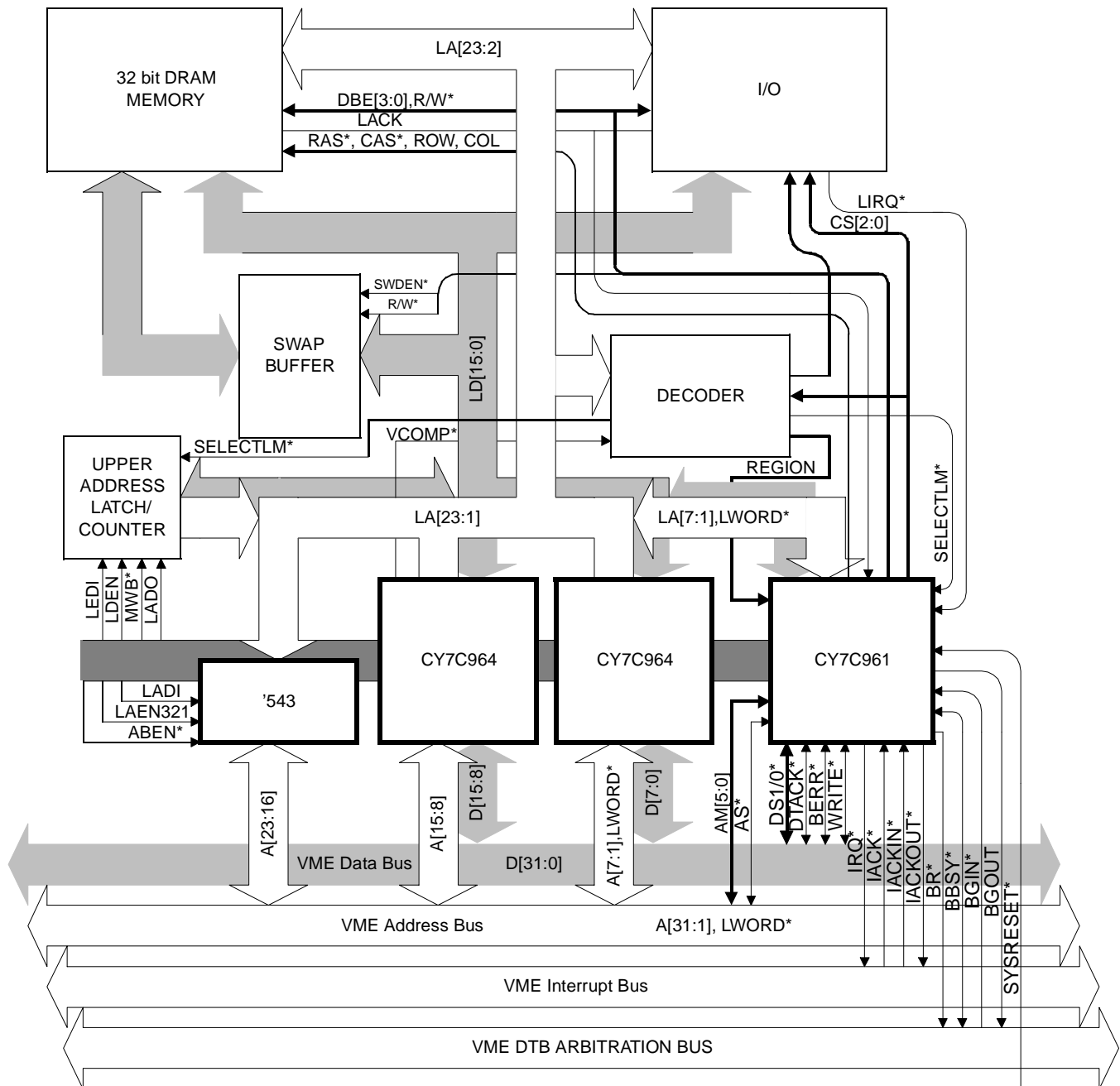


**Figure 3-5. CY7C960 3U Block Diagram**

Figure 3-7 shows the system diagram for a CY7C961 3U implementation. Note that there are additional connections to the VME arbitration bus. The block diagram shown supports A40 master operations through the use of an external upper address latch. In this implementation the local DRAM is 32 bits wide, though the VMEbus data connections are only 16 bits wide. A swap buffer comprised of bidirectional transceivers such as the CY74FCT162445 is used to drive the correct byte lanes of the DRAM, controlled by the CY7C961 automatically. Refer to section 3.6.3, Swap Buffer Control, for more information.



**Figure 3-6. CY7C960 Low-Cost Block Diagram**



**Figure 3-7. CY7C961 3U Block Diagram**

These four examples illustrate the flexibility of the CY7C960 and CY7C961 in supporting many different VMEbus and local bus configurations.