3.7 Interfacing without CY7C964

3.7.1 Reduced Cost, Fewer Features

Many board designs need only simple VMEbus slave interfaces. The CY7C960 used in combination with Cypress FCT Logic family devices meets this need perfectly. A complete interface can be built using the CY7C960 in combination with industry standard latches, transceivers, and latched transceivers.

This interface supports Rev C VMEbus: A16, A24, A32 D8, D16, D32, D32UAT, RMW, in other words, a complete interface excluding the performance and multiplexed address features of VME64.

Because the CY7C964 was designed as an integrated replacement for a pair of bidirectional transceivers controlling address and data in the VMEbus interface, the number and sense of signals controlling transceiver function have been preserved in the design of the CY7C960. This makes direct connection and control of discrete devices straightforward.

Figure 3-25 illustrates just such an implementation. One pair of CY74FCT16543T devices handles the bidirectional data path while a pair of CY74FCT162373T devices provides for latching and driving 32 bits of address from the VMEbus to the local side of the interface. A swap buffer, implemented with a CY74FCT162245T device is optional depending on the VMEbus transactions the slave interface is intended to accept.

The pull-up resistor shown is required to program the polarity of the LAEN output of the CY7C960. LAEN is three-stated at power-on or warm reset. The logic level sensed on LAEN during the first initialization cycle determines the deasserted state of LAEN during normal operation. In this case, the deasserted state is required to be High.

The FCT543 devices are rated 64 mA sink current and 32 mA source current over commercial temperature range. The FCT245 and FCT373 devices have balanced 24 mA output drive.

In *Figure 3-25* all components are drawn to relative scale assuming the CY7C960 in a 64-pin thin quad flat pack. The FCT Logic devices are depicted in thin shrunk small outline packages. The total footprint area of the interface as shown is only 1.08 sq. in. for the 6 chips. This compares to the slightly larger CY7C960/CY7C964 solution requiring 1.16 sq. in. using 5 identical packages. The CY7C961/CY7C964 chip set occupies 1.34 sq. in. All of these interface sets have thin package profiles suitable for mounting on the back side of a VMEbus board without violating mechanical clearance requirements.

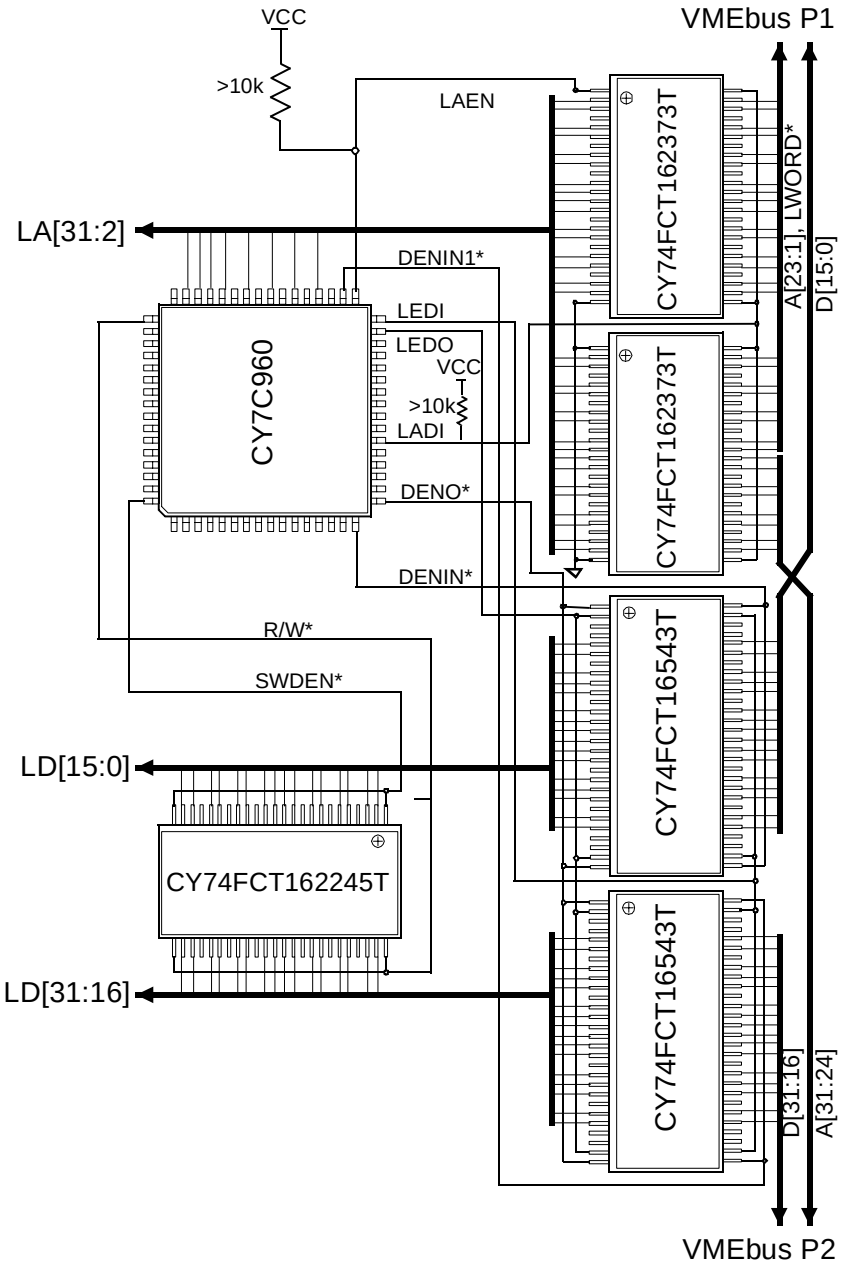

Figure 3-25. VMEbus Interface Implemented with CY7C960 and FCT Logic Family.