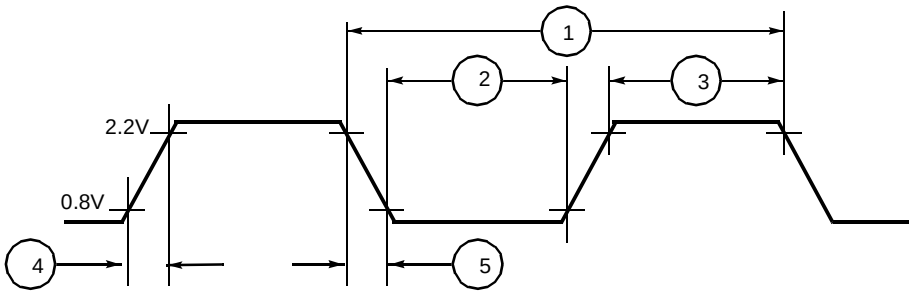
5.6

VAC068A AC Performance Specifications

Clock Input

Num.	Characteristic	Commercial		Military	
		Min.	Max.	Min.	Max.
	Frequency of Operation (MHz)	1	50	1	40
1	Cycle Time (ns)	20	1000	2.5	1000
2, 3	Clock Pulse Width (Measured from 1.5V to 1.5V)			11.25	
4, 5	Rise and Fall Time (ns)		5		5



AC Specifications

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
GLOBAL RESET								
1	RESET*[0] to WORD*[L]	1	5T		5T		5T	
2	WORD*[0] to RESET* High, WORD*[H]	1	10T		10T		10T	
REGISTER WRITE								
1	LA[31:8], FCi, R/W* Valid to PAS*[L] (Set-Up Time)	1	10		10		10	
2	LD[31:16] Valid to DSACKi*[L] (Set-Up Time)	1	5		5		5	
3	PAS*[0] to DSACKi*[L]	1	6 + 1T	35 + 2T	5 + 1T	36 + 2T	5 + 1T	40 + 2T
4	PAS*[1] to DSACKi*[H]	1	5	29	4	30	4	33
5	PAS*[1] to LA[31:8], FCi, R /W* (Hold Time)	1	5		5		5	
6	PAS*[1] to LD[31:16] Invalid		6	33	5	34	5	36
REGISTER READ								
1	LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
2	PAS*[0] to DSACKi*[L]		6	35 + 1T	5	36 + 1T	5	40 +1T
3	PAS*[0] to LD[31:16] Valid		9	51 + 1T	8	53 + 1T	7	58 +1T
4	PAS*[1] to DSACKi*[H]		5	17	4	17	5	18
5	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
6	PAS*[0] to LD[31:16] Invalid	2	6 + 3T	44 + 35T	5 + 3T	44 + 3.5T	5 + 3T	45 + 3.5T
LOCAL ACCESS VIA LOCAL BUS								
1	LA[31:8], FCi, R/W* to PAS*[0] (Set-Up Time)	1	10		10		10	
2	PAS*[0] to ASIZ1/0, WORD* Valid		7	33	6	34	6	37
3	PAS*[0] to Chip Select[L]	3, 4	6	33	5	34	5	38
4	PAS*[0] to DSACKi*[L]	5	PI1 + 6	PI1+24+1T	PI1 + 5	PI1+25+1T	PI1 + 5	PI1+28+1T
5	PAS*[0] to IORD*/IOWR*[L]	6	PI3 + 6	PI3+47+1T	PI3 + 6	PI3+48+1T	PI3 + 5	PI3+53+1T
6	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
7	PAS*[1] to ASIZ1/0 WORD* Invalid		7	37	7	38	6	42
8	PAS*[1] to Chip Select*[H]	3	4	34	3	35	3	39
9	PAS*[1] to DSACKi*[H]		4	16	4	17	4	18
10	PAS*[1] to IORD*[H] / IOWR*[H]	6	PI3 + 4	PI3+21+1T	PI3 + 3	PI3+22+1T	PI3 + 3	PI3+25+1T
LOCAL ACCESS VIA VMEbus								
1	PAS*[0] to ASIZ1/0, WORD* Valid		7	33	6	34	6	37
2	PAS*[0] to Chip Select[L]	7	6	33	5	34	5	38
3	PAS*[0] to DSACKi*[L]	8	PI2 + 6	PI2+29+1T	PI2 + 5	PI2+30+1T	PI2 + 5	PI2+33+1T
4	PAS*[0] to IORD*[L], IOWR*[L]	6	PI3 + 6	PI3 + 47+1T	PI3 + 6	PI3+48+1T	PI3 + 5	PI3+53+1T
5	PAS*[1] to ASIZ1/0, WORD* Invalid		7	37	7	38	6	42
6	PAS*[1] to Chip Select[H]	6	4	34	3	35	3	39
7	PAS*[1] to DSACKi*[H]	9	5	17	4	17	4	18
8	PAS*[1] to IORD*[H], IOWR*[H]	6	PI3 + 4	PI3+21+1T	PI3 + 3	PI3+22+1T	PI3 + 3	PI3+25+1T
VMEbus SLAVE/SLAVE BLOCK ACCESS								
1	AS*[0] to SLSELi*[L] or ICFSEL*[L]		3	24	3	25	2	27
2	LAEN[1] to LA[31:8] Valid		4	24	3	25	3	27
3	AS*[1] to SLSELi*[H] or ICFSEL*[L]		6	20	5	21	5	23
4	LAEN[0] to LA[31:0] Invalid		12	30	10	31	10	33
VMEbus MASTER ACCESS								
1	LA[31:8], FCi, R/W* to PAS*[0] (Set-Up Time)	1	10		10		10	

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
2	PAS*[0] to ASIZ1/0, WORD* Valid		7	33	6	34	6	37
3	PAS*[0] to MWB*[L]		11	30	10	32	10	35
4	ABEN*[0] to A[31:8] Valid		3	17	2	18	2	20
5	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
6	PAS*[1] to ASIZ1/0, WORD* Invalid		7	37	7	38	6	42
7	PAS*[1] to MWB*[L]		3	31	2	32	2	36
8	ABEN*[1] to A[31:8] Invalid		2	10	1	10	1	11
MASTER BLOCK TRANSFER INITIATION CYCLE								
1	LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	
2	PAS*[0] to ASIZ1/0, WORD* Valid		7	33	6	34	6	37
3	PAS*[0] to DSACKi*[L]		6 + 1T	35 + 2T	5 + 1T	36 + 2T	5 + 1T	40 + 2T
4	PAS*[0] to MWB*[L]		11	30	10	32	10	35
5	PAS*[1] to ASIZ1/0, WORD* (Hold Time)		7	37	7	38	6	42
6	PAS*[1] to DSACKi*[H]		5	17	4	17	4	18
7	PAS*[1] to MWB*[H]		3	31	2	32	2	36
8	ABEN*[0] to A[31:8] Valid		3	17	2	18	2	20
9	LAEN[1], FCi Valid to LA[31:8] Valid		4	24	3	25	3	27
10	LAEN[1], FCi Valid to LDMACK*[1]		1	27	1	28	1	31
BOUNDARY CROSSING								
1	BLT*[1] to LA[31:8] Incremented		1	27	1	28	1	33
2	LADO[0] to A[31:8] Incremented		7	28	5	29	4	33
PIO OUTPUT								
1	LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	
2	LD[31:16] to PAS*[0] (Set-Up Time)	1	5		5		5	
3	PAS*[0] to PIO[13:0] Valid		4 + 1T	54 + 2T	3 + 1T	56 + 2T	3 + 1T	63 + 2T
4	PAS*[0] to DSACKi*[L]		6 + 1T	35 + 2T	5 + 1T	36 + 2T	5 + 1T	40 + 2T
5	PAS*[1] to DSACKi*[H]		4	16	4	17	4	18
6	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
7	PAS*[1] to LD[31:16] Invalid		6	44	5	44	5	45
PIO INPUT								
1	LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
2	PIO[13:0] to PAS*[0] (Set-Up Time)	1	5		5		5	
3	PAS*[0] to DSACKi*[L]		6	35 + 1T	5	36 + 1T	5	40 + 1T
4	PAS*[0] to LD[31:16] Valid		9	51 +1T	8	53 + 1T	7	58 + 1T
5	PAS*[1] to DSACKi*[H]		4	16	4	17	4	18
6	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
7	PAS*[1] to LD[31:16] Invalid		6	44	5	44	5	45

Notes:

1. Guaranteed, but not tested.
2. Maximum time to LD[31:16] invalid is PAS*[0] + 3.5T or PAS*[1], whichever occurs first.
3. Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, VSBSEL*, FPUCS*, CS*, or IOSELi*.
4. The Decode Control register provides facilities to condition DRAMCS* or boundary decodes with the assertion of PAS*.
5. PI1 is the programmable interval for EPROMCS*, SHRCS*, and IOSELi* in the DSACKi* Control register.
6. PI3 is the programmable interval for IORD* and IOWR* in the Decode Control register.
7. Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, or VSBSEL*.
8. PI2 is the programmable interval for EPROMCS*, SHRCS*, DRAMCS*, or VSBSEL* in the Decode Control register.
9. SLSELi* redirection is enabled in the Decode Control register.

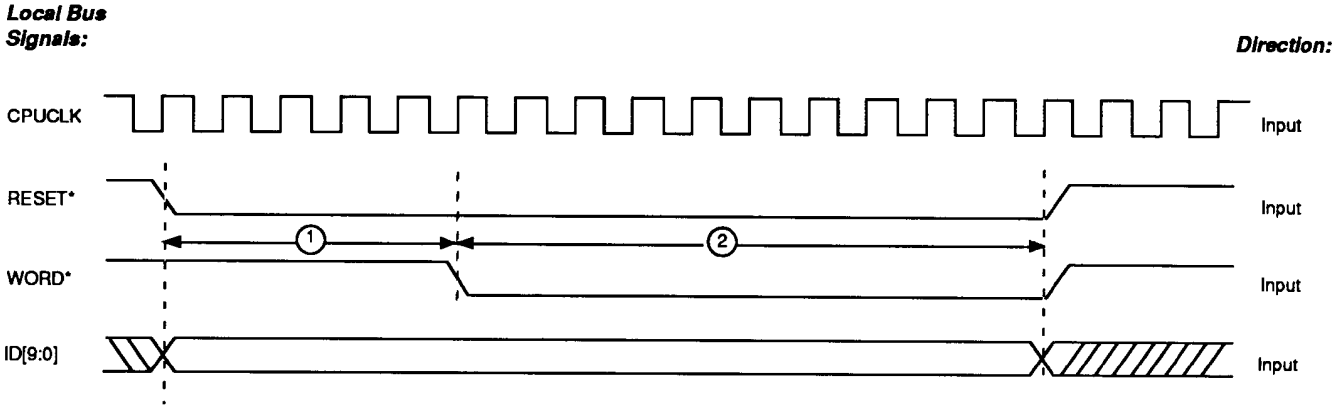


Figure 5-4. VAC068A Global Reset

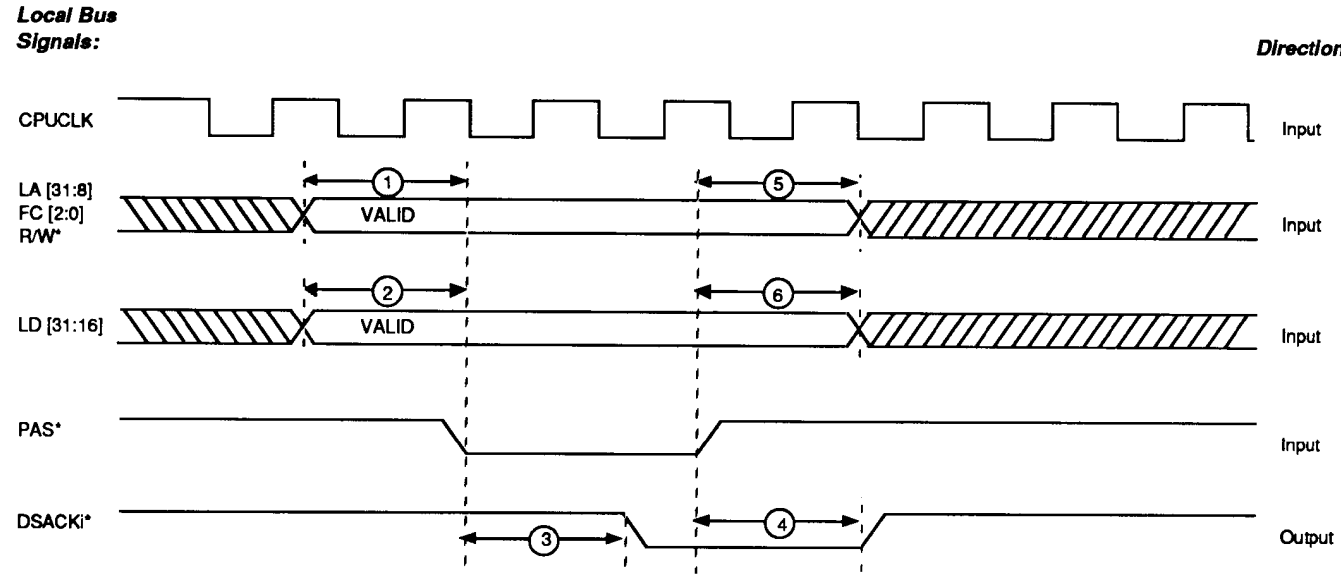


Figure 5-5. VAC068A Register Write

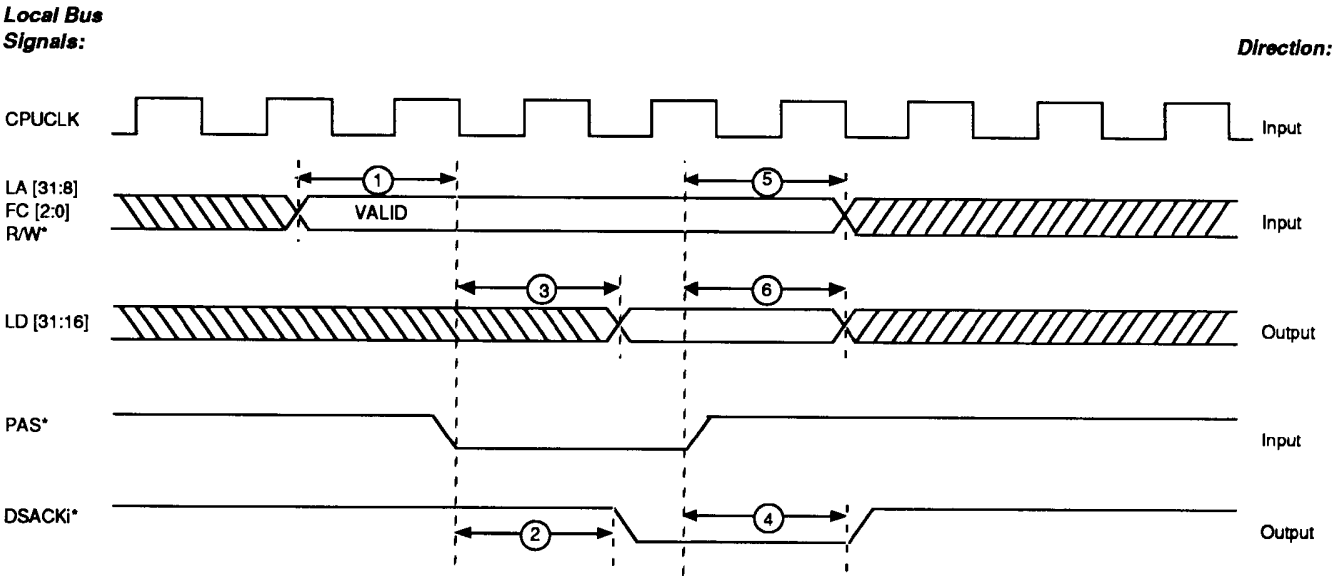


Figure 5-6. VAC068A Register Read

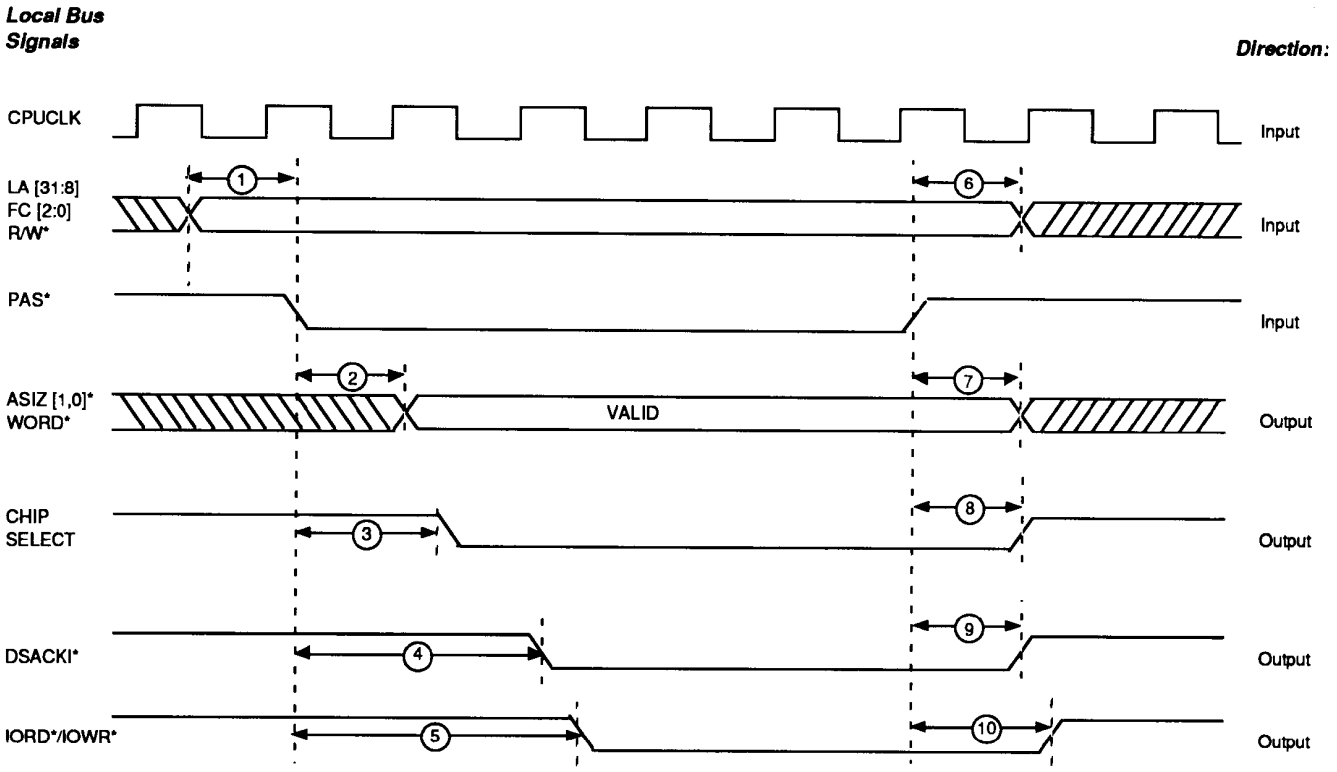


Figure 5-7. Local Resource Access via Local Bus

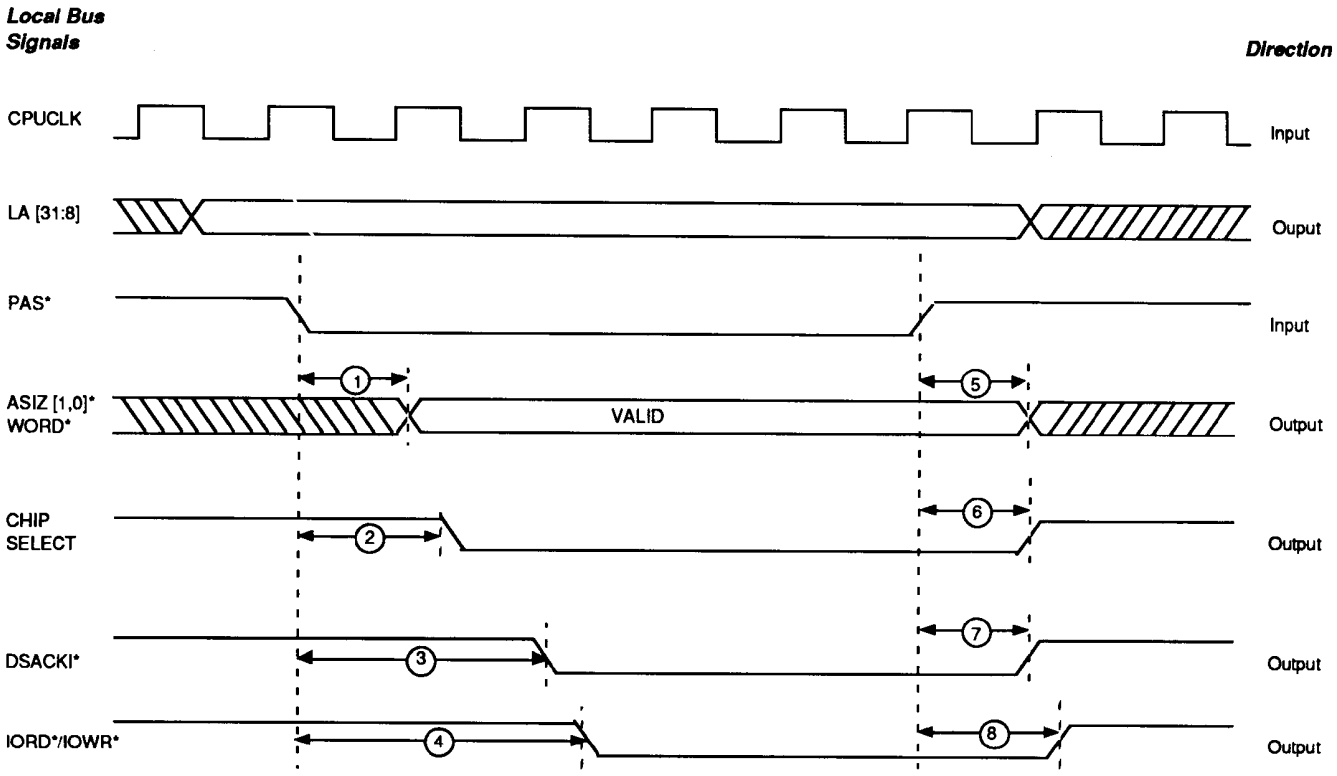


Figure 5-8. Local Resource Accesses via VMEbus

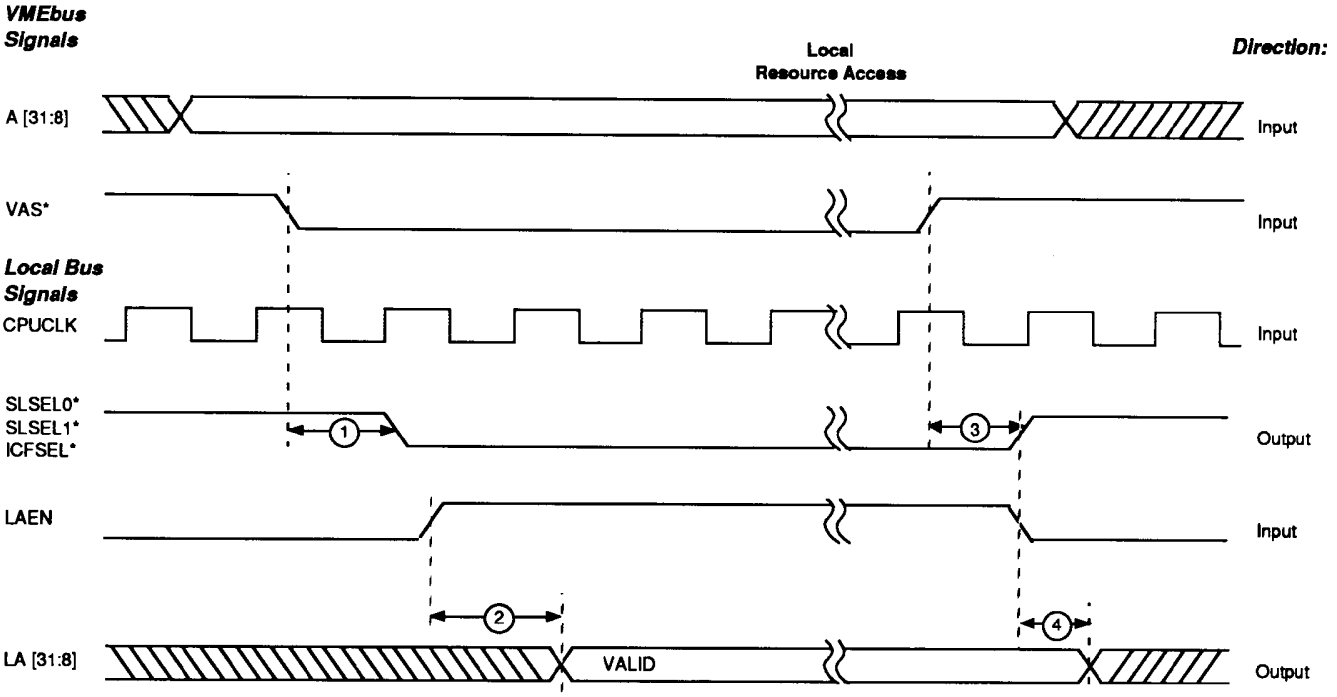


Figure 5-9. VMEbus Accesses – Slave

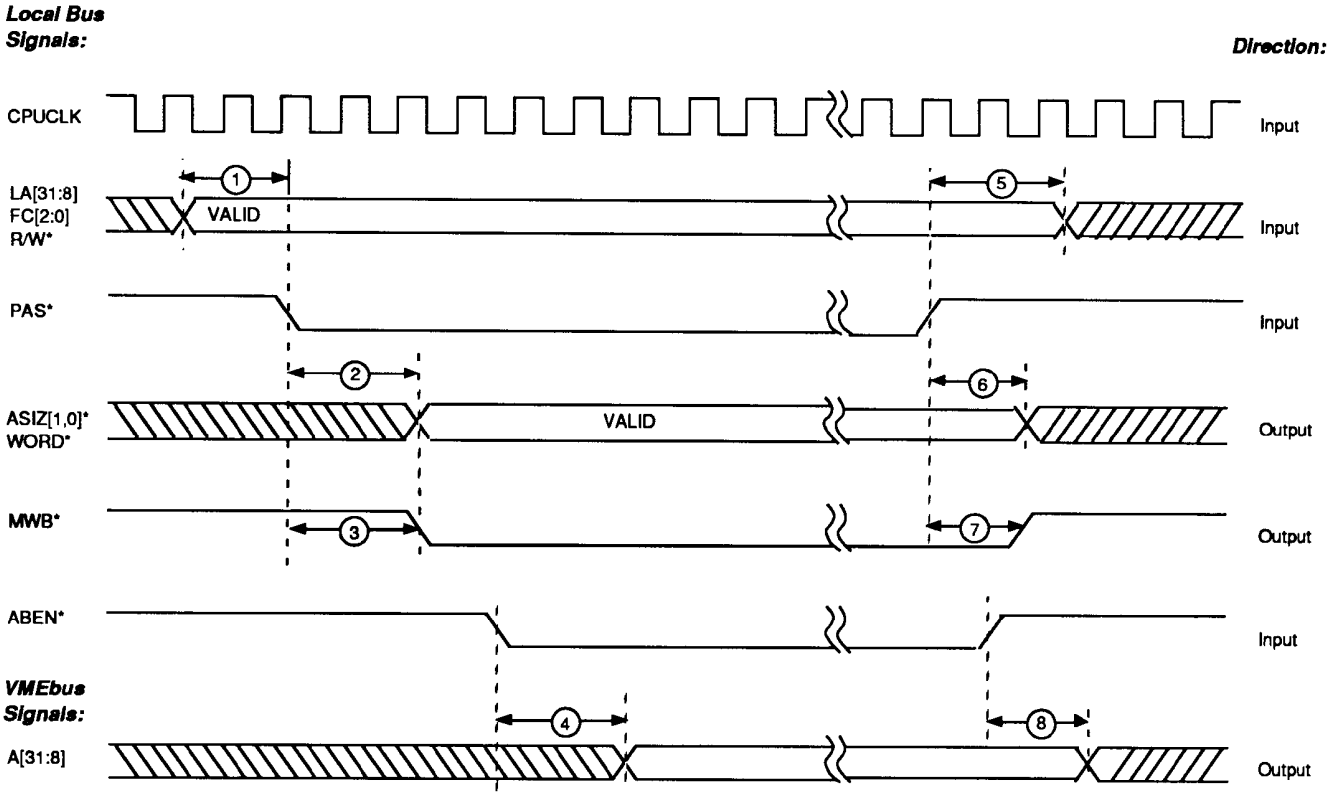


Figure 5-10. VMEbus Accesses – Master

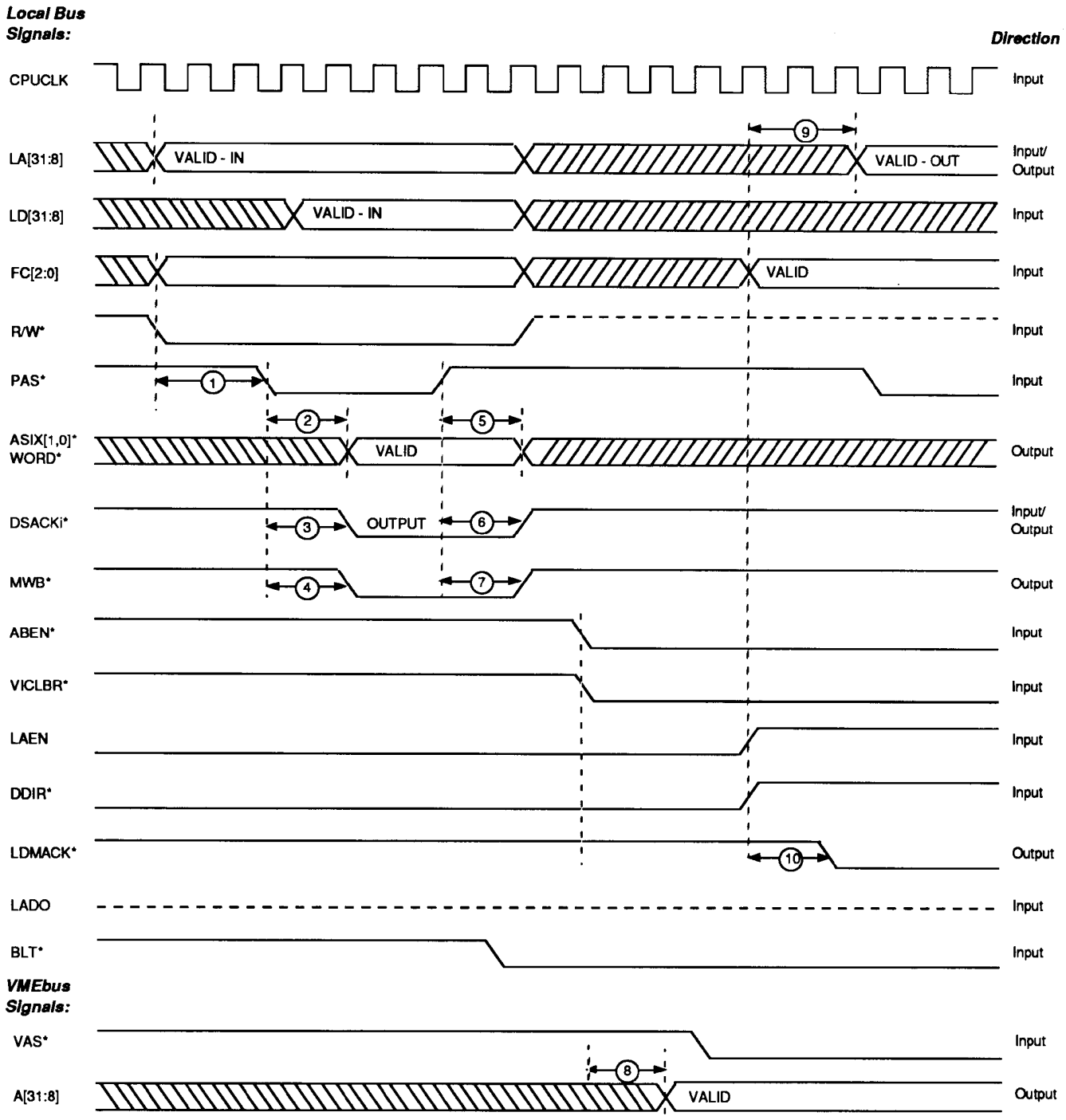


Figure 5-11. Master Block Transfer – Initialization Cycle

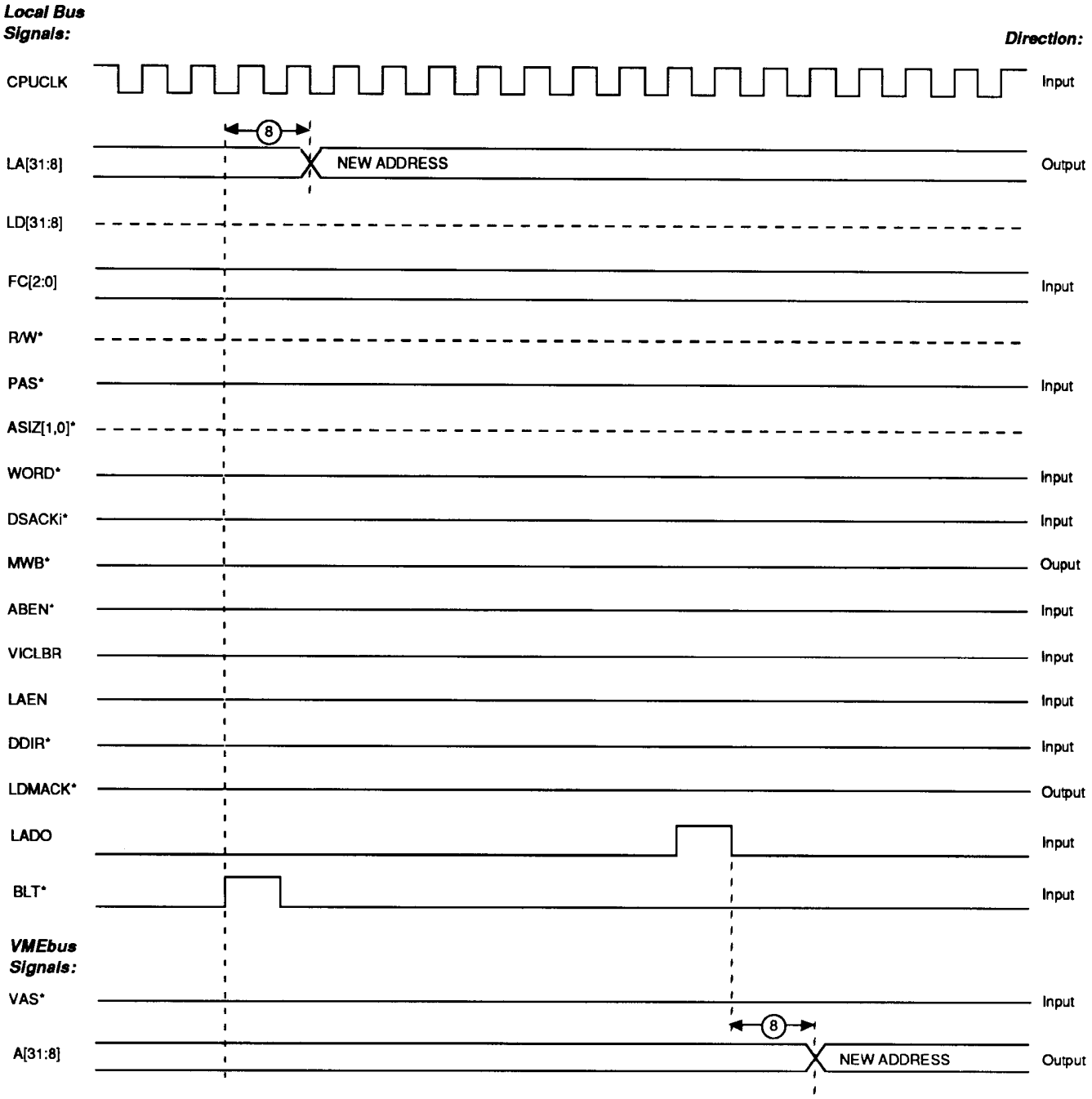


Figure 5-12. Master Block Transfer – Local and VME Boundary Crossing

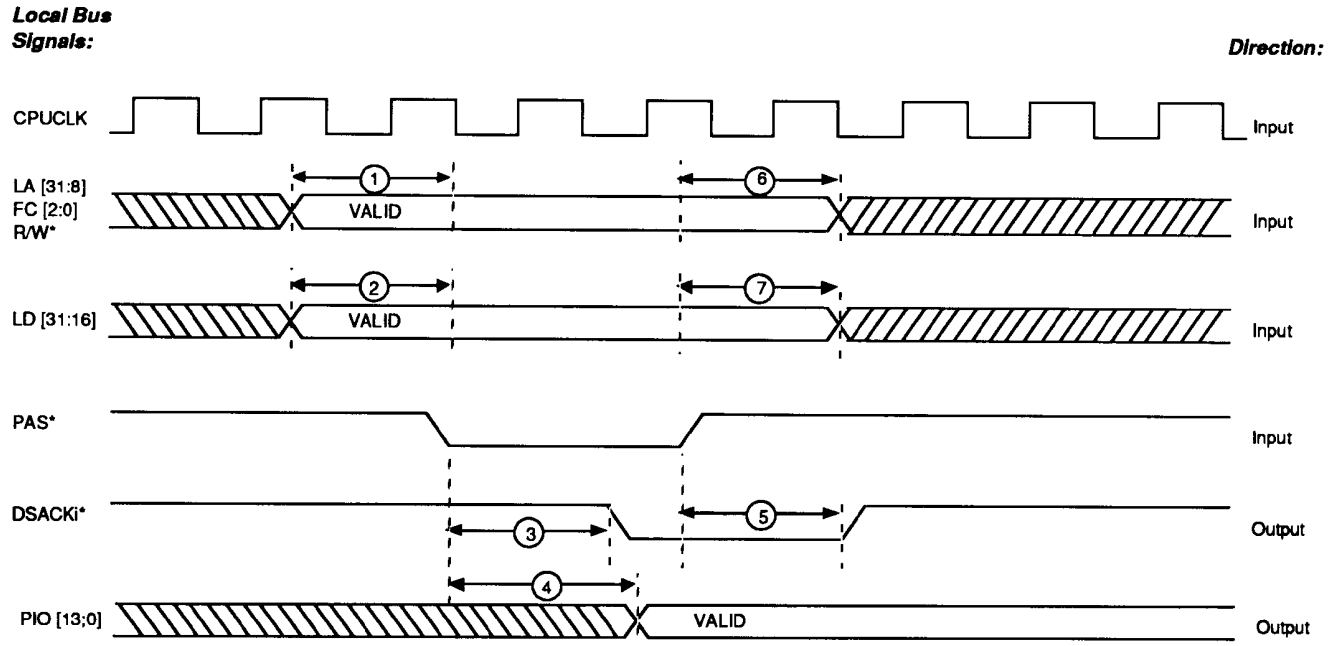


Figure 5-13. PIO Operation – Output

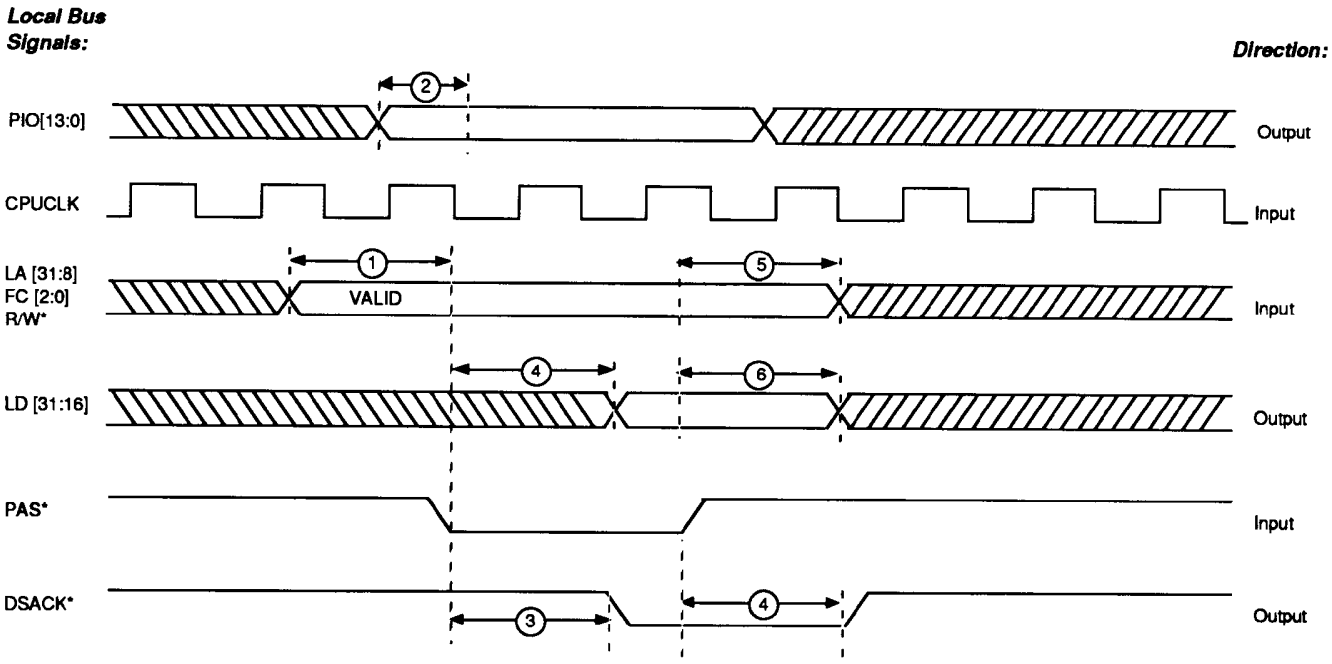


Figure 5-14. PIO Operation – Input

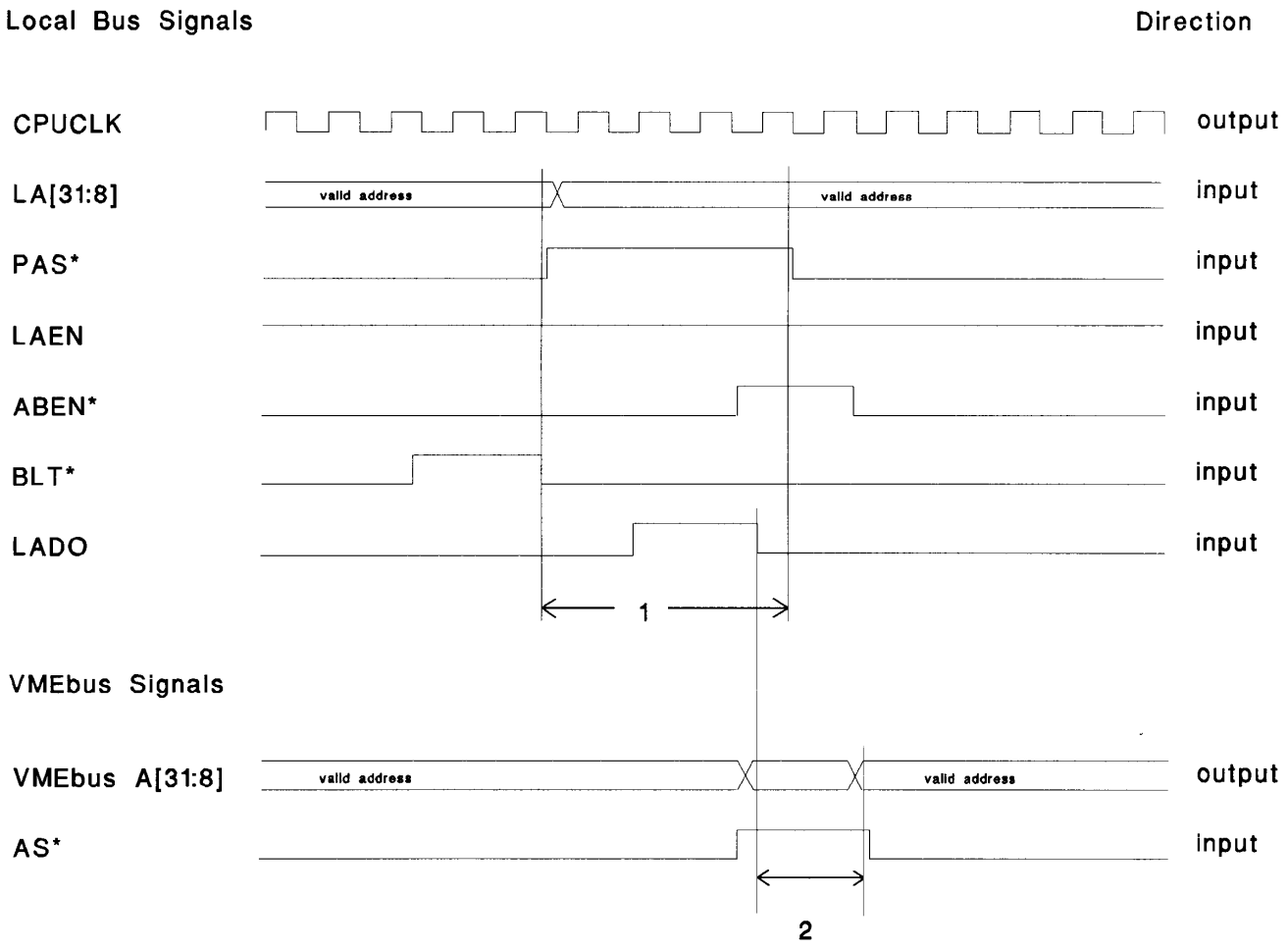


Figure 5-15. Master Block Transfer – Local and VMEbus Boundary Crossing (DMA Write Cycle)