5.7
VAC068A Signal List and Pinout

Table 5-2. VMEbus Signals

Name	PGA Pin	QFP Pin	Type	Description
A08	A8	139	Three-State I/O	VMEbus Address Signals
A09	B8	138	Three-State I/O	VMEbus Address Signals
A10	A7	142	Three-State I/O	VMEbus Address Signals
A11	B7	144	Three-State I/O	VMEbus Address Signals
A12	A6	143	Three-State I/O	VMEbus Address Signals
A13	B6	145	Three-State I/O	VMEbus Address Signals
A14	A5	147	Three-State I/O	VMEbus Address Signals
A15	B5	148	Three-State I/O	VMEbus Address Signals
A16	A4	149	Three-State I/O	VMEbus Address Signals
A17	A3	150	Three-State I/O	VMEbus Address Signals
A18	B4	151	Three-State I/O	VMEbus Address Signals
A19	B3	153	Three-State I/O	VMEbus Address Signals
A20	A2	154	Three-State I/O	VMEbus Address Signals
A21	C3	156	Three-State I/O	VMEbus Address Signals
A22	B2	157	Three-State I/O	VMEbus Address Signals
A23	A1	158	Three-State I/O	VMEbus Address Signals
A24	B9	134	Three-State I/O	VMEbus Address Signals
A25	A9	137	Three-State I/O	VMEbus Address Signals
A26	B10	132	Three-State I/O	VMEbus Address Signals
A27	A10	136	Three-State I/O	VMEbus Address Signals
A28	B11	129	Three-State I/O	VMEbus Address Signals
A29	A11	133	Three-State I/O	VMEbus Address Signals
A30	A13	128	Three-State I/O	VMEbus Address Signals
A31	A12	130	Three-State I/O	VMEbus Address Signals
AS*	D2	6	Input	VMEbus Address Strobe Signal
ABEN*	E2	9	Input	VMEbus Address Bus Enable Signal

Table 5-3. Local Signals

Name	PGA Pin	QFP Pin	Type	Description
ASIZ0	P1	34	Three-State I/O	Identifies VMEbus Address Size
ASIZ1	M3	35	Three-State I/O	Identifies VMEbus Address Size
BLT*	F1	16	Input	DMA Control Signal
CACHINH*	P13	73	Open Collector Input	Data Cache Inhibit to Processor
CPUCLK	N3	36	Input	CPU Clock Input
CS*	D14	111	Output	Chip Select to VIC068A Signal
DDIR	C1	8	Input	Swap Data Direction Buffer
DRAMCS*	N11	72	Output	DRAM Chip Select
DSACK0*	P5	49	Three-State I/O	Data and Size Acknowledge
DSACK1*	R3	48	Three-State I/O	Data and Size Acknowledge
EPROMCS*	P12	71	Output	EPROM Chip Select
FC0	P2	37	Input	CPU, VIC068A Function Code Input
FC1	R1	38	Input	CPU, VIC068A Function Code Input
FC2	N4	43	Input	CPU, VIC068A Function Code Input
FCIACK*	N2	33	Output	Interrupt Acknowledge Cycle
FPUCS*	R13	70	Output	Floating-Point Coprocessor Select
ICFSEL*	H1	19	Output	Interprocessor Communications Select
ID08	K1	23	Three-State I/O	Isolated Local Data Signals
ID09	K2	25	Three-State I/O	Isolated Local Data Signals
ID10	J2	24	Three-State I/O	Isolated Local Data Signals
ID11	L1	27	Three-State I/O	Isolated Local Data Signals
ID12	L2	28	Three-State I/O	Isolated Local Data Signals
ID13	M1	29	Three-State I/O	Isolated Local Data Signals
ID14	N1	30	Three-State I/O	Isolated Local Data Signals
ID15	L3	32	Three-State I/O	Isolated Local Data Signals
IOSEL0*	R15	78	Output	Local I/O Device Chip Select
IOSEL1*	J14	94	Output	Local I/O Device Chip Select
LA08	P14	77	Three-State I/O	Local Address Signals
LA09	M13	83	Three-State I/O	Local Address Signals
LA10	P15	85	Three-State I/O	Local Address Signals
LA11	N13	76	Three-State I/O	Local Address Signals
LA12	N14	84	Three-State I/O	Local Address Signals
LA13	L13	87	Three-State I/O	Local Address Signals
LA14	M14	86	Three-State I/O	Local Address Signals
LA15	L14	89	Three-State I/O	Local Address Signals

Table 5-3. Local Signals (continued)

Name	PGA Pin	QFP Pin	Type	Description
LA16	N15	88	Three-State I/O	Local Address Signals
LA17	K14	92	Three-State I/O	Local Address Signals
LA18	M15	90	Three-State I/O	Local Address Signals
LA19	K15	96	Three-State I/O	Local Address Signals
LA20	L15	93	Three-State I/O	Local Address Signals
LA21	J15	97	Three-State I/O	Local Address Signals
LA22	H14	98	Three-State I/O	Local Address Signals
LA23	H15	99	Three-State I/O	Local Address Signals
LA24	G14	104	Three-State I/O	Local Address Signals
LA25	G15	102	Three-State I/O	Local Address Signals
LA26	F14	105	Three-State I/O	Local Address Signals
LA27	F15	103	Three-State I/O	Local Address Signals
LA28	E15	107	Three-State I/O	Local Address Signals
LA29	F13	106	Three-State I/O	Local Address Signals
LA30	C15	110	Three-State I/O	Local Address Signals
LA31	E14	108	Three-State I/O	Local Address Signals
LD16	P6	52	Three-State I/O	Local Data Signals
LD17	R6	56	Three-State I/O	Local Data Signals
LD18	P7	54	Three-State I/O	Local Data Signals
LD19	R4	50	Three-State I/O	Local Data Signals
LD20	R7	57	Three-State I/O	Local Data Signals
LD21	R5	53	Three-State I/O	Local Data Signals
LD22	P8	58	Three-State I/O	Local Data Signals
LD23	N7	55	Three-State I/O	Local Data Signals
LD24	N8	60	Three-State I/O	Local Data Signals
LD25	R8	59	Three-State I/O	Local Data Signals
LD26	R9	62	Three-State I/O	Local Data Signals
LD27	P9	64	Three-State I/O	Local Data Signals
LD28	R10	63	Three-State I/O	Local Data Signals
LD29	P10	65	Three-State I/O	Local Data Signals
LD30	R11	67	Three-State I/O	Local Data Signals
LD31	P11	68	Three-State I/O	Local Data Signals
LADO	D3	3	Input	Latch VMEbus Address Out Signal
LADI	E1	13	Input	Latch Local Address In Signal
LAEN	P3	44	Input	Local Address Bus Enable Signal

Table 5-3. Local Signals (continued)

Name	PGA Pin	QFP Pin	Type	Description
LBR*	G3	15	Input	Local Bus Request to VIC068A Signal
LDMACK*	E3	7	Output	Local DMA is in Progress
MWB*	R12	69	Output	Module Wants Local Bus Signal
PAS*	R2	45	Input	Processor Address Strobe
PIO0/TXDA	C11	127	Three-State I/O	General-Purpose I/O or UART A Transmit Signal
PIO1/RXDA	B12	126	Three-State I/O	General-Purpose I/O or UART A Receive Signal
PIO2/TXDB	A14	125	Three-State I/O	General-Purpose I/O or UART B Transmit Signal
PIO3/RXDB	B13	124	Three-State I/O	General-Purpose I/O or UART B Receive Signal
PIO4/IORD*	F2	12	Three-State I/O	General-Purpose I/O or I/O Read Signal
PIO5/IOWR*	C12	123	Three-State I/O	General-Purpose I/O or I/O Write Signal
PIO6/ IOSEL3*	B14	117	Three-State I/O	General-Purpose I/O or I/O Select 3 Signal
PIO7/ Interrupt	C13	116	Three-State I/O	General-Purpose I/O or Interrupt Request Signal
PIO8/ IOSEL4*	D13	115	Three-State I/O	General-Purpose I/O or I/O Select 4 Signal
PIO9/ IOSEL5*	B15	114	Three-State I/O	General-Purpose I/O or I/O Select 5 Signal
PIO10/ Interrupt	C14	113	Three-State I/O	General-Purpose I/O or Interrupt Request Signal
PIO11/ Interrupt	D1	10	Three-State I/O	General-Purpose I/O or Interrupt Request Signal
PIO12/ SHRCS*	D15	109	Three-State I/O	General-Purpose I/O or Shared Resources Chip Select Signal
PIO13/ IOSEL2*	B1	5	Three-State I/O	General-Purpose I/O or I/O Select 2 Signal
REFGT*	G1	17	Output	Refresh Grant Signal
RESET*	R14	74	Input	System Reset Signal
R/W*	P4	46	Input	Read/Write Signal
SLSEL0*	H2	18	Output	Slave Select 0 Signal
SLSEL1*	J1	22	Output	Slave Select 1 Signal
SWDEN*	C2	4	Input	Swap Data Enable Signal
VSBSEL*	G2	14	Output	VSB Chip Select Signal
WORD*	M2	31	Output	16-Bit Data Access Signal

Table 5-4. Power Supply Signals[1]

Name	PGA Pin	Type	Description
V_{DD}	A15	Input	Power Input
V_{DD}	C5	Input	Power Input
V_{DD}	C7	Input	Power Input
V_{DD}	C9	Input	Power Input
V_{DD}	H3	Input	Power Input
V_{DD} Core	H13	Input	Power Input
V_{DD}	J13	Input	Power Input
V_{DD}	N5	Input	Power Input
V_{DD}	N10	Input	Power Input
V_{DD}		Input	Power Input
V_{DD}		Input	Power Input
V_{DD}		Input	Power Input
V_{DD}		Input	Power Input
V_{DD}		Input	Power Input
V_{DD}		Input	Power Input
V_{SS}	C4	Input	Ground
V_{SS}	C6	Input	Ground
V_{SS}	C8	Input	Ground
V_{SS}	C10	Input	Ground
V_{SS}	E13	Input	Ground
V_{SS}	F3	Input	Ground
V_{SS}	G13	Input	Ground
V_{SS} Core	J3	Input	Ground
V_{SS}	K3	Input	Ground
V_{SS}	N6	Input	Ground
V_{SS}	N9	Input	Ground
V_{SS}	N12	Input	Ground
V_{SS}	K13	Input	Ground
V_{SS}		Input	Ground
V_{SS}		Input	Ground
V_{SS}		Input	Ground

Table 5-4. Power Supply Signals[1] (continued)

Name	PGA Pin	Type	Description
V_{SS}		Input	Ground
V_{SS}		Input	Ground
V_{SS}		Input	Ground
V_{SS}		Input	Ground
V_{SS}		Input	Ground

Note:

1. For QFP power supply signals, see .

Table 5-5. Pinout for VAC068A Plastic and Ceramic Quad Flatpack (160-Pin): Cavity Up

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	32	ID15	63	LD28	94	IOSEL1*
2	V_{SS}	33	FCIACK*	64	LD27	95	V_{DD}
3	LADO*	34	ASIZ0*	65	LD29	96	LA19
4	SWDEN*	35	ASIZ1*	66	V_{DD}	97	LA21
5	PIO13-IOSEL2*	36	CPUCLK	67	LD30	98	LA22
6	AS*	37	FC0	68	LD31	99	LA23
7	LDMACK*	38	FC1	69	MWB*	100	V_{DD} Core
8	DDIR	39	V_{SS}	70	FPUCS*	101	V_{SS}
9	ABEN*	40	V_{SS}	71	EPROMCS*	102	LA25
10	PIO11	41	V_{DD}	72	DRAMCS*	103	LA27
11	V_{SS}	42	V_{DD}	73	CACHINH*	104	LA24
12	PIO4-IORD*	43	FC2	74	RESET*	105	LA26
13	LADI	44	LAEN	75	V_{SS}	106	LA29
14	VSBSEL*	45	PAS*	76	LA11	107	LA28
15	LBR*	46	R/W*	77	LA8	108	LA31
16	BLT*	47	V_{DD}	78	IOSEL0*	109	PIO12-SHRCS*
17	REFGT*	48	DSACK1*	79	V_{DD}	110	LA30
18	SLSEL0*	49	DSACK0*	80	V_{DD}	111	CS*
19	ICFSEL*	50	LD19	81	V_{SS}	112	V_{SS}
20	V_{DD}	51	V_{SS}	82	V_{SS}	113	PIO10
21	V_{SS} Core	52	LD16	83	LA9	114	PIO9-IOSEL5*
22	SLSEL1*	53	LD21	84	LA12	115	PIO8-IOSEL4*
23	ID8	54	LD18	85	LA10	116	V_{DD}
24	ID10	55	LD23	86	LA14	117	PIO6-IOSEL3*
25	ID9	56	LD17	87	LA13	118	V_{DD}
26	V_{SS}	57	LD20	88	LA16	119	V_{SS}
27	ID11	58	LD22	89	LA15	120	V_{SS}
28	ID12	59	LD25	90	LA18	121	V_{DD}
29	ID13	60	LD24	91	V_{SS}	122	V_{DD}
30	ID14	61	V_{SS}	92	LA17	123	PIO5-IOWR*
31	WORD*	62	LD26	93	LA20	124	PIO3-RXDB

Table 5-5. Pinout for VAC068A Plastic and Ceramic Quad Flatpack (160-Pin): Cavity Up (continued)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
125	PIO2-TXDB	134	A24	143	A12	152	V_{DD}
126	PIO1-RXDA	135	V_{DD}	144	A11	153	A19
127	PIO0-TXDA	136	A27	145	A13	154	A20
128	A30	137	A25	146	V_{SS}	155	V_{SS}
129	A28	138	A9	147	A14	156	A21
130	A31	139	A8	148	A15	157	A22
131	V_{SS}	140	V_{SS}	149	A16	158	A23
132	A26	141	V_{DD}	150	A17	159	V_{DD}
133	A29	142	A10	151	A18	160	V_{DD}

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
A23	PIO13/ IOSEL2*	DDIR	PIO11	LADI	BLT*	REFGT*	ICFSEL*	SLSEL1*	ID8	ID11	ID13	ID14	ASIZ0	FC1	1
A20	A22	SWDEN*	VAS*	ABEN*	PIO4/ IORD*	VSBSEL*	SLSEL0*	IDI0	ID9	ID12	WORD*	FCIACK*	FC0	PAS*	2
A17	A19	A21	LADO	LDMACK*	VSS	LBR*	VDD	VSS	VSS	ID15	ASIZ1	CPUCLK	LAEN	DSACK1*	3
A16	A18	VSS	LOCATOR PIN									FC2	R/W*	LD19	4
A14	A15	VDD										VDD	DSACK0*	LD21	5
A12	A13	VSS										VSS	LD16	LD17	6
A10	A11	VDD										LD23	LD18	LD20	7
A08	A09	VSS										LD24	LD22	LD25	8
A25	A24	VDD										VSS	LD27	LD26	9
A27	A26	VSS										VDD	LD29	LD28	10
A29	A28	PIO0/ TXDA										DRAMCS*	LD31	LD30	11
A31	PIO1/ RXDA	PIO5/ IOWR*										VSS	EPROMCS*	MWB*	12
A30	PIO3/ RXDB	PIO7	PIO8/ IOSEL4*	VSS	LA29	VSS	VDD	VDD	VSS	LA13	LA9	LA11	CACHINH*	FPUCS*	13
P102/ TXDB	PIO6/ IOSEL3*	PIO10	CS*	LA31	LA26	LA24	LA22	IOSEL1*	LA17	LA15	LA14	LA12	LA8	RESET*	14
VDD	PIO9/ IOSEL5*	LA30	PIO12/ SHRCS*	LA28	LA27	LA25	LA23	LA21	LA19	LA20	LA18	LA16	LA10	IOSEL0*	15

Figure 5-16. VAC068A Pin Grid Array (PGA), Bottom View

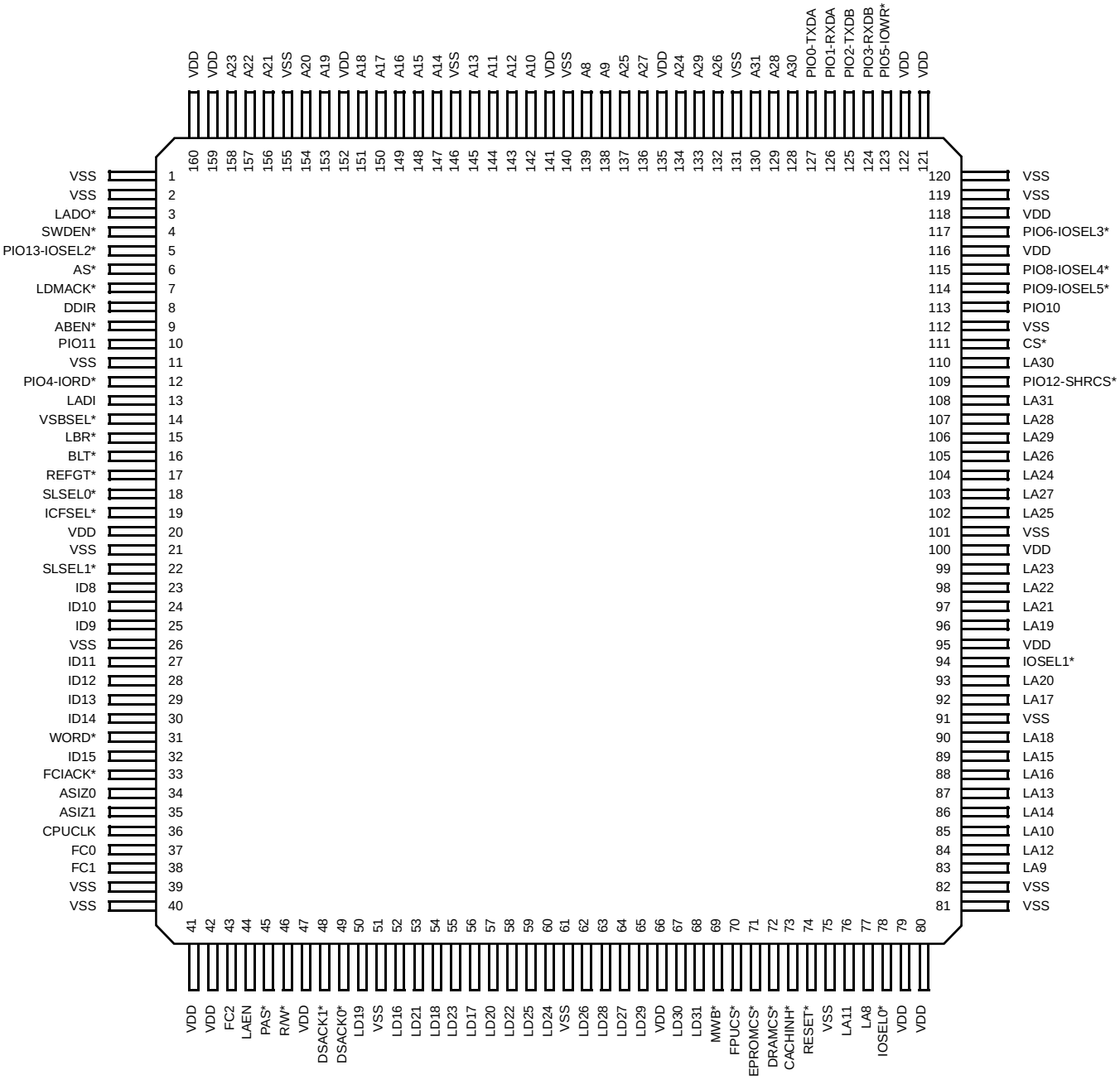

Figure 5-17. VAC068A Quad Flatpack (QFP), Top View