

Cypress Semiconductor CD-ROM

Programmable Logic

Part Number	Part Description	Last Updated
PLDs		
	Introduction to Cypress PLDs	11/01/95
	PLD Programming Information	03/17/97
CPLDs		
Delta39K™ CPLD Family	CPLDs at FPGA Densities™	07/05/01
Delta39K Pin Tables	CPLDs at FPGA Densities	04/09/01
Quantum38K™ CPLD Family	CPLDs at ASIC Prices™	07/05/01
Quantum38K Pin Tables	CPLDs at ASIC Prices	04/20/01
Ultra37000™ CPLD Family	UltraLogic™ High-Performance CPLDs	03/15/01
UltraLogic™ FLASH370i™ CPLD Family	UltraLogic High-Density Flash ISR CPLDs	07/20/00
CY7C371i	UltraLogic 32-Macrocell Flash ISR CPLD	07/10/00
CY7C372i	UltraLogic 64-Macrocell Flash ISR CPLD	07/10/00
CY7C373i	UltraLogic 64-Macrocell Flash ISR CPLD	07/10/00
CY7C374i	UltraLogic 128-Macrocell Flash ISR CPLD	07/09/01
CY7C375i	UltraLogic 128-Macrocell Flash ISR CPLD	07/10/00
FLASH370™ CPLDs	High-Density Flash CPLDs	07/20/00
CY7C371	UltraLogic 32-Macrocell Flash ISR CPLD	04/20/98
CY7C372	UltraLogic 64-Macrocell Flash ISR CPLD	04/01/98
CY7C373	UltraLogic 64-Macrocell Flash ISR CPLD	04/01/98
CY7C374	UltraLogic 128-Macrocell Flash ISR CPLD	04/01/98
CY7C375	UltraLogic 128-Macrocell Flash ISR CPLD	04/01/98
EPLDs		
CY7C340 EPLDs	Multiple Array Matrix High-Density EPLDs	07/19/00
CY7C341B	192-Macrocell MAX EPLD	12/09/99
CY7C341	192-Macrocell MAX EPLD	07/19/00
CY7C342B	128-Macrocell MAX EPLD	07/19/00
CY7C342	128-Macrocell MAX EPLD	07/19/00

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CY7C343	64-Macrocell MAX EPLD	07/18/00
CY7C343B	64-Macrocell MAX EPLD	12/08/99
CY7C344	32-Macrocell MAX EPLD	07/18/00
CY7C344B	32-Macrocell MAX EPLD	12/08/99
CY7C346	128-Macrocell MAX EPLD	07/18/00
CY7C346B	128-Macrocell MAX EPLD	12/08/99
SPLDs		
PALC20 Series	Reprogrammable CMOS PALC 16L8, 16R8, 16R6, 16R4	09/01/95
PALCE16V8	Flash Erasable, Reprogrammable CMOS PAL Device	09/03/98
PALCE20V8	Flash Erasable, Reprogrammable CMOS PAL Device	03/26/97
PLDC20G10B	CMOS Generic 24-Pin Reprogrammable Logic Device	03/26/97
PLDC20G10	CMOS Generic 24-Pin Reprogrammable Logic Device	03/26/97
PLDC20RA10	Reprogrammable Asynchronous CMOS Logic Device	03/26/97
PALCE22V10	Flash Erasable, Reprogrammable CMOS PAL Device	10/01/95
PALC22V10	Reprogrammable CMOS PAL Device	09/01/95
PALC22V10B	Reprogrammable CMOS PAL Device	03/06/97
PALC22V10D	Flash Erasable, Reprogrammable CMOS PAL Device	10/01/95
CY7C331	Asynchronous Registered EPLD	01/01/94
CY7C335	Universal Synchronous EPLD	03/26/97
	Inventra™ DMAxN-B1 Multi-Channel DMA Controller	2000
	Inventra HDLC-CORE-B1 Single Channel HDLC Core	2000
	Inventra M16550A-B1 UART with FIFOs	2000
	Inventra M16x50-B1 Enhanced 16550A-Compatible UART	2000
	Inventra MI2C-B1 I²C Bus Interface	2000
2001 Application Note	Interfacing the QDR™ to the Delta39K™	07/23/2001
2001 Application Note	Delta39K and Quantum 38K™ I/O Standards and Configurations	06/01/2001
2001 Application Note	Using FIFOs in Delta39K CPLDs	01/05/2001
2001 Application Note	Using the Delta39K ISR™ Prototype Board	01/19/2001
2001 Application Note	Delta39K and Quantum38K Dual-Port RAM	01/09/2001

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2000 Application Note	<u>Configuring Delta39K /Quantum38K</u>	05/02/01
2000 Application Note	<u>Delta39K PLL and Clock Tree</u>	07/06/01
2000 Application Note	<u>The Delta39K/Quantum38K Carry Chain</u>	09/25/00
2000 Application Note	<u>Targeting Cypress PLDs from the Leonardo Spectrum Environment</u>	08/10/00
2000 Application Note	<u>Targeting Cypress PLDs with Synplify® 6.0</u>	08/08/00
2000 Application Note	<u>Method to Instantiate and Use a Core in LeonardoSpectrum™</u>	08/22/00
2000 Application Note	<u>Method to Instantiate and Use a Core in Synplify™</u>	08/23/00
2000 Application Note	<u>Method to Instantiate and Use a Core in Warp Enterprise/Professional™</u>	08/23/00
2000 Application Note	<u>Method to Instantiate and Use a Core in Warp® with Cypress CPLDs</u>	08/21/00
2000 Application Note	<u>Importing a Warp Post-fit Netlist Into Mentor Graphics' ModelSim™</u>	08/22/00
1997 Application Note	<u>FLASH370™ Family of CPLDs and Designing with Warp2®</u>	03/06/97
1994 Application Note	<u>Design Optimization Using Warp Synthesis Directives</u>	04/01/94
1995 Application Note	<u>Targeting Cypress PLDs from the Cadence Environment</u>	01/01/95
1997 Application Note	<u>Designing with the CY7C335 and Warp 2 VHDL Compiler</u>	03/07/97
1999 Application Note	<u>Targeting Cypress PLDs from the Synopsys FPGA Express Environment</u>	02/19/99
1999 Application Note	<u>An Introduction to Active-HDL Sim</u>	04/02/99
1999 Application Note	<u>An Introduction to Active-HDL FSM</u>	04/02/99
1999 Application Note	<u>PCI Target Designs Using Ultra37000™ CPLDs</u>	05/19/99
1999 Application Note	<u>Implementing a Reframe Controller for the CY7B933 HOTLink®</u>	04/29/99
	<u>Receiver in a CY37032 CPLD</u>	
1999 Application Note	<u>Implementing a Synchronous DRAM Controller in Cypress CPLDs</u>	07/15/99
1999 Application Note	<u>An Introduction to In System Reprogramming with the Ultra37000</u>	05/07/99
1999 Application Note	<u>Board Layout Considerations for ISR™ Programming of Cypress CPLDs</u>	07/15/99
1999 Application Note	<u>Designing with Cypress ISR CPLDs for PC Cable Programming</u>	05/15/99
1999 Application Note	<u>Using Ultra37000 ISR Prototype Board</u>	04/28/99
1999 Application Note	<u>Converting Designs from FLASH to Ultra37000 Devices</u>	06/14/99
1999 Application Note	<u>ISR Programming Using an Embedded Processor with Jam™</u>	06/30/99
1999 Application Note	<u>CPLD Power Consumption Comparison (White Paper)</u>	04/01/99
1999 Application Note	<u>Power Estimation and Thermal Management for Cypress CPLDs</u>	04/05/99
1999 Application Note	<u>Using Heat Sinks with Larger CPLDs</u>	04/02/99
1998 Application Note	<u>Efficient Arithmetic Designs with Cypress CPLDs</u>	07/02/98
1998 Application Note	<u>Using IEEE 1149.1 Boundary Scan (JTAG) With Cypress Ultra37000 CPLDs</u>	11/18/98
1998 Application Note	<u>Understand Bus-Hold--A Feature of Cypress CPLDs</u>	02/01/98
1997 Application Note	<u>Using Hierarchy in VHDL Design</u>	03/05/97

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1997 Application Note	<u>Getting Started Converting .ABL Files to VHDL</u>	03/05/97
1997 Application Note	<u>Abel-HDL vs. IEEE-1076 VHDL</u>	03/06/97
1997 Application Note	<u>An Introduction to In System Reprogramming with FLASH370i</u>	03/05/97
1997 Application Note	<u>FLASH370i 5V to 12V DC-DC Converter Solutions</u>	01/01/97
1997 Application Note	<u>Are Your PLDs Metastable?</u>	03/06/97
1995 Application Note	<u>State Machine Design Considerations and Methodologies</u>	12/01/95
1995 Application Note	<u>Implementing a 128Kx32 Dual-Port RAM Using the FLASH370</u>	12/01/95
1995 Application Note	<u>Cascading ISR Devices</u>	01/01/95
1994 Application Note	<u>Using Cypress CPLDs in Mixed-Voltage Systems</u>	04/01/94