

PowerPC 740 Embedded Processor

200, 233, and 266MHz

Highlights

Power Management Unit

- Static low-power design
- Dynamic power management
- Integrated Thermal Management Assist Unit
- Doze, Nap, Sleep, and Deep Sleep power-saving modes

Instruction Fetching & Branch Unit

- 4 instructions fetched from L1 per clock
- 64-entry, 4-way set associative BTIC to eliminate branch delays
- 512-entry BHT for dynamic branch prediction

Dispatch Unit

- Dispatches 2 instructions per cycle
- 4-stage pipeline: Fetch, Dispatch, Execute, and Complete

Load/Store Unit

- One cycle cache access
- Executes cache and TLB instructions
- Alignment and number denormalization
- Hit under reload instruction

Fixed-Point Execution Units (2)

- FXU1 - multiply, divide, shift, rotate, arithmetics, and logicals
- FXU2 - shift, rotate, arithmetics, and logicals
- Single-cycle arithmetics, shift, rotate and logicals
- Hardware multiply and divide
- Early-out multiply

Floating-Point Execution Unit

- Optimized for single-precision multiply/add
- IEEE-754 standard single-and double-precision floating point arithmetic
- Thirty-two, 64-bit Floating Point Registers

System Unit

- Executes condition register logical, special register transfer, and other system instructions

Memory Management Unit

- 52-bit virtual and 32-bit real addressing
- 8 Block Address Translation registers
- 128-entry, 2-way data TLB
- 128-entry, 2-way instruction TLB
- Hardware table walk

Cache Unit

- 32K, 8-way set associative instruction cache
- 32K, 8-way set associative data cache
- 3-state coherency (MEI), 32 byte block
- Physically tagged and addressed
- Copy-back or write-through data cache
- I-cache throttling capability

Bus Interface Unit

- General purpose interface for a wide range of system configurations
- 32-bit address and 64-bit data bus
- Powerful diagnostic and test interface through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface
- Parity checking on bus
- Bi Endian operation

Product Description

The IBM PowerPC 740™ embedded processor is a 32-bit implementation of the PowerPC™ family of Reduced Instruction Set Computer (RISC) microprocessors. This processor is especially suitable for high-end communications and networking applications such as hubs, routers and LAN switches, as well as network computers and storage controllers. The PowerPC 740 delivers impressive application performance at a low typical power consumption of 4.2 watts at 200MHz.

Enhancements to the PowerPC 740 microprocessor family, compared to the PowerPC 603 microprocessor family, include:

- Performance monitor
- Thermal Assist Unit
- Higher clock frequencies delivering higher levels of performance with lower power consumption
- Doubled caches and TLBs
- Revised BIU and performance enhancements
- Hardware TLB-miss table walk
- 2x to 8x bus divider ratios, with half-step increments
- Dynamic branch prediction and branch instruction cache (BTIC)
- Second FXU/ALU



The PowerPC 740 is supported by the IBM27-82660 chipset, providing memory control and PCI Bridge functionality. An evaluation kit is

also available, which includes a development board, limited function compiler, ROM monitor source and debugger, and basic RTOS.

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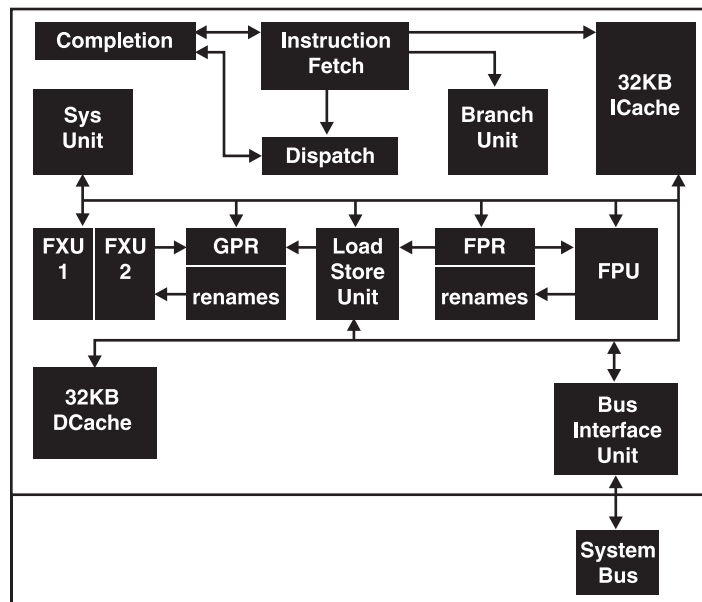
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PowerPC 740 Embedded Processor Specifications

Technology	0.25µm / 0.18 L _{eff} - CMOS 6S2 technology, five levels of metal
Die Size	7.56 mm x 8.79 mm (67 mm ²)
Performance (@ 266MHz)	11.5 SPECint95 (est.) 6.9 SPECfp95 (est.)
Number of Transistors	6.35 million
CPU bus Ratio	2X, 2.5X, 3X, 3.5X, 4X, 4.5X, 5X, 5.5X, 6X, 6.5X, 7X, 7.5X, 8X
L1 Cache	32K Instruction and 32K Data
I/Os	161 Signal, 79 Power
Power Supply	2.5V ± 100mV core 3.3V ± 5% I/O
Power Dissipation (Typ.)	4.2W @ 200MHz, 5.7W @ 266MHz
Temperature Range	0°C to 105°C
Packaging	Ball Grid Array (255 pins, 21mm x 21mm)



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