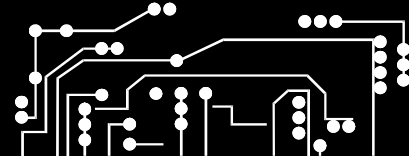


PowerPC Embedded Processors

Application Note



403GA/GC Migration to 403GCX

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Abstract - The 403GCX provides a direct pin replacement for the 403GA and 403GC for those users requiring a higher performance solution. This note covers the hardware and software implications of moving to a 403GCX.

The 403GCX contains a number of functional enhancements to the 403GA/ GC. To minimize the effort required to migrate, the 403GCX initialization state is compatible with the 403GA/GC. The functional enhancements must be configured to be used except for the cache size. The functional enhancements are:

Cache size - The only cache change is the increase in cache size. The instruction cache has been increased to 16K and the data cache to 8K. All other cache characteristics remain the same as the 403GA/GC.

Clock doubling - The 403GCX core contains clock generation logic enabling it to generate a core clock that is 2x the frequency of the clock input pin. This must be explicitly enabled by setting a bit in the IOCR of the 403GCX. The external interface continues to operate at the frequency of the input clock. The time base is part of the core and therefore increments at the core clock rate, which may affect timer routines.

Byte Parity - Four odd-parity bits will be multiplexed with trace outputs to permit parity checking on all external memory transfers and DMA operations. Trace will be unavailable when parity is enabled. The enable bits, which control parity generation and checking for external memory banks and DMA transfers, are located in a second 32-bit bank register.

Support for EDO DRAM - EDO DRAM is a new type of device that can offer substantial performance benefits for multiple accesses within a single page. A bit in the IOCR will modify the 403GCX BIU timings to take advantage of this family of DRAM devices. **Note when using EDO mode the DRAM read on CAS bit (IOCR bit 26) must be set to 0**

Sample on Ready in SRAM device paced mode - This change will allow the BIU to latch the data in the same cycle that Ready samples active. Currently the 403GA/GC latches the data in the next cycle after the 403GA/GC samples Ready as active. The behavior is selectable and controlled by a new bit in the IOCR.

Burst Last - Some peripheral devices and system designs expect an end of burst signal. In byte enable mode, the \overline{OE} pin becomes the end of burst, BLAST, signal.

The above listed functions are the differences between the 403GCX and the 403GC. There is another group of functions that are differences between the 403GA and the 403GC. The following list plus the above list covers the full 403GA to 403GCX differences. A summary of the register and bit changes for both lists of function follows the text description. The 403GA to 403GC functional changes are:

MMU added. The MMU highlights are:

- Variable page sizes, from 1KB to 16 MB
- 64 entry fully associative TLB
- Software reload of TLB entries
- Zone protection
- Precache MMU design, with TLB entries qualified by TID
- Control over real mode storage attributes
- New exception vectors for TLB miss on I side, and D side

Several new instructions are added to support the MMU: **tlbia**, **tlbre**, **tlbwe**, **tlbsx**, and **tlbsync**. In addition new Machine State Register (MSR) bits were added for real mode vs. virtual mode selection, and corresponding Save Restore Registers SRR1 and SRR3 bits were added. New Error Syndrome Register (ESR) bits were added; and new Special Purpose Registers (SPRs) were added for control of guarded storage (SGR), real-mode control of write policy (DCWR), and Process ID (PID). New interrupt vectors were added for TLB exceptions. The 403GC and GCX will power up in real mode.

Time Base Changes. The time base has been increased from 56 bits to 64 bits. The ability to read the time base in nonprivileged or user mode has been added through two new SPRs. Note that when running the GCX clock doubled the time base, and all derived hardware timers, increment at the doubled rate.

READY. Ready powers-up as synchronous, but can be programmed to accept an asynchronous Ready. The data is transferred during the third cycle after Ready is sampled.

Device Paced Time-Out. For the 403GA the bus will time out if Ready has not been received within 128 cycles. This time-out can be disabled in the IOCR for the 403GC.

Byte Enables. The 403GA uses write byte enables for control of bytes during write, but uses a common OE for all bytes during a read. The 403GC provides the capability to configure the write byte enables as just byte enables that are valid during both reads and writes by setting a bit in the IOCR. The timing does change when byte enable mode is selected. Please refer to the 403GC Data Sheet.

Address Tri State. The 403GA tri-states the address bus when it is not active. The 403GC allows the selection of address bus tri-state or hold last state when the bus is inactive.

DRAM Control Tri State. When enabled by a bit in the IOCR, the DRAM control lines are tri-stated during external bus master mode. This feature allows sophisticated external bus masters, such as graphics chips, to use their DRAM controller to access memory. In addition to the 403GA-Jx this change is not implemented in the 403GC-JA version of the part.

Reset. For the 403GA the Reset pin was driven low for 3 cycles following a reset instruction or the pin was pulled low externally. For the 403GC the Reset pin will drive low for 2048 cycles. Note that during power-up the Reset pin will drive low for 0-2047 cycles because the counter powers up with a random value.



Protection. The 403GA used bounds registers to provide a level of software protection. With the addition of the TLB, the 403GC can provide a much greater level of protection and flexibility. The bounds registers are still present and function as before, but they have been renamed in exception handling as the Data Storage Interrupt (DSI).

Detailed description of migration changes

The hardware issues will be covered first, followed by the software issues. For the 403GA/GC, pins 83, 84, 85, and 86 are exclusively used as trace debug pins. On the 403GA/GC they are outputs and their initial state is driving low. On the 403GCX these pins can be trace debug or byte parity. Their initial state is as inputs on the 403GCX. To avoid floating inputs we recommend pulling these pins to ground through a 10K resistor if byte parity is not being used.

The reset pin of the 403GA will drive low for 3 cycles after it is pulled low. On the 403GC and 403GCX the reset pin will drive low for 2048 cycles after it is pulled low. Any problem can be avoided if only passive pull-up is used on the reset line.

Pins 122, 123, 124, and 125 are $\overline{\text{WBE0:3}}$, write byte enable, pins on the 403GA. Reads are done across all bytes using pin 126 the $\overline{\text{OE}}$ pin. The initial state of these pins on the 403GC and GCX are as $\overline{\text{WBE0:3}}$ with the same functionality as the 403GA. On the 403GC and GCX the $\overline{\text{WBE0:3}}$ pins can be configured in the IOCR to operate as byte enables whether the cycle is read or write (IOCR bit 20, BEM=1). The timing differences between the two modes are detailed in the Data Sheet for the 403GC and GCX. When the 403GC is in byte enable mode (BEM=1) the system designer may choose whether or not to use the $\overline{\text{OE}}$ pin. For the 403GCX in byte enable mode pin 126, $\overline{\text{OE}}$, is configured to operate as an end of burst signal, Burst last (BLAST).

- There is a difference in the software migration effort from the 403GA to the 403GCX versus the 403GC to 403GCX. This is due to the MMU on the 403GC and 403GCX. The assumption is made that systems designers looking for a simple drop-in upgrade from the 403GA to the 403GCX will not be using the MMU.

Cache synonyms (Instruction relocation only)

Note: The following information is only of concern if the MMU is being used, instruction relocation is active, and page sizes are 4KB or smaller.

To increase performance during instruction access, the 403GC/GCX implementations access the cache and translate the address in the same cycle. The address is translated and the cache tags for the selected congruence class are read in parallel during the first portion of the cycle, while the tags are compared to the translated address and the instruction selected from the appropriate side in the second portion of the cycle. As long as the cache set size (cache size divided by associativity) is the same or smaller than the physical page size, the bits used to access the congruence class and the bits that are translated are disjoint and the congruence class selection and address translation can occur in parallel. For example, the 403GC has a cache set size of 1KB (2KB / 2 way). Thus 10 bits (Address bits A22-A31) are needed to select a byte within the set. The minimum page size is 1KB, meaning that the lowest order 10 bits (A22-A31) select the byte within the page and thus are not translated. Therefore address translation of A0-A21 can occur in parallel with cache access using A22-A31. The larger cache set size of the 403GCX (16KB / 2 way = 8KB set) presents a problem in that there are 13 bits (Address A19-A31) needed to select a byte from the set, while A0-A21 are still translated for a 1KB page.

This causes an overlap between bits 19:21, introducing the notion of cache synonyms. If multiple virtual addresses map to the same real page, the information may appear multiple times in cache. For 1KB pages, virtual addresses matching in bits A0-A18 and A22-A27 but differing in bits 19:21 may have cache synonyms. For 4KB pages, virtual addresses differing in bit 19 will be affected.

The practical effect of this situation occurs when a real instruction page with multiple virtual mappings exists in the cache in multiple places and must be cast out of the cache. For 1KB pages, each virtual address differing in bits 19:21 must be cast out of cache (via **icbi**) individually; up to 8 per cache line in the page. For 4KB pages, each virtual address differing in bit 19 must be cast out; up to 2 per cache line in the page. For larger pages, there are no synonyms and casting out any one of the multiple virtual addresses removes the physical information from cache.

The following is a summary of program model changes.

Register	Description 403GA/GC	Description 403GCX	Init GA GC/GCX
BESR[3:5] 0x91	00x-Protection Violation 01x-Access to a non-configured bank 10x-Active level on bus error input pin 11x-Bus time-out Bit 3,4 active, Bit 5 reserved	000-Protection violation 001-Parity error 010-Access to a non-configured bank 011-Reserved 100-Active level on bus error input pin 101-Reserved 110-Bus time-out 111-Reserved	0

Register	Description	Init GA	Init GC	Init GCX
BRH0[0] 0x70	Parity Enable, 0=disable 1=enable	N/A	N/A	0
BRH1[0] 0x71	Parity Enable, 0=disable 1=enable	N/A	N/A	0
BRH2[0] 0x72	Parity Enable, 0=disable 1=enable	N/A	N/A	0
BRH3[0] 0x73	Parity Enable, 0=disable 1=enable	N/A	N/A	0
BRH4[0] 0x74	Parity Enable, 0=disable 1=enable	N/A	N/A	0
BRH5[0] 0x75	Parity Enable, 0=disable 1=enable	N/A	N/A	0
BRH6[0] 0x76	Parity Enable, 0=disable 1=enable	N/A	N/A	0
BRH7[0] 0x77	Parity Enable, 0=disable 1=enable	N/A	N/A	0

Register	Description	Init GA	Init GC	Init GCX
DCWR[0:31] 0x3BA	Data cache write-thru, bit per 128MB region 0=copy back, 1=write thru See NOTE	N/A	Random	Random

Register	Description	Init GA	Init GC	Init GCX
DMACR0[28] 0xC0	Enable parity checking on DMA Channel 0, 1=on 0=off	N/A	N/A	0
DMACR1[28] 0xC8	Enable parity checking on DMA Channel 1, 1=on 0=off	N/A	N/A	0
DMACR2[28] 0xD0	Enable parity checking on DMA Channel 2, 1=on 0=off	N/A	N/A	0
DMACR3[28] 0xD8	Enable parity checking on DMA Channel 3, 1=on 0=off	N/A	N/A	0

Register	Description	Init GA	Init GC	Init GCX
ESR[8] 0x3D4	Data storage exception-store operation	N/A	0	0
ESR[9]	Data/Instruction storage exception- zone fault	N/A	0	0

Register	Description	Init GA	Init GC	Init GCX
IOCR[12] 0xA0	DRAM Tri-state enable, 0=disable 1=enable	N/A	0	0
IOCR[13]	Enable sampling on Ready , 0=disable 1=enable	N/A	N/A	0
IOCR[16]	Enable EDO DRAM mode, 0=disable 1=enable	N/A	N/A	0
IOCR[17]	Enable core clock doubling, 0=disable 1=enable	N/A	N/A	0
IOCR[18]	Address bus Tri-state, 0=tri-state 1=Drive last value	N/A	0	0
IOCR[19]	Static power disable, 0=normal, 1=low power, note early RAS and TLB array disabled	N/A	0	0
IOCR[20]	Byte enable mode, 0= $\overline{\text{WBE}}$ are write byte enables, 1=WBE are Read/Write byte enables (timing is altered)	N/A	0	0
IOCR[21]	Device paced time-out, 0=128 cycle time-out on Ready, 1=No time-out on external cycles (OPB time-out unaffected)	N/A	0	0
IOCR[24]	Asynchronous Ready, 0=data is latched 1 cycle after Ready (setup time required) 1=data is latched 3 cycles after Ready (no setup time requirement)	N/A	0	0

IOCR[27:28]	Real-Time Debug Mode 00-Trace status outputs disabled 01-Program status and bus status 10-Program status and trace output 11-Byte parity on trace outputs (GCX only)	00	00	00
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Register	Description	Init GA	Init GC	Init GCX
MSR[26]	Instruction address translation, 0=off 1=on	N/A	0	0
MSR[27]	Data address translation, 0=off 1=on	N/A	0	0

Register	Description	Init GA	Init GC	Init GCX
PID[24:31] 0x3B1	Process identification	N/A	Random	Random

Register	Description	Init GA	Init GC	Init GCX
PVR[0:31] 0x11F	Process version register	0x00200011	0x00200200	0x00201400

Register	Description	Init GA	Init GC	Init GCX
SGR[0:31] 0x3B9	Storage Guarded, bit per 128MB region 0=normal, 1=guarded See NOTE	N/A	0xFFFFFFFF	0xFFFFFFFF

Register	Description	Init GA	Init GC	Init GCX
SRR1[26] 0x01B	Instruction relocate- value is loaded from MSR on non-critical Interrupt	N/A	Random	Random
SRR1[27]	Data relocate- value is loaded from MSR on non-critical Interrupt	N/A	Random	Random
SRR3[26] 0x3DF	Instruction relocate- value is loaded from MSR on Critical Interrupt	N/A	Random	Random
SRR3[27]	Data relocate- value is loaded from MSR on critical interrupt	N/A	Random	Random

Register	Description	Init GA	Init GC	Init GCX
TBHI[0:7] 0x3DC	Upper 8 bits of time base	N/A	Random	Random
TBHU[0:31] 0x3CC	Time base high user mode-read only	N/A	TB high	TB high
TBLU[0:31] 0x3CD	Time base low user mode-read only	N/A	TB low	TB low

Register	Description	Init GA	Init GC	Init GCX
ZPR[0:31] 0x3B0	Zone protection register	N/A	Random	Random

Exception Vector Offsets

Offset	Exception type	GA	GC	GCX
0x0300	Data storage interrupt	Protect bounds	Protect bounds or TLB protection violation (zone or write violation)	Protect bounds or TLB protection violation (zone or write violation)
0x0400	Instruction Storage Interrupt	N/A	TLB protection violation (zone or Ex=0 or G=1)	TLB protection violation (zone or Ex=0 or G=1)
0x1100	Data TLB miss	N/A	When translation is enabled	When translation is enabled
0x1200	Instruction TLB miss	N/A	When translation is enabled	When translation is enabled

Note: Initialization of the 403GCX must take care of the registers that power up in a random or active state. This is especially true of those migrating from the 403GA since most of the new registers were added when the MMU was added to the 403GC. The DCWR register should be set to zeros and the SGR register should be set to put the proper memory regions in normal mode. This should be done as one of the first items in the initialization routine.

Following is a code example of cache initialization that uses the Processor Version Register to use one piece of code to properly initialize any of the 403Gx processors , including the 403GCX.

```

!-----
! Invalidate i-cache and d-cache TAG arrays.
! User Processor Version Register to determine which processor
! and the proper number of congruence classes.
!
! 403GA/403GB/403GC ( 1K D-cache, 2K I-cache)
!   32 data cache congruence classes
!   64 instruction cache congruence classes
!
! 403GCX:      ( 8K D-cache, 16K I-cache)
!   256 data cache congruence classes
!   512 instruction cache congruence classes
!-----

mfppvr r4
rlwinm r4,r4,24,24,31    ! use bits 16:23 of pvr to determine
cmpi   cr0,0,r4,0x14     ! which processor
bne    not_403GCX        ! 0x00=>GA 0x01=>GB 0x02=>GC 0x14=>GCX
addi   r7,r0,256         ! set r7 to # of lines in data cache
                        ! for loop count- GCX has 256 lines
b      dcache
not_403GCX:
addi   r7,r0,32          ! set r7 to # of lines in data cache
                        ! for loop count- GA & GC has 32 lines
dcache:
addi   r6,0,0x0000       ! clear GPR 6
mtctr  r7                ! set loop ctr
dclloop:
dccc  0,r6              ! invalidate line
addi   r6,r6,0x10        ! bump to next line
bdnz   dclloop
icache:
addi   r6,0,0x0000       ! clear GPR 6
rlwinm r7,r7,1,0,31      ! double r7 since i cache has twice
                        ! lines of the d cache for all 403s
mtctr  r7                ! set loop ctr
icloop:
iccci  0,r6              ! invalidate line
addi   r6,r6,0x10        ! bump to next line
bdnz   icloop

```

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